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The characteristics of the high-K Er_2O_3 (erbium oxide) dielectrics deposited on polycrystalline silicon

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ABSTRACT

The high-k Er_2O_3 films deposited on polycrystalline silicon treated with various post-rapid thermal annealing (RTA) temperatures were formed as high k dielectrics. In order to study the annealing effects, electrical measurements, optical characterizations, and multiple material analyses techniques including X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), and atomic force microscopy (AFM) were performed to examine the differences between the samples in various annealing conditions. The annealing temperature at 800 °C was the optimal condition to form a well-crystallized Er_2O_3 film with excellent material quality and electrical properties. RTA annealing at an appropriate annealing temperature of 800 °C might effectively mitigate the dangling bonds and traps and improve electrical and material properties of the dielectric.

1. Introduction

Recently, various high dielectric constant (K) materials have been recommended to replace SiO_2 for solving reliability issues. Due to low gate leakage current and high gate capacitance, rare earth (RE) oxide dielectrics such as La_2O_3, Pr_2O_3, and Gd_2O_3 have been intensively investigated as SiO_2-replacing materials [1–3]. In addition to these materials, erbium oxide (Er_2O_3), which is valuable for applications in photonics, telecommunications, and optics for its photoluminescence (PL) and electroluminescence (EL) properties, has also been demonstrated to be interesting as an alternative gate oxide with a dielectric constant K about 10–14 [4–6], a wide band gap (~5.4 eV), and a relatively large conduction band offset. Functioning as a protective and corrosion-resistant coating [7] because of high chemical and thermal stability, Er_2O_3 may also be a promising candidate as a suitable gate dielectric layer.

According to previous reports [4–6], high-$k$$Er_2O_3$ layers were put directly on the silicon layer as a conventional way to form high-k dielectrics. In this study, the inter-dielectrics (polyoxides), which exhibited low conductivity, high breakdown fields and high charge to breakdown, substituted the traditional silicon layer. Furthermore, Er_2O_3, a promising high-k material with superior dielectric strength and lower gate leakage current, was deposited by RF sputtering on polycrystalline treated with post RTA annealing as an alternative method to fabricate high-k inter-dielectrics for future nonvolatile applications.

Different from previous studies, post rapid thermal annealing (RTA) was applied to improve the high-$k$$Er_2O_3$ layer as inter-dielectrics deposited on polycrystalline silicon. To monitor the annealing effects on the dielectrics, multiple material analysis, electrical measurements and optical characterizations were used to examine the differences between the as-deposited sample and the sample annealed in various temperatures. Regarding electrical properties, the capacitance versus voltage (C–V) equivalent oxide thickness (EOT) measurements, the J–E (current density versus electric field) characteristics under both polarities, and the gate voltage shift (ΔV_g) under constant current stress were evaluated by using a HP4200 semiconductor parameter analyzer. As for the physical properties, a combination of X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), and atomic force microscopy (AFM) was performed to characterize the crystalline structure, material composition, and the morphology between the Er_2O_3 and Poly-Si interface. Besides, photoluminescence measurements were incorporated to assess the presence and the concentration of the defect structure. By a thorough structural, electrical, and optical investigation, we could find the optimal annealing condition to improve the dielectric with excellent physical and electrical properties.

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2. Experimental details

The dielectric was fabricated on an $n+$ polysilicon/oxide/p-type silicon substrate. First, the p-type Si wafer was thermally oxidized to have a SiO_2 layer of 550 nm. A 300 nm thickness polysilicon film was deposited on the oxide layer at 625 °C by a low pressure chemical vapor deposition (LPCVD) system. Then, the wafer was implanted with phosphorous at a 5×10^{15} cm^{-2} dosage with activated energy of 30 keV for 30 s in an N_2 ambient at 950 °C to obtain a sheet resistance of 60–70 Ω/sq. After that, the native oxide was removed by dipping in diluted hydrofluoric acid (HF) solution. A 35 nm Er_2O_3 gate dielectric was deposited by RF Sputtering system on top of the processed substrate. After the gate dielectric was formed, the sample was treated by rapid thermal annealing (RTA) for 30 s in N_2 ambient at various temperatures of 600 °C, 700 °C, 800 °C, and 900 °C to improve the quality of the thin film. After the RTA treatment, an aluminum gate of a thickness of 300 nm was deposited and patterned by photolithography and wet etching to complete the fabrication of the high-$k$$Er_2O_3$ dielectric.

3. Results and discussion

To gain insight to the change in the high-$k$$Er_2O_3$ dielectric with various annealing conditions, a combinational material analysis of XRD, XPS and AFM was adopted to investigate the physical properties among the as-deposited sample and the samples treated at various temperatures. The XRD spectra of the Er_2O_3 dielectrics under various annealing conditions are presented in Fig. 1. In the XRD spectrum of the as-deposited sample, one small peak was around $2\theta = 30°$ and several weak features were around $2\theta = 47.45°$ and $47.85°$, indicative of a poor crystallized Er_2O_3 structure. The tiny peak around $2\theta = 30°$ could be indexed to the (100) reflection of hexagonal erbium. As the annealing temperature increased to 600 °C, the tiny peak around $2\theta = 30°$ in the spectrum became much weaker while another peak around $2\theta = 33°$ emerged, which could be indexed to the (222) reflection of hexagonal erbium, indicative of a distortion of the hexagonal lattice [8,9]. This distortion could be related to either oxygen inclusions in the erbium lattice or the superposition of the reflection patterns of erbium and Er_2O_3. In the spectra of the samples annealed at 700 °C and 800 °C, the (222) peak around became stronger, implying that a better crystallized Er_2O_3 structure was formed. The strongest (222) peak in the XRD spectra occurred in the sample annealed at 800 °C, showing a preferential orientation of the (222) planes of cubic Er_2O_3 parallel to the substrate. As the annealing temperature elevated to a high temperature of 900 °C, the diffraction pattern of the (222) peak diminished, signifying that some chemical reactions at a high annealing temperature of 900 °C might occur to form a badly crystallized Er_2O_3 structure.

Besides, to monitor the structural and compositional changes of the Er_2O_3 film in detail, the XPS spectra for the samples in different annealing conditions were investigated. According to Pan et al.'s studies [10], the X-ray photoelectron spectroscopy (XPS) has been used to explore the structural and compositional properties of the high-k films with thickness above 10 nm deposited on a silicon substrate. Fig. 2(a) shows the variation in Er 4d peak as a function of the annealing temperature. The Er 4d peaks of the samples annealed at 600 °C, 700 °C, and 800 °C shifted closer to the indexed peak energy of Er_2O_3 (168.4 eV) due to oxygen bonding to erbium. Compared with the as-deposited sample, the slightly higher signal intensities of Er 4d peak of the annealed sample at 800 °C in the binding energy suggest that the formation of well crystallized Er_2O_3 after annealing. As the annealing temperature went up to 900 °C, the Er 4d peak shifted back to a lower binding energy (167.5 eV) by approximately 0.9 eV. There was a sudden

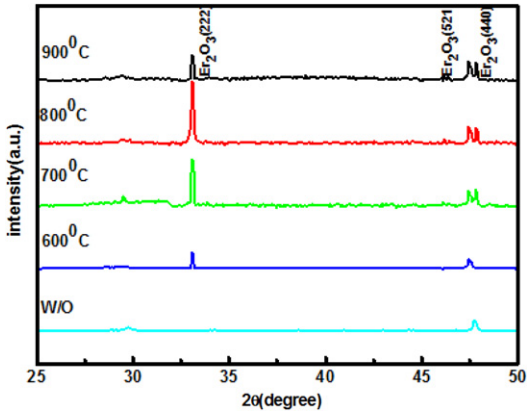

Fig. 1. XRD results of the Er_2O_3 film annealed at 600 °C, 700 °C, 800 °C, and 900 °C in N_2 ambient for 30 s.

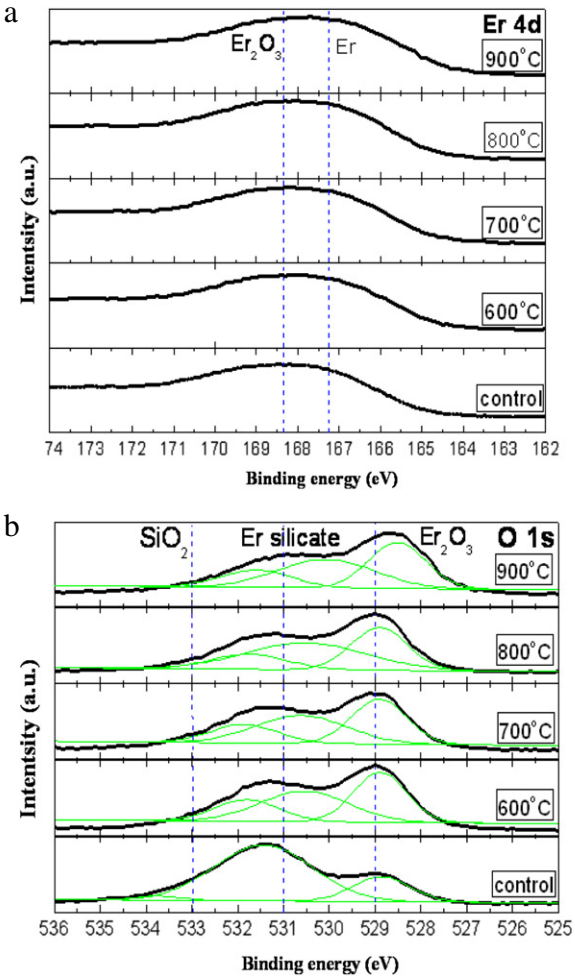

Fig. 2. XPS results of (a) Er 4d, and (b) O 1s of the Er_2O_3 film annealed at 600 °C, 700 °C, 800 °C, and 900 °C in N_2 ambient for 30 s.

change in the Er bonding status at 900 °C, indicating that an inferior crystallized Er_2O_3 was formed due to the Er atoms out-diffusion toward the interface at high-temperature annealing.

Besides, as shown in Fig. 2(b), the O 1s XPS spectra of high-$k$$Er_2O_3$ film for the samples annealed at various temperatures in N_2 ambient for 30 s. The spectra in Fig. 2(b) were deconvoluted into three Gaussian features corresponding to three peaks of chemical states. The peak of the low energy state centered at 529 eV was caused by the O atoms in Er_2O_3 [11], the peak of

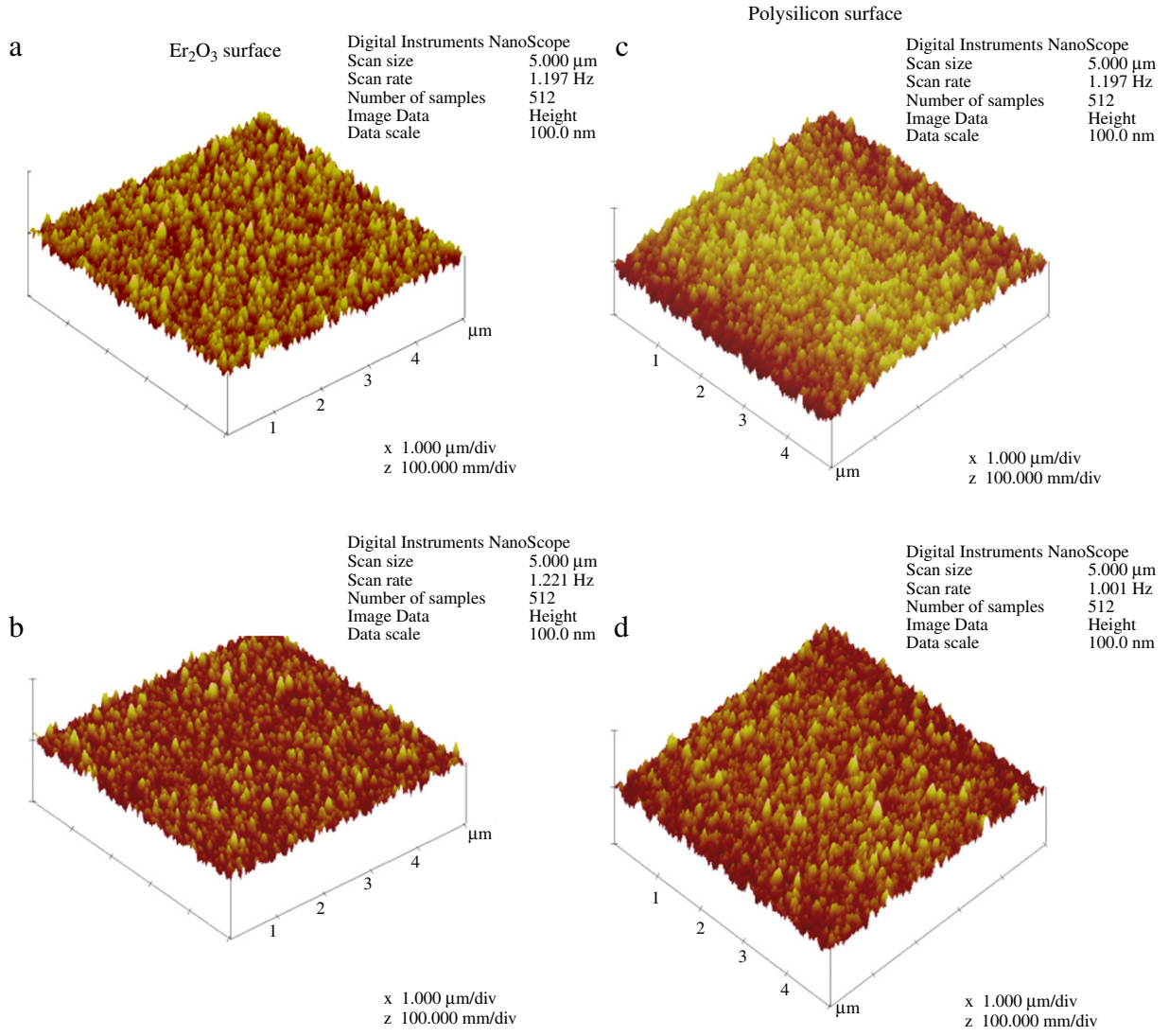

Fig. 3. AFM images of the Er_2O_3 surface of (a) the as-deposited sample and (b) the sample treated at 800 °C RTA annealing; AFM images of the polysilicon surface of (c) the as-deposited sample and (d) the sample annealed at 800 °C in N_2 ambient for 30 s.

the intermediate energy state centered at 531 eV was due to the interfacial O atoms in nonstoichiometric $ErSi_xO_y$, and the peak of the high energy state centered at 533 eV was attributed to the O atoms in SiO_2 [12]. The spectrum of the as-deposited sample was composed of the components of Er_2O_3, Er silicate, and SiO_2. The O 1s peak intensity corresponding to Er_2O_3 became stronger after post-annealing at 600 °C, 700 °C, and 800 °C, indicating that annealing at a proper temperature could enhance the formation of a well crystallized Er_2O_3 structure. Moreover, the highest O 1s peak corresponding to Er_2O_3 appeared at an optimal annealing temperature of 800 °C, which was consistent with all the aforementioned material analysis. Also, as the annealing temperature went up to 900 °C, the peak corresponding to Er_2O_3 shifted to a lower energy, suggesting that an inferior crystallized Er_2O_3 was formed due to the Er atoms out-diffusion toward the interface because of a high annealing temperature of 900 °C [13].

Furthermore, to visualize the surface texture of the interface practically, AFM was integrated to examine the surface roughness of the as-deposited and the sample annealed at 800 °C as shown in Fig. 3(a) and (b). Based on the AFM images of the Er_2O_3 surface for the as-deposited and the annealed sample, the RMS (root mean square) surface roughness values were 7.38 nm and 5.63 nm, respectively. Consistent with the aforementioned XRD and XPS analysis, the sample annealed at 800 °C had a smoother Er_2O_3 surface than the as-deposited sample did, indicative of the increase of the grain size due to the formation of a well crystallized Er_2O_3 in this annealing condition. According to the AFM analysis, the post RTA annealing treatment enhanced the Er_2O_3 grain formation and hence improved the smoothness of the surface texture. Furthermore, the high-$k$$Er_2O_3$ layer was removed with wet etching so that the AFM analysis could reveal the morphology of the interface between the high-$k$$Er_2O_3$ dielectric and the polysilicon as shown in Fig. 3(c) and (d). According to the AFM results, the interface roughness between the high-$k$$Er_2O_3$ dielectric and polysilicon had also been improved from 7.89 nm (as-deposited) to 5.85 nm by post-RTA annealing at 800 °C. As for the interfacial region, the reaction of Er, O and Si may cause non-uniform polysilicon grain boundary and rough interface between the high-$k$$Er_2O_3$ dielectric and polysilicon, proper annealing can minimize the interface states to form better interface. According to the AFM images, proper annealing at 800 °C can cause more uniform surface, indicating the decrease of the interface states in the interfacial region.

On the other hand, the electrical characteristics of the high-$k$$Er_2O_3$ dielectric annealed in different conditions were also studied. First, we measured the EOT of the samples extracting from

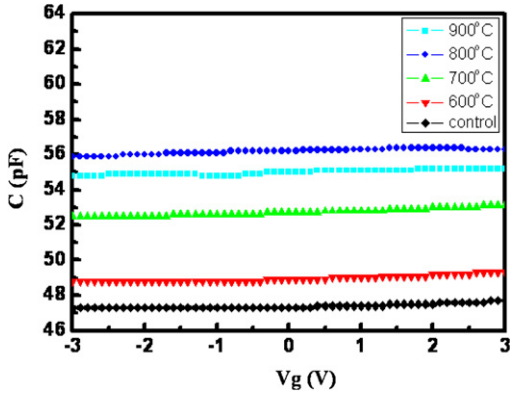

Fig. 4. High frequency capacitance–voltage (C–V) curves of the as-deposited sample and the samples annealed at 600 °C, 700 °C, 800 °C, and 900 °C in N_2 ambient for 30 s.

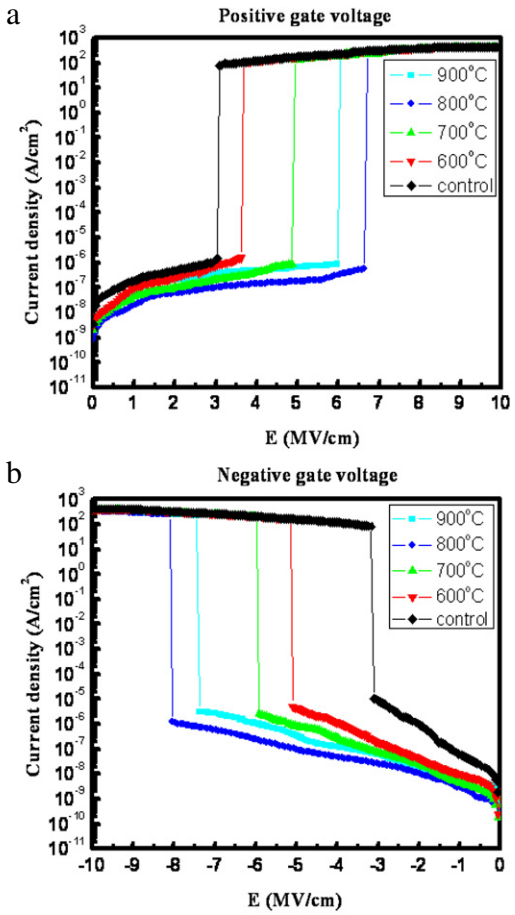

Fig. 5. The current density versus electric field (J–E) characteristics of the as-deposited sample and the samples annealed at 600 °C, 700 °C, 800 °C, and 900 °C under the top gate applied with (a) positive bias and (b) negative bias.

the high frequency C–V curves shown in Fig. 4. The capacitance values and relative dielectric constants (K) of the as-deposited and the sample annealed at 600, 700, 800, and 900 °C were 46.2 pF (8.57), 47.9 pF (8.91), 52.5 pF (9.75), 54.6 pF (10.19), and 50.7 pF (9.39). Hence, the EOT values of the samples were 182, 175, 160, 153, and 166 Å for the above samples. The results indicate that high temperature annealing could effectively decrease the EOT and improve dielectric reliability. However, when the annealing temperature went up to 900 °C, the EOT increased slightly again.

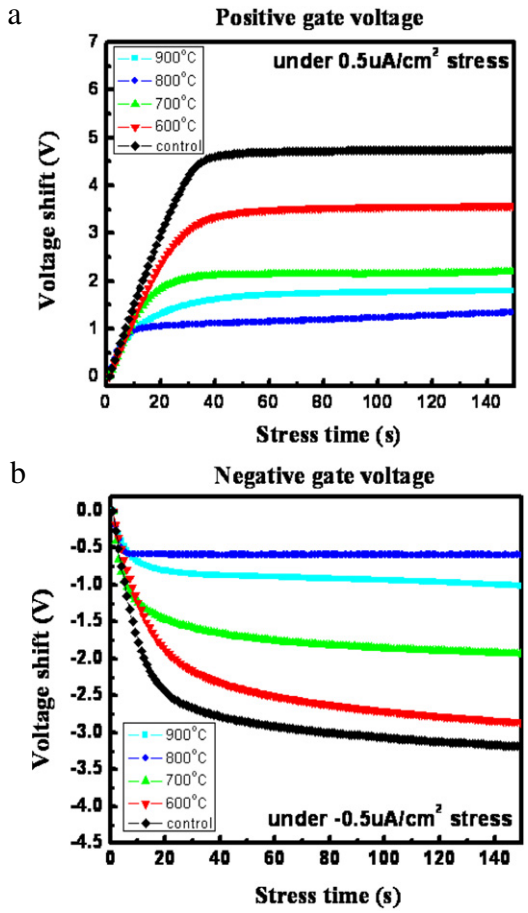

Fig. 6. The gate voltage shift versus time for the as-deposited sample and the samples annealed at 600 °C, 700 °C, 800 °C, and 900 °C under the (a) +0.5 μA/cm^2 constant current stress and (b) −0.5 μA/cm^2 constant current stress.

The J–E (current density versus electric field) characteristics as shown in Fig. 5(a) and (b) were performed under both polarity for $-V_g$ (electron injection from top gate electrode) and $+V_g$ (electron injection from bottom n+-polysilicon electrode) to investigate the breakdown electric field. The breakdown electric field increased as the post rapid thermal annealing temperature elevated from 600 °C to 800 °C, and within this temperature range the leakage current under the high electrical field both under substrate $+V_g$ and gate $-V_g$ bias was suppressed. Since the post-RTA annealing could passivate the dangling bonds and traps inside the high-$k$$Er_2O_3$ dielectric and the interface between the high-$k$$Er_2O_3$ dielectric and polysilicon, the samples would have better electrical characteristics with a higher RTA annealing temperature in this range. However, as the annealing temperature went up to 900 °C, the quality of the sample became worse. The breakdown electric field decreased and the leakage current increased, indicating that more dangling bonds and traps were formed.

Furthermore, the gate voltage shift (ΔV_g) versus time as shown in Fig. 6(a) and (b) were also measured under 0.5 μA/cm^2 and −0.5 μA/cm^2 constant current stress for the samples in different annealing conditions. Similarly, the sample with post rapid thermal annealing treatment at 800 °C had the smallest gate voltage shifts among the as-deposited sample and the samples treated at various annealing temperatures. Since the increase in the gate voltage was due to electron trapping, the sample with post-RTA annealing at 800 °C exhibited the lowest electron trapping rate, which was consistent with the aforementioned electrical measurements and material analyses. The results further confirm that the RTA annealing at an appropriate annealing temperature of

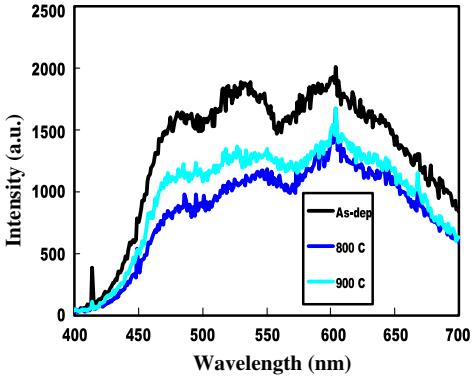

Fig. 7. PL spectra of the defect-related luminescence from the as-deposited sample and the samples annealed at 600 °C, 700 °C, 800 °C, and 900 °C.

800 °C might effectively mitigate the dangling bonds and traps in the dielectric layer and the interface between high-k dielectric and polysilicon. Therefore, the electrical results of the samples were also in line with all the material analyses.

Finally, PL measurements were incorporated to zoom in the defect structure such as dangling bonds and traps [14]. The PL measurement was conducted on the dielectric. The sample was stimulated by a 257 nm Argon laser and the emission light was collected by a spectrometer. Since the defect states could generate a continuous spectrum, the concentration of the defect could be detected by evaluating the intensity of defect-related luminescence [15]. As shown in Fig. 7, the as-deposited sample had a strong defect-related luminescence spectrum. As the annealing temperature increased to 800 °C, the luminescence intensity drastically decreased, signifying that the dangling bonds and the traps were passivated by the annealing. However, as the annealing temperature further increased to 900 °C, the defect-related luminescence became stronger again, indicating that annealing at a high temperature might cause some chemical reactions to enhance the formation of a bad crystallized Er_2O_3 structure. The optical investigation results were congruent with all the material analyses and electrical measurements.

4. Conclusions

The high-$k$$Er_2O_3$ gate dielectrics deposited on polycrystalline silicon were fabricated. The samples treated at different annealing temperatures were examined by applying various material, optical, and electrical analyses. All the electrical test and structural examination concluded that annealing temperature at 800 °C was the optimal condition that could form a well-crystallized Er_2O_3 film. The high-$k$$Er_2O_3$ dielectric is promising for future generation of electronic device applications.

References

[1] T. Hamada, Y. Saito, M. Hirayama, H. Aharoni, T. Ohmi, IEEE Electron Device Lett. 22 (2001) 423.
[2] J.H. Klootwijk, H. van Kranenburg, P.H. Woerlee, H. Wallinga, IEEE Trans. Electron Devices 46 (1999) 1435.
[3] C.H. Kao, C.S. Lai, C.L. Lee, J. Electrochem. Soc. 153 (2006) 128.
[4] W. He, S. Schuetz, R. Solanki, J. Belot, J. McAndrew, Electrochem. Solid-State Lett. 7 (2004) G131.
[5] A. Sakai, S. Sakashita, M. Sakashita, Y. Yasuda, S. Zaima, S. Miyazaki, Appl. Phys. Lett. 85 (2004) 5322.
[6] V. Mikhelashvili, G. Eisenstein, F. Edelman, R. Brener, N. Zakharov, P. Werner, J. Appl. Phys. 95 (2004) 613.
[7] J.P. Zhou, C.L. Chai, S.Y. Yang, Z.K. Liu, S.L. Song, Y.L. Li, N.F. Chen, J. Cryst. Growth 270 (2004) 21.
[8] V. Mikhelashvili, G. Eisenstein, F. Edelmann, Appl. Phys. Lett. 80 (2002) 2156.
[9] M. Miritello, R. Lo Savio, A.M. Piro, G. Franzo, F. Priolo, F. Iacona, C. Bongiorno, J. Appl. Phys. 100 (2006) 013502.
[10] T.M. Pan, T.Y. Yu, Y.Y. Hsieh, J. Appl. Phys. 102 (2007) 074111.
[11] J.F. Moulder, W.F. Stickle, P.E. Sobol, K.D. Bomben, Handbook of X-Ray Photoelectron Spectroscopy, Perkin-Elmer, Eden Prairie, MN, 1992.
[12] M.P. Singh, C.S. Thakur, K. Shalini, T. Shripathi, N. Bhat, S.A. Shivashankar, in: 204th The Electrochemical Society Meeting, 539, 2003.
[13] C.H. Kao, H. Chen, J.S. Chiu, K.S. Chen, Appl. Phys. Lett. 96 (2010) 112901.
[14] C. Delerue, G. Allan, M. Lannoo, Phys. Rev. B 48 (1993) 11024.
[15] M. Akazawa, A. Domanowska, B. Adamowicz, H. Hasegawa, J. Vac. Sci. Technol. B 27 (2009) 2028.