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Characterizations and thermal stability improvement of phase-change memory device containing Ce-doped GeSbTe films

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ABSTRACT

Phase-transition temperature of GeSbTe (GST) chalcogenide film was drastically increased from 159 to 236 °C by cerium (Ce) doping (up to 8.6 at.%) without altering the resistivity property of GST. Grain refinement *via* the solid-solution mechanism and the amplification of *p*-type semiconducting behavior in Ce-doped GST were observed. They were correlated with the enhancement of thermal stability and data retention property of GST as revealed by exothermal and isothermal analyses. Phase-change memory (PCM) device characterized at various temperatures revealed an effective thermal stability improvement on the threshold voltage of PCM device by Ce doping.

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1. Introduction

Phase-change memory (PCM) based on the reversible phase-change property of chalcogenide thin films has been recognized as one of the promising candidates for next-generation non-volatile memories due to its low power consumption, high operation speed, high recording density and excellent scalability to nanometer-scale cell sizes. In addition, PCM is also feasible to multi-state memory since the chalcogenide programming layer exhibits a relatively large resistivity difference (about 10^5 times) in between amorphous and crystalline states [1,2]. This is far more significant than the reflectivity change up to 30% for the same phase-change chalcogenides applied to optical memory devices.

Presently, GeSbTe (GST)-based chalcogenides are the most popular programming layer materials for PCM. However, as the device sizes continuously scale down, insufficiency in material properties of GST gradually restraints the device performance, *e.g.*, writing current, thermal stability, and overwrite capability. Various methods have been proposed to overcome these difficulties and, in addition to adjusting the chemical constitutions of chalcogenides, the modification of physical properties by alien-element doping is often employed. Nitrogen (N) [3,4], oxygen (O) [5], silicon oxide (SiO_x) [6], silicon (Si) [7], molybdenum (Mo) [8], tin (Sn) [9,10], and bismuth (Bi) [10] have been added into GST and their feasibilities to PCM have been evaluated. Among these, nonmetallic N element seems to be the most promising one for physical properties adjustment. As to the metallic dopants, they were reported to accelerate the recrystallization rate of GST [11]. Nevertheless, metallic dopants often reduce the resistivity level of amorphous GST and suppress the resistivity ratio of the amorphous and crystalline GST [8].

Most dopants reported previously [3–7,8–10] are the Group IVA, VA or VIA elements with the electron configurations similar to those of Ge, Sb and Te. In this work, cerium (Ce) is chosen as the dopant of GST for the following reasons: (*i*) distinctive electron configuration of the Group IIIB rare-earth element; (*ii*) relatively small electronegativity (χ) in comparison with the elements of GST ($\chi_{Ce}=1.1$–1.2; $\chi_{Ge}=1.8$; $\chi_{Sb}=1.9$; $\chi_{Te}=2.1$); (*iii*) relatively large atomic size of Ce in comparison with Ge, Sb and Te ($r_{Ce}=0.185$ nm; $r_{Ge}=0.125$ nm; $r_{Sb}=0.145$ nm; $r_{Te}=0.140$ nm). In addition to the chemical bond alternation in GST due to the difference in χ for physical property modification, it is anticipated that Ce may present as the substitutional-type dopant in GST and relevant study would provide a good comparison with the N dopant which has been reported as the interstitial-type solute in GST [4].

2. Experimental details

Electrical properties and microstructures of pristine GST and Ce-doped GST layers are investigated in this work. 150-nm thick thin-film samples were deposited on the thermally oxidized Si substrates by using a sputtering system at background pressure better than 6.7×10^{-4} Pa without substrate heating. Ce doping was realized by the target-attachment method [8] in which the doping concentration was adjusted by the amounts of Ce foils mounted on the GST target

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($Ge_2Sb_2Te_5$; purity: 99.99%; supplier: Tosima, Japan). The Ce foils (purity: 99.99%) were supplied by Alfa Aesar, USA.

The composition of specimen was analyzed by using an inductively coupled plasma-mass spectrometer (Perkin Elmer SCIEX ELAN 5000) operated at RF power = 1000 W, carrier gas flow rate = 1.3×10^{-5} m^3/s, auxiliary gas flow rate = 2×10^{-5} m^3/s and plasma gas flow rate = 2.5×10^{-4} m^3/s. Evolution of microstructures of the samples were analyzed by an in-house *x*-ray diffractometer (M18XHF, MAC Science) within Cu-K_α radiation (λ = 0.1542 nm) at scanning rate of 0.033°/s. The microstructures of the samples were also examined by a transmission electron microscope (TEM, Philips Tecnai 20) operating at 200 kV and the energy dispersive spectrometer (EDS, Link ISIS 300) attached to TEM was adopted for composition analysis. The method of plan-view TEM sample preparation is briefed as follows. Pristine and Ce-doped GST layers about 50 nm in thickness were deposited on the KBr substrates. After dissolving away the KBr in a dish of de-ionized water, the GST thin films were dragged out of the water, mounted on the copper mesh, and immediately transferred to TEM for characterization. Ecopia HMS-3000 Hall-effect analyzer was utilized to analyze the effects of Ce-doping on the charge carrier type and transport properties of GST.

Static-mode current–voltage (*I–V*) characteristics were determined by using an *I–V* source meter (Keithley Instruments Inc., Model 2400) equipped with a self-assembly heating apparatus in vacuum ambient with pressure better than 0.13 Pa. Meanwhile, cross-point-type PCM devices with 5-μm contact hole containing pristine GST or Ce-doped GST as the programming layers were prepared. The device structure with the electrical characterization setup is schematically shown in Fig. 1.

3. Results and discussion

Composition analysis revealed the Ce content in doped GST samples monotonously increases with the increase of area coverage ratio of Ce foils on GST target. For instance, the doped sample prepared at the condition of Ce area coverage ratio = 7% resulted in about 8.6 at.% Ce in GST. Similar increasing trend was also observed in the characterization of phase-transition temperature of Ce-doped GST as revealed by subsequent *in-situ* electrical property measurement. Since the increase trend of phase-transition temperature alleviated and intermetallic phases seemed to emerge in the samples prepared at area coverage ratio of Ce = 10%, in below we report the analytical results of Ce-doped GST prepared at Ce area coverage ratio = 7% (termed GST7C hereafter). Characterizations for pristine GST sample are also presented for the purpose of comparison.

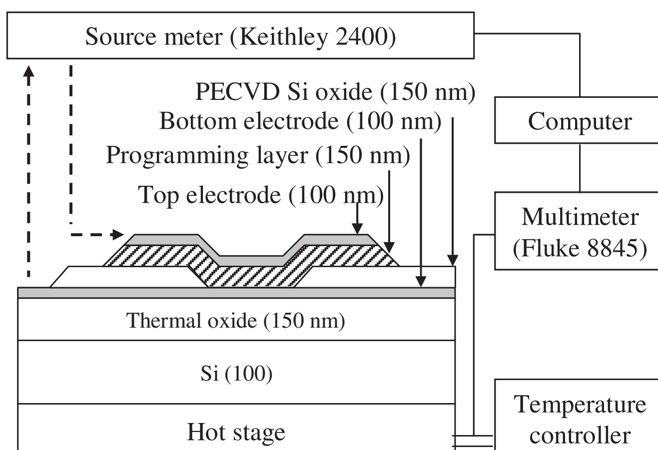

Fig. 1. Cross-sectional view of PCM device and the electrical characterization setup.

Fig. 2 shows the XRD profiles of as-deposited samples and samples subjected to 300 °C/1-h and 350 °C/1-h annealing treatments. Absence of characteristic peaks in diffraction patterns of as-deposited samples indicates the samples deposited at room temperature are amorphous. High-temperature treatments are known to result in the recrystallization of GST; however, Fig. 2 indicates GST transforms from meta-stable face-centered cubic (FCC) to stable hexagonal structure when temperature increases from 300 to 350 °C while the FCC structure is preserved in the GST7C heated up to 350 °C. This illustrates Ce doping is able to stabilize the GST in FCC status. Further, a careful inspection of XRD patterns found the Ce doping causes the XRD peaks shift to smaller diffraction angle side. Meanwhile, a calculation of full-width-half maximum (FWHM) of $(200)_{FCC}$ peaks for the samples heated at 300 °C for 1 h found that the FWHM of GST7C layers = 1.61° while that of GST = 1.12°. This implies that Ce doping results in the lattice expansion and grain size refinement of GST. The lattice expansion is ascribed to the relatively large atomic radius of Ce in comparison with those of Ge, Sb and Te.

Fig. 3(a) and (b) separately presents the plan-view TEM micrographs, both bright- and dark-field images, in conjunction with the selected area electron diffraction (SAED) patterns for GST and GST7C samples subjected to 300 °C/1-h annealing. Grain size reduction in GST7C due to Ce doping can be readily seen, in agreement with the XRD analysis presented previously.

Fig. 3(c) shows the EDX element mapping on a specific area of GST7C sample shown in Fig. 3(b). Separation of Ge-rich and SbTe-rich phases can be observed in accord with the element image contrast; however, Ce element mapping indicates a nearly uniform dispersion of Ce in GST7C. Since the XRD analysis shown in Fig. 2 revealed no Ce-related intermetallic compounds (IMCs) in GST, it implies that Ce presents in a form of solid solution in GST in composition range studied in this work. The Ce atoms should disperse in GST lattice as the substitutional solutes due to the comparatively large atomic size of Ce. The stress field induced by the difference in atomic sizes may inhibit the grain boundary motion and hence result in the grain refinement of GST7C as depicted in Fig. 3(b).

Fig. 4(a) depicts the typical resistivity (ρ) and corresponding derivative (${}^{d}\rho/{}_{d}T$) profiles for 150-nm thick GST and GST7C layers as a function of temperature measured at a heating rate of 1 °C per minute. A unique features observed in Fig. 4(a) is, unlike other metallic dopants, Ce doping barely affects the levels of ρ for amorphous GST and the resistivity ratio of amorphous and crystalline GST remains the same at about 10^5 times. At the same temperature level, the

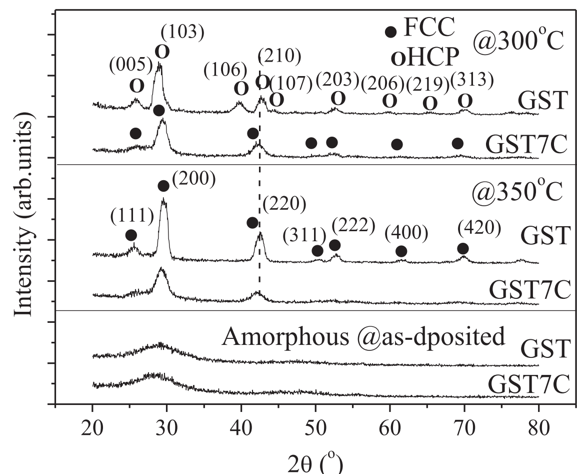

Fig. 2. XRD patterns of as-deposited GST and GST7C layers and the samples subjected to 300 and 350 °C annealing for 1 h.

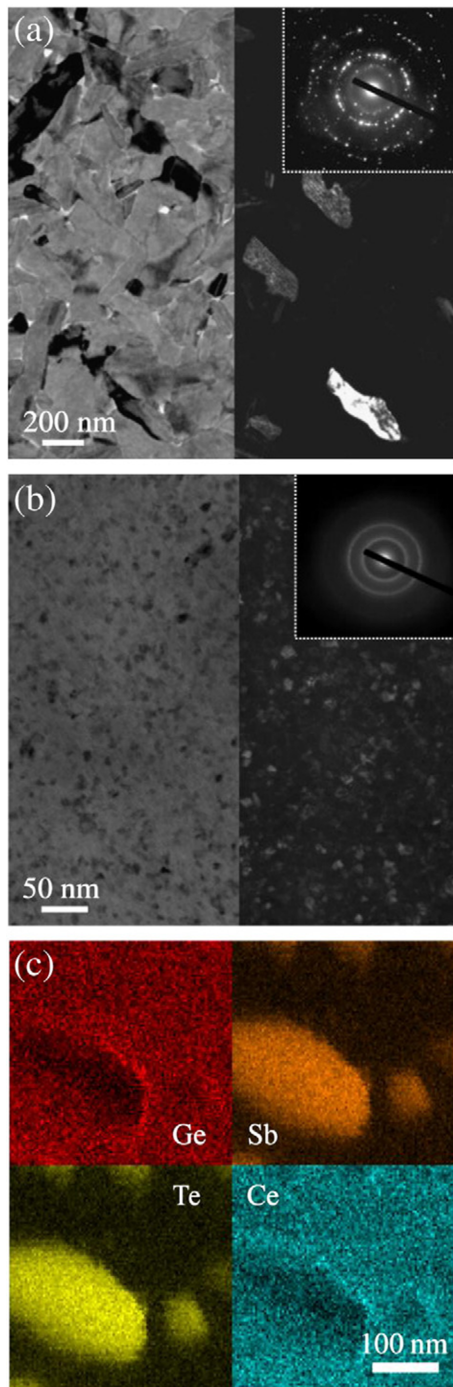

Fig. 3. Plan-view TEM micrographs of (a) GST and (b) GST7C samples subjected to the annealing at 300 °C for 1 h. Bright-field image (left-hand part), dark-field image (right-hand part) and SAED patterns (upper right-hand side) are presented simultaneously. (c) EDX element mapping for Ge, Sb, Te, and Ce in a specific area of GST7C sample shown in (b).

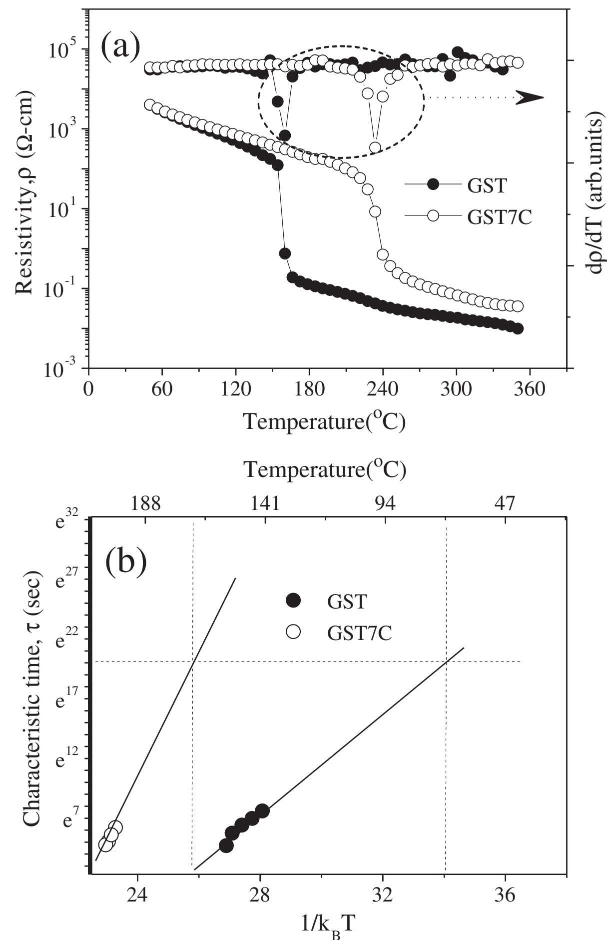

Fig. 4. (a) Typical profiles of ρ and corresponding derivatives $({}^{d}\rho/{}_{d}T)$ as a function of temperature measured at a heating rate of 1 °C per minute for GST and GST7C. (b) A plot of characteristic time *versus* reciprocal of temperature.

crystalline GST7C exhibits a higher level of ρ in comparison with the pristine GST. This is ascribed to the grain refinement effect due to Ce doping and will benefit the reduction of writing current when the Ce-doped GST is implanted in the PCM devices.

Since the values of ρ decrease with the increase of temperature as depicted in Fig. 4(a), both the pristine and the Ce-doped GSTs, either in amorphous of crystalline state, possess the semiconducting feature. Charge carrier property measurement indicated both samples are *p*-type semiconductors with the hole concentrations $= 3.55\times10^{20}$ and 2.92×10^{21} cm^{-3}, respectively. Presumably, the amplification of acceptor-like characteristics in Ce-doped GST is correlated to the electronic configuration of Ce which is known as $[Xe]4f^{1}5d^{1}6s^{2}$. The partially-filled inner 4*d* and 5*f* orbitals in Ce might provide additional acceptor levels in the bandgap structure of GST for hole carrier generation. The hole concentration increment and the crystallinity improvement in crystalline GST7C would benefit the electrical conduction; nevertheless, the presence of grain boundaries and lattice distortion cause by Ce doping discourage the propagation of charge carriers so as to neutralize the conduction improvement. This results in moderate conductivity suppression for crystalline GST7C in comparison with the crystalline GST.

Previous studies reported that the metallic dopants usually suppress the resistivity level or, promote the conduction of amorphous GST [8–10]. In GST7C sample, the electrons at outermost 6*s* orbital of Ce likely induce the resistivity drop. However, stress fields caused by the difference of atomic sizes in between Ce and elements in GST matrix would disturb the carrier migration. Such a carrier scattering effect might be a key factor to inhibit the drop of ρ in amorphous GST7C as illustrated in Fig. 4(a). We however note this work is a preliminary study of Ce-doped GST. Topics such as the effect of dopant's electronic configuration on the electrical properties of doped GST, the effects of Ce doping on bandgap structure and bonding configurations of GST, either in amorphous or crystalline state, remain to be investigated in order to characterize the origin of transport property changes in Ce-doped GST.

According to the derivative profiles of resistivity depicted in Fig. 4(a), recrystallization temperatures (T_x) for GST and GST7C were determined as 159 and 236 °C, respectively (see Table 1). This illustrates Ce doping may stabilize the amorphous GST. The increment of T_x is ascribed to the uniformly dispersed Ce solutes in GST matrix that inhibit the grain growth and coalescence during recrystallization.

Presently N doping is widely recognized as the most promising method to modify the physical properties of chalcogenides [3,4]. Analytical results presented above indicate Ce doping is as effective as N doping to improve the recrystallization property of GST; however, N doping simultaneously increases the resistivity levels of amorphous and crystalline GST [3,4,8] whereas, as depicted by Fig. 4(a), Ce doping does not dramatically alter the resistivity levels of amorphous and crystalline GST. In other words, N doping shifts the resistivity profile toward high-resistivity side while Ce doping shifts the resistivity profile toward the high-temperature side in the plot of resistivity against temperature. When the PCM cells are programmed, adjacent amorphous bits suffer the parasitic heating which might result in the data loss. Such a thermal cross-talk phenomenon has become a concern of PCM under the trend of device scale-down [2]. Thermal resistance is known to correlate with the phonon and electron scattering in the bulk of material. In PCM, thermal boundary resistance (TBR) is another issue that considerably affects the temperature distribution of programming layer and the device performance [12–14]. TBR is resulted from the scattering process at the interface and its influence exaggerates when the difference in resistance across the interface becomes large. According to the resistivity properties presented above, it can be inferred that N doping pronounces the thermal resistance heating and TBR effects in the devices whereas Ce doping might alleviate the thermal cross-talk in between PCM cells in the trend of device scale-down. Further, in a view of fabrication Ce doping can be achieved by conventional sputtering using the composite GST target containing appropriate amount of Ce. Though N doping can also be realized by simply allowing the N_2 gas flow during deposition, it nevertheless induces the reactive sputtering that the etching effect caused by inadequate N_2 gas flow would degrade the film quality. As a result, Ce is a promising dopant for the modification of GST properties as well as the enhancement of PCM performance.

Both exothermal experiment in conjunction with Kissinger theory [15] and isothermal experiment in conjunction with Arrhenius formulation [16] were carried out in this study and the activation energies, E_a and E_a^f, corresponding to these two types of experiments were calculated accordingly. As summarized in Table 1, Ce doping escalates both the values of E_a and E_a^f. During the isothermal process, the change of ρ is in essential driven by the percolation effect [8] and this process can be elucidated by a characteristic time, τ, in the plot of ρ *versus* time. A plot of τ *versus* the reciprocal of T for GST and GST7C is shown in Fig. 4(b). This allows us to determine the maximum temperatures of sample retention by extrapolating method [16]. For 10-year retention, the maximum temperatures for GST and GST7C samples were found to be 76 °C and 170 °C, respectively. In conjunction with the values of E_a and E_a^f listed in Table 1, it illustrates that Ce doping may effectively enhance the thermal stability of GST layers and thereby benefit the data retention of PCM.

Fig. 5(a) and (b) presents the static-mode *I–V* characteristics of PCM devices containing GST and GST7C programming layers at various test temperatures. It can be seen that the switching threshold voltage (V_{th}) increases with the Ce doping (V_{th} = 1.90 V for GST and V_{th} = 3.30 V for GST7C at room temperature). Since the proposal of chalcogenides for PCM devices, the threshold switching phenomenon has attracted numerous research interests and its origin is still in debate. The explanations include microscopic phase change [17], thermally induced instabilities [18], carrier generation by impact ionization [19,20], and the mobility gap of an amorphous material [21,22]. In the viewpoint of phase-change process, V_{th} is related to the requirement of a significant current passing through the cell and the generation of heat by Joule effect to induce the phase transition. Presumably, GST7C is able to produce a larger V_{th} due to its larger E_a than that of GST. In accord with the profiles shown in Fig. 5(a) and (b), the temperature dependence of V_{th} can be obtained and is plotted in Fig. 5(c). Though each device features the decrease in V_{th} with the

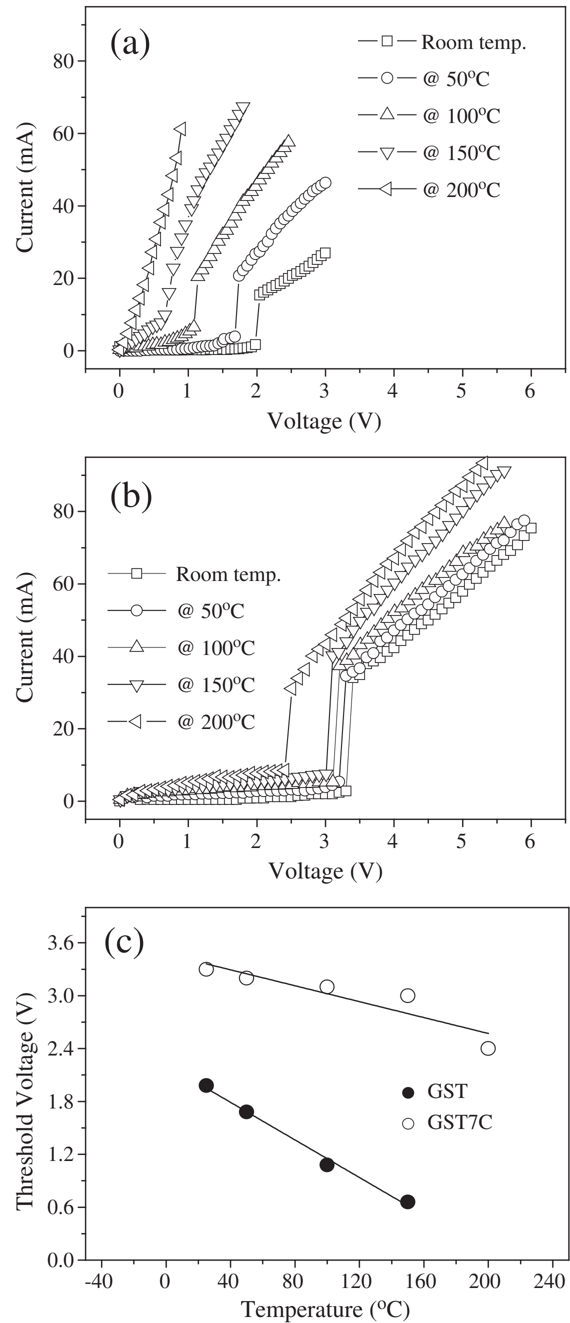

Fig. 5. Static *I–V* profiles for PCM devices containing (a) GST and (b) GST7C as the programming layers at various test temperature. (c) The temperature dependence of V_{th} of PCM devices.

Table 1
A list of the values of T_x, E_a, E_a^f, and temperatures for 10-year retention of amorphous state of GST and GST7C layers.

Samples	T_x (°C)	E_a (eV)	E_a^f (eV)	Temperatures for 10-year retention (°C)
GST	159	2.05 ± 0.1	2.3 ± 0.3	76
GST7C	236	4.53 ± 0.1	4.63 ± 0.2	170

increase of temperature, GST7C device is superior to GST device in terms of stability in V_{th} at various temperatures. Another feature shown in Fig. 5(c) is that the V_{th} of GST7C device is less sensitive to the temperature change in comparison with GST device. Without the incorporation of dopants, pristine GST exhibits an obvious change in grain size during the amorphous-to-crystalline transition as illustrated by Fig. 3(a). By forming the obstacle of grain boundary motions, Ce stabilizes the microstructure of GST7C (see Fig. 3(b)) and consequently leads to the stabilization of physical properties for doped sample subjected to temperature change. Analytical results presented above confirm that Ce doping may enhance the thermal stability of amorphous GST and result in a better PCM device stability [6,7]. Further, Ce doping effectively refines the grains of GST and this would benefit the scale-down of PCM devices and the reduction of writing current as revealed by the resistivity property presented in Fig. 4(a).

4. Conclusions

In summary, this work demonstrates a metallic dopant type, Ce, which may effectively enhance the thermal stability of GST without degrading its electrical properties. Analytical results indicated that Ce-doping effectively refines the microstructure of GST *via* the solid-solution mechanism. Enhancement of *p*-type semiconducting property was observed in Ce-doped GST, implying the dopant's electronic configuration likely plays a key role in the property modification of GST. The difference in ρ for amorphous and crystalline Ce-doped GST remains at about five orders of magnitude without the loss of phase-change reversibility. At the same temperature level, Ce-doping was found to escalate the level of ρ of crystalline GST which, in turn, benefits the writing current reduction for PCM applications. As compared with pristine GST device, GST7C device exhibited a better stability in switching threshold property. With such distinctive electrical properties, Ce-doped GST can be a promising chalcogenide for PCM device applications with better signal contrast preservation and high-density signal storage capability. The findings reported in this work may also benefit the development of optical storage media if the analysis on optical properties of Ce-doped GST were accomplished.

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