Design of a Subthreshold-Supply Bootstrapped CMOS Inverter Based on an Active Leakage-Current Reduction Technique

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***Abstract*—This brief presents a bootstrapped CMOS inverter operated with a subthreshold power supply. In addition to improving the driving ability, a large gate voltage swing from $-V_{DD}$ to $2V_{DD}$ suppresses the subthreshold leakage current. As compared with other reported works, the proposed bootstrapped inverter uses fewer transistors operated in the subthreshold region. Therefore, our design has shorter delay time. The Monte Carlo analysis results indicate that a sigma of delay time is only 6.3 ns under the process and temperature variations with 200-mV operation. Additionally, a test chip is fabricated in the 90-nm SPRVT low-K CMOS process. Chip measurement results demonstrate the feasibility of operating ten-stage bootstrapped inverters with a 200-fF loading of each stage at 200-mV V_{DD}. The test chip is able to achieve 10-MHz clock rate at 200 mV V_{DD}, the power consumption is 1.01 μW, and the leakage power is 107 nW.**

***Index Terms*—Bootstrapped circuit, leakage-current reduction, low-voltage circuit, subthreshold circuit.**

I. Introduction

SCALING power supply has become popular in low-power CMOS VLSI in the recent years. Although many approaches, even down to the subthreshold supply, achieve ultralow power consumption [1]–[3], the driving capability of CMOS devices in the subthreshold region remains challenging. While requiring a large area to compensate for driving efficiency in subthreshold power supply, a conventional CMOS-tapered buffer also incurs a severe $I_{\rm off}$ problem in the nanometer process. Bootstrapping is an effective means of enhancing the speed in order to raise the driving efficiency. Therefore, a previous work has developed a bootstrapped CMOS driver for large capacitive loads [4]. According to Fig. 1(a), the bootstrapped driver consists of a pull-up and pull-down control pair to drive the PMOS and NMOS transistors, respectively. In the design of Lou and Kuo, the gate voltages of PMOS and NMOS driver transistors are kept V_{DD} and 0 in the cutoff phase. In the driving phase, the gate voltages of PMOS and NMOS transistors are fed $-V_{DD}$ and $2V_{DD}$ to increase the current density. Several researchers have proposed some improvements based on the architecture in Fig. 1(a). Despite a previous effort [5] to increase the boosting efficiency by rearranging the timing of the switching and boosting signals, reverse leakage current remains the main drawback of conventional bootstrapped drivers.

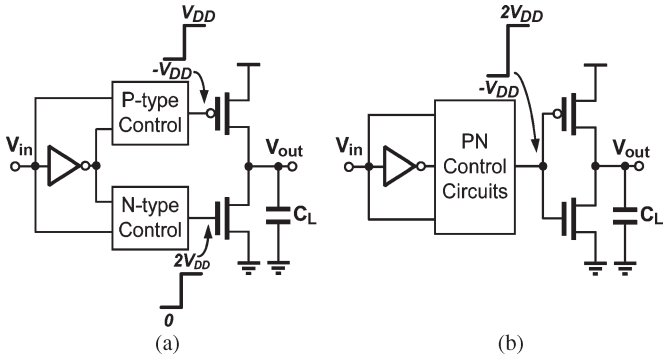

Fig. 1. (a) Conventional bootstrapped circuit. (b) Proposed bootstrapped circuit.

Kil *et al.* proposed a precharge enhancement scheme to accelerate the bootstrapped circuit operations [6]. That scheme also feeds back the output boosting signal to effectively suppress the reverse leakage current and maintain the output boosting voltage level. However, extra capacitors increase the hardware cost by two folds. Due to the inherent limitations of the precharge bootstrapped circuit, precharge enhancement scheme rapidly degrades at a high frequency. Additionally, static power in this design encounters a serious problem since it accounts for most of the power consumption. Among other bootstrapped circuits, single capacitor ones reduce the costs of the hardware overhead [7], [8]. However, their complex circuitry design seriously degrades charge sharing at the capacitor node. Moreover, the leakage current is problematic as well.

This brief introduces a bootstrapped CMOS inverter to achieve high boosting efficiency and improve the speed. The proposed circuit is applicable in both increasing driving ability by boosting signals into the superthreshold region and reducing the leakage current in the subthreshold region. Fig. 1(b) illustrates the circuit diagram. Theoretically, the PN bootstrap circuit produces an output swing of $-V_{DD}$ to $2V_{DD}$. The $2V_{DD}$ $(-V_{DD})$ value enhances the driving capability of the NMOS (PMOS) driver and suppresses the leakage

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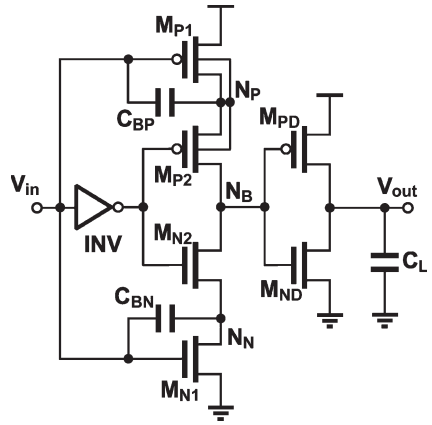

Fig. 2. Proposed bootstrapped inverter.

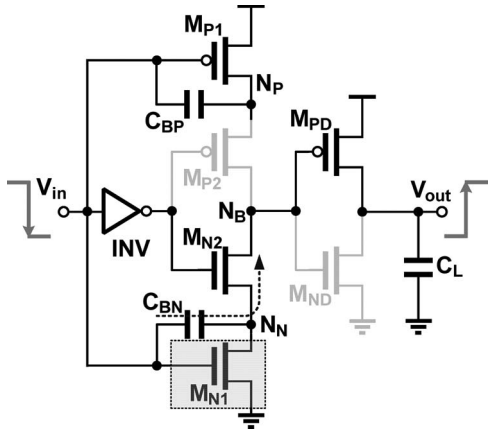

Fig. 3. Proposed bootstrapped inverter operations (input H to L).

for the PMOS (NMOS). The PN bootstrap circuit provides V_{SG} $(V_{GS}) = 2V_{DD}$ and turns on the PMOS (NMOS) driver. In contrast, a negative V_{SG} $(V_{GS}) = -V_{DD}$ suppresses the leakage current, while the PMOS (NMOS) driver is turned off. Moreover, as compared with other previous works, the proposed design scheme has fewer devices in the subthreshold region. Consequently, that explains why the process variation affects the proposed design scheme to a lesser extent.

The rest of this brief is organized as follows. Section II introduces the structure and the operations of the circuit. Section III then evaluates in detail the performance of the proposed circuit, which includes the leakage current, the delay, and the Monte Carlo analysis on the process variation. Next, Section IV summarizes the test chip and the measurement results. Conclusions are finally drawn in Section V, along with recommendations for future research.

II. Proposed Bootstrapped CMOS Inverter

Fig. 2 schematically depicts the proposed bootstrapped CMOS inverter, where $C_{\rm BP}$ and $C_{\rm BN}$ are the bootstrap capacitors, M_{P1} and M_{N1} are the transistors for $C_{\rm BP}$ precharge and $C_{\rm BN}$ predischarge, INV refers to the inverter to control M_{P2} and M_{N2}, $M_{\rm PD}$ and $M_{\rm ND}$ are the output drivers for C_L, and N_P and N_N are the boosted nodes. Node N_B is boosted above V_{DD} and below ground to enhance the driving capability. Figs. 3 and 4 show the operations with the input switching from H to L and from L to H, respectively. Fig. 5 shows the simulated transient waveforms with an output load of 0.5 pF under a power supply of 200 mV. According to this figure, before $V_{\rm in}$ transits from H to L, node N_N has the initial voltage of 0 V. After transiting from H to L, N_N is boosted below ground to (-188 mV). Meanwhile, M_{P2} is turned off and M_{N2} is turned on. Therefore, the boosted signal at N_N passes through M_{N1} to N_B to drive $M_{\rm PD}$ in order to pull up the capacitive load C_L. At this moment, M_{P1} is turned on to precharge N_P to V_{DD} (0.2 V). However, M_{N1} is turned on reversely causing the reverse current flow to charge N_N. At the end of the period, while $V_{\rm in}$ is L, N_N still holds (-90 mV). When $V_{\rm in}$ goes from L to H, the operation is similar to $V_{\rm in}$ transiting from H to L. N_P is boosted above V_{DD} to 389 mV and discharged to 303 mV at the end of the period while $V_{\rm in}$ is H.

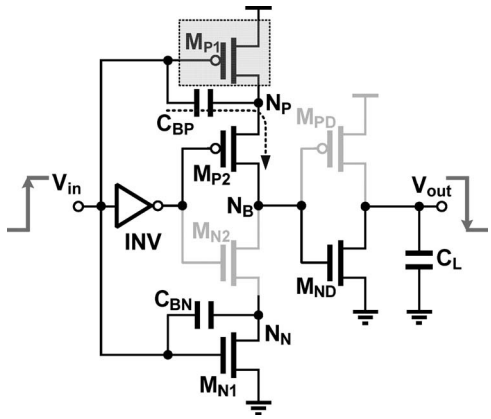

Fig. 4. Proposed bootstrapped inverter operations (input L to H).

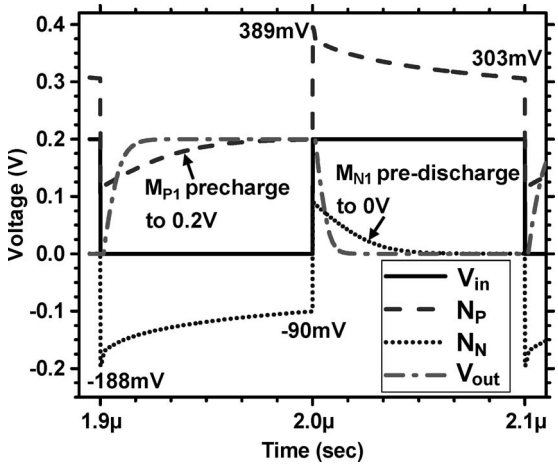

Fig. 5. Simulated timing waveforms at 5 MHz at 200-mV V_{DD}.

III. Detail Evaluation and Discussion

The proposed bootstrapped CMOS inverter is superior to previous designs in terms of leakage power and switching speed. In a low-voltage circuit design, decreasing the $I_{\rm on}/I_{\rm off}$ ratio degrades the noise margin. In the proposed design, the boosted voltage is used in both driving and cutoff phases. Additionally, the proposed design improves the $I_{\rm on}/I_{\rm off}$ ratio by using the active bootstrapped leakage reduction method. Moreover, fewer design components increase the speed of the bootstrapped

TABLE I
DEVICE SIZING

Driver topology	Sub-circuit	NMOS W/L (nm/nm)	m_n	PMOS W/L (nm/nm)	m_p
Conventional INV	inverter	420 / 80	30	440 / 80	30
Proposed Bootstrapped inverter	inverter	400 / 80	4	200 / 80	4
	M_{P1}, M_{N1}	200 / 80	1	200 / 80	1
	M_{P2}, M_{N2}	200 / 160	1	200 / 160	1
	driver	285 / 80	1	340 / 80	2
Bootstrapped driver [4]	inverter	400 / 80	4	200 / 80	4
	switch	200 / 80	3	200 / 80	3
	driver	250 / 80	1	340 / 80	2
Bootstrapped driver [6]	inverter	400 / 80	4	200 / 80	4
	switch	200 / 80	4	200 / 80	4
	driver	260 / 80	1	300 / 80	2

circuit. Owing to the fewer components operating in the subthreshold region, the proposed design scheme performs better than other previous works in terms of the Monte Carol analysis.

To compare the performances of the proposed scheme and the conventional ones more fairly, this work redesigned the conventional inverter and reported bootstrapped drivers by using the 90-nm process. The sizes of the conventional inverter and the bootstrapped driver are designed to obtain the same rise/fall transient output waveforms. Their device sizes are listed in Table I. A 30-fF boost capacitor is used to ensure that the boosting efficiency exceeds 80%. These features are evaluated in detail as follows.

A. Boosting Efficiency

The boosting efficiency is affected by the node parasitic capacitance [6]. Assume that $C_{\rm PT}$ is the total parasitic capacitance at the N_B node. Thus, voltage V_B for the boosting to $2V_{DD}$ is represented as

$$V_B \approx \frac{C_{\rm BP}}{C_{\rm BP}+C_{\rm PT}} \cdot 2V_{DD} \triangleq \beta \cdot 2V_{DD} \tag{1}$$

where β is defined as the boost efficient factor or the so-called boosting efficiency. The boosting efficiency is heavily dependent on the total parasitic capacitance. In order to obtain the boosting efficiency, the boost capacitance must be designed significantly larger than the node parasitic capacitance.

B. Reduction of the Leakage Current

In the proposed design scheme, the boosted high $(2V_{DD})$ at N_B enhances the driving capability of $M_{\rm ND}$ and suppresses the leakage current of $M_{\rm PD}$. Similarly, the boosted low $(-V_{DD})$ at N_B enhances the driving of $M_{\rm PD}$ and reduces the leakage of $M_{\rm ND}$.

The $I_{\rm off}$ current is primarily formed by a subthreshold leakage current [9], [10]. Hence, scaling the supply voltage lowers the $I_{\rm on}/I_{\rm off}$ ratio. In the previous literature, bootstrapped drivers improve the $I_{\rm on}/I_{\rm off}$ ratio only by enhancing $I_{\rm on}$ unidirectionally. The proposed design effectively suppresses the leakage current of PMOS (NMOS) by providing a potential of $-V_{DD}$ to V_{SG} (V_{GS}). According to the I–V formula in the subthreshold region, our design reduces the leakage current exponentially.

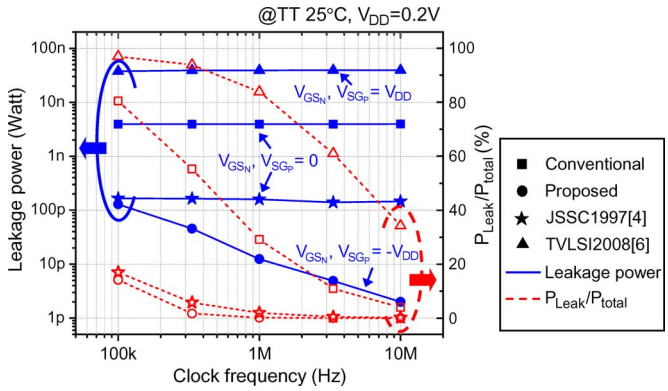

Fig. 6. Leakage power as a function of frequency from 10 MHz to 100 kHz.

The leakage power of a periodic waveform can be estimated by separating it from the average total power. The total energy E_T of a period of T is

$$\begin{aligned} E_T &= P_T \cdot T \approx (P_{\rm SW}+P_{\rm SC}+P_{\rm Leakage}) \cdot T \\ &= E_{\rm SW}+E_{\rm SC}+P_{\rm Leakage} \cdot T \end{aligned} \tag{2}$$

where P_T is the averaged total power, $P_{\rm SW}$ denotes the switching power, $P_{\rm SC}$ is to the short-circuit power, and $P_{\rm Leakage}$ is the leakage power. The switching energy, the short-circuit energy, and the leakage current are assumed to remain constant under the same power supply. Consequently, the leakage power with two signals can be obtained by test signals with periods T_1 and T_2, i.e.,

$$P_{\rm Leakage} = \frac{P_{T1} \cdot T_1 - P_{T2} \cdot T_2}{(T_1 - T_2)}. \tag{3}$$

Fig. 6 shows the comparison results for the leakage power as a function of frequency with a 0.2-pF capacitive load at 200 mV V_{DD}. The ratio of the leakage power to the total power is also shown in Fig. 6. Owing to the negative V_{GS} control, the leakage power at 10 MHz under 0.2 V of the proposed bootstrapped inverter is 2 pW. The leakage power is 3.9 nW for a conventional inverter, 0.15 nW for [4], and 39 nW for [6]. Although the PMOS (NMOS) transistor is turned off with the positive voltage V_{SG} $(V_{GS}) = V_{DD}$ in [6], the leakage power in [6] is more than three orders higher than that in the proposed design scheme. When the operating frequency goes from 10 MHz to 100 kHz, the potential of the boost node becomes lower due to the node leakage that degrades the leakage performance. The potential of the boost node even returns to V_{DD} or 0 at 100 kHz. Hence, we can find out that the leakage power is very close to the design in [4] obviously.

C. Delay Time Analysis

Delay time is another important feature of bootstrapped circuits. Although the driving transistors operate in a triode region under the subthreshlod supply, other devices remain in the subthreshlod region. The total delay time is thus the sum

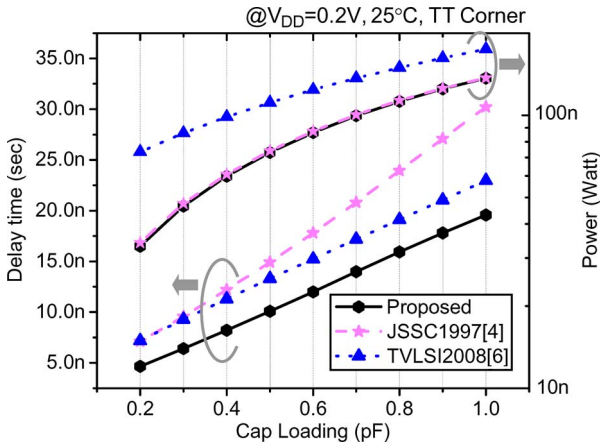

Fig. 7. Delay time and power consumption versus capacitive loads at 10 MHz.

of the propagation delay of the INV and the driver, which is denoted as

$$t_{P,\mathrm{BI}} = t_{P,\mathrm{INV}} + t_{P,\mathrm{Driver}} \tag{4}$$

where $t_{P,\mathrm{BI}}$, $t_{P,\mathrm{INV}}$, and $t_{P,\mathrm{Driver}}$ are the delays of the bootstrapped inverter, the INV, and the driver, respectively.

Assume that the boost efficiency is the same for all bootstrapped drivers. The delay time of the INV becomes a dominant factor. The subthreshold logic delay is derived in [9] as

$$t_P = \frac{k_f \cdot C_L \cdot V_{DD}}{\mu C_{\mathrm{dep}} \frac{W}{L} V_T^2 \exp\left(\frac{V_{DD}-V_{\mathrm{th}}}{nV_T}\right)} \tag{5}$$

where k_f is a fitting parameter. However, the circuit delay time is related to the RC loading effects. The proposed bootstrapped inverter has the shortest delay time among the other bootstrapped circuits since the loading of INV is only the gate capacitance of M_{N2} and M_{P2}.

Fig. 7 summarizes the comparison results for the delay time (from H to L) and the power consumption as a function of C_L at 10 MHz with a supply of 200 mV. The proposed design is the lowest in power consumption and delay time.

D. Delay Time Analysis of Process Variation

Subthreshold operation limits the yield due to its serious process variations. Although the boosted control signal pushes the driver transistors into the triode region, the residue circuit devices still incur the same serious problems with the variation. With fewer devices in the subthreshold region, the proposed design is less affected by the process variation.

The delay time variability analysis is performed based on Monte Carlo simulations. Device mismatch, threshold voltage V_{th}, and process corner variation are assumed to be Gaussian random distribution. In order to cover the most critical process and temperature corners, Monte Carlo simulations are under 3σ process variation at 25 °C, 125 °C, and -40 °C, which are shown in Fig. 8. The supply voltage is 200 mV, and the clock rate is 1 MHz. The number of samples for each temperature corner is 1500, and the total number of samples is 4500. For the worst case at -40 °C, a conventional inverter has an average

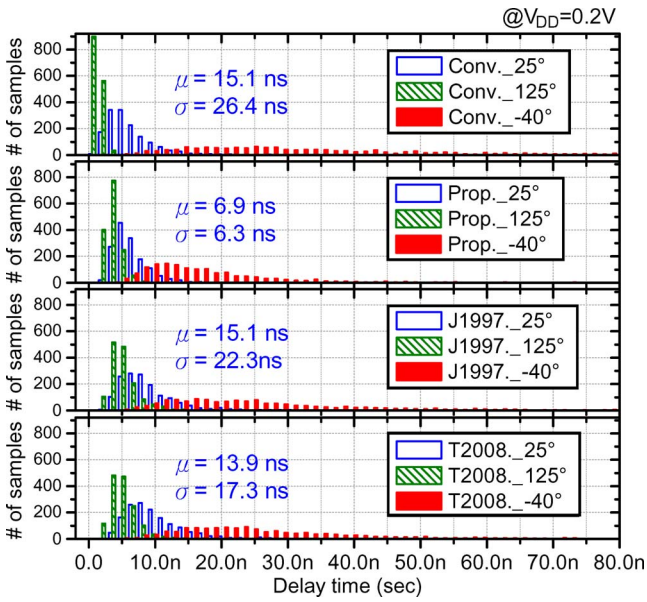

Fig. 8. Monte Carlo simulation results under a power supply of 200 mV.

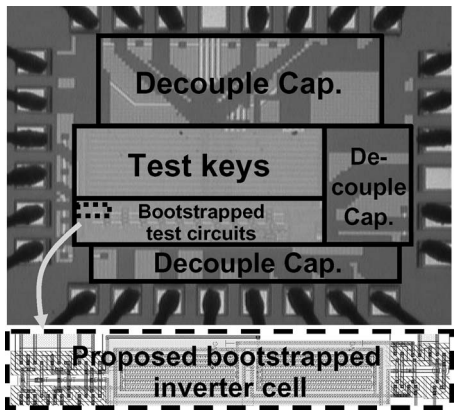

Fig. 9. Die photograph and cell layout.

delay of 15.1 ns, and the standard deviation is 26.4 ns. The proposed design does not only reduce the average delay to 6.9 ns but also the standard deviation to 6.3 ns, which is much better than [4] and [6]. Obviously, our design has higher immunity to the process and temperature variations.

IV. Implementation and Measurement Results

A test chip of bootstrapped CMOS inverters is implemented in 90-nm 1P9M SPRVT process to demonstrate the effectiveness of the proposed design scheme. The test circuits include the reported bootstrapped circuits of [4], [6], and the proposed design. The circuits also contain test keys to verify the interconnection model. Each bootstrapped circuit is implemented as a ten-stage cascade driver chain. In each stage, two 30-fF metal–oxide–metal (MOM) capacitors serve as bootstrap capacitors, and a 200-fF MOM capacitor serves as C_L. Level shifters are used to boost the 200-mV internal signal to the 500-mV chip input/output (I/O) signal for the measurement. The total area is 958 μm $\times$ 776 μm, and the core area is 566 μm $\times$ 102 μm. Fig. 9 shows the die photograph. The layout area of the proposed bootstrapped inverter cell is 25.8 μm $\times$ 4.1 μm.

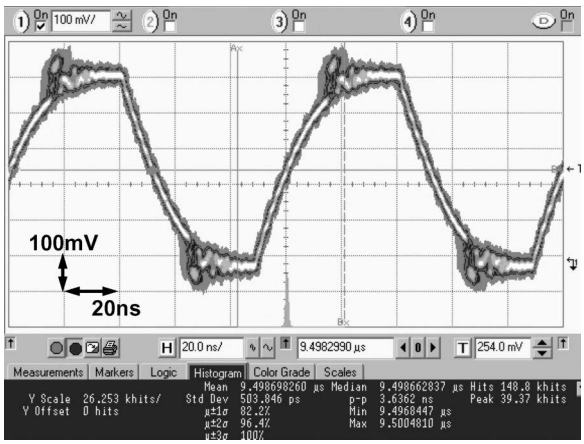

Fig. 10. Measured waveform at 200-mV core V_{DD} (500-mV I/O V_{DD}).

TABLE II
CHIP SUMMARY

Item	Specification (unit)			
Process	90nm SPRVT Low-K CMOS Process			
Supply Voltage	Bootstrapped Circuits		0.2V	
	Level Shift Buffer		0.2V, 0.5V	
	Digital Circuits		0.5V	
Power Dissipation @ 10 MHz (10 stages)	Leakage Power		Total Power	
	Post-sim (FF Corner)	Measured	Post-sim (FF Corner)	Measured
	133nW	107nW	1.13uW	1.01uW
Layout Area	Interconnect Test Circuits		575μm×307μm	
	Bootstrapped Circuits		566μm×102μm	
	Whole Chip		958μm×776μm	

TABLE III
COMPARISONS

	JSSC1997 [4]	T.VLSI2008 [6]	Proposed
Supply voltage (V)	0.2	0.2	0.2
Max frequency (MHz)	4	5	10
Delay time (us)	47.3	48.2	30.1
Total Power (uW)	0.74	1.71	1.01
Leakage Power (nW)	276	833	107
Energy per cycle (pJ)	0.19	0.34	0.10

Fig. 10 shows the measured waveform. The cumulative clock peak-to-peak and root-mean-square jitters are 3.6 ns and 504 ps, respectively. The measured average total power is 1.01 uW. With the leakage power estimated in (3), the derived leakage power is 107 nW with the periods of 100 and 105 ns. Table II lists the summary of the chip. Table III lists the comparisons of measured results with other works at 0.2-V V_{DD}. For a ten-stage driver chain operating at 10 MHz, the proposed design has a delay time of 30.1 us, the energy efficiency is 0.1 pJ/cycle, and the leakage power is 107 nW, which is the best, as compared with [4] and [6].

V. CONCLUSION

This brief has described a subthreshold-supply bootstrapped CMOS inverter with an active leakage current reduction technique. Based on 4500 times of Monte Carlo simulations, the average delay time of the proposed design with 200-fF C_L is 6.9 ns with a standard deviation of 6.3 ns, which achieves a reduction of 76% from the conventional inverter. Measured results verify that the test chip can achieve a clock rate of 10 MHz at 200 mV V_{DD}. Due to the negative V_{GS} suppression, the measured leakage power is more than 50% improvement over the previously reported bootstrapped drivers. The power consumption is 1.01 μW, and the leakage power is 107 nW, and the energy efficiency is 0.1 pJ/cycle.

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