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# Quantitative Discussion on Electron-hole Universal Tunnel Mass in Ultrathin Dielectric of Oxide and Oxide-Nitride

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MOS and MIS capacitor has been extensively studied in past several decades by many authors. It has been expected to reveal how basic physics relate electron device operation. In this structure, several physical phenomena co-work and then exhibit the electrical properties measured in IV- and CV-characteristics. On the other hand, the conventional models were established separately for the inversion layer (positive gate voltage), the depletion region (negative-low gate voltage), and the accumulation region (negative-high gate voltage). In addition, actual MOS/MIS samples have interfacial transition layer where physical properties are gradually changed from Si to oxide or other dielectric, the varying composition ratio of molecules and local traps owing to atomistic dangling bonds through dielectric layer. ***What will happen if we self-consistently unify all the physical models that are separately developed?***

## Introduction

In electron devices engineering, the device dimension is shrunk according to Moore's law [1] and the scaling rule [2], and then the thickness of gate dielectric layers fabricated on the silicon surface is thinned annually. Accordingly, the device modeling is made complicated by the interface factors that become notable with the scaling. The interface factors are composed of trap-induced issues or some inconsistency in lattice and contaminations at the interface, and the intrinsic issues that are independent of the traps and the lattice inconsistency. However, it can be regarded that the extrinsic issues, which is from traps, lattice-inconsistency and contaminations, can also exist inside the gate dielectric layers, apart from the interface. It is thereby indispensable to distinguish the intrinsic and extrinsic factors firstly. Here note that the intrinsic interface factor must become notable as the gate dielectric thickness is decreased. This, as a result, relatively enhances the influence of interface physics between the dielectrics and the silicon surface on the property of gate dielectrics [3]-[16]. It is accordingly convenient to carefully study the thickness dependence of physical and electrical properties of gate capacitor samples from which the extrinsic factors have been removed appropriately. MOS capacitor is a first preferable sample. The interface physics made notable by the scaling must be self-consistently involved in the device modeling. Provided that the unified modeling of interface physics and device modeling is succeeded, we must be able to reproduce the measured curves of both CV- and JV-characteristics in both polarity of gate voltage, irrespectively of oxide thickness.

In this paper, firstly, we will validate the intrinsic interface modeling with five samples of MOS capacitor with different gate oxide thicknesses. Subsequently, for the modeling of the extrinsic factor inside the gate dielectric, experimental and analyzing technique of molecular composition of dielectric film will be carefully discussed.

## Intrinsic factor at the interface

Let us regard that MOS capacitor is an appropriate sample for investigating the intrinsic factor for interface physics, because the extrinsic factors have been extensively studied and removed as possible. Fig. 1 is the first evidence of our successful unification [15] in MOS capacitor. In this comparison, all fitting parameter we used is the tunnel mass whose oxide thickness dependence is shown in Fig. 2. It sounds that the tunnel mass of electron is 0.85 $m_0$, where $m_0$ is the rest electron mass, and independent of oxide thickness within a reasonable error. If we ignore anyone of the co-working models, a discrepancy occurs between theory and measurements. Trying to compensate this discrepancy, the tunnel mass becomes dependent of oxide thickness, and is distorted with respect of the polarity of gate voltage.

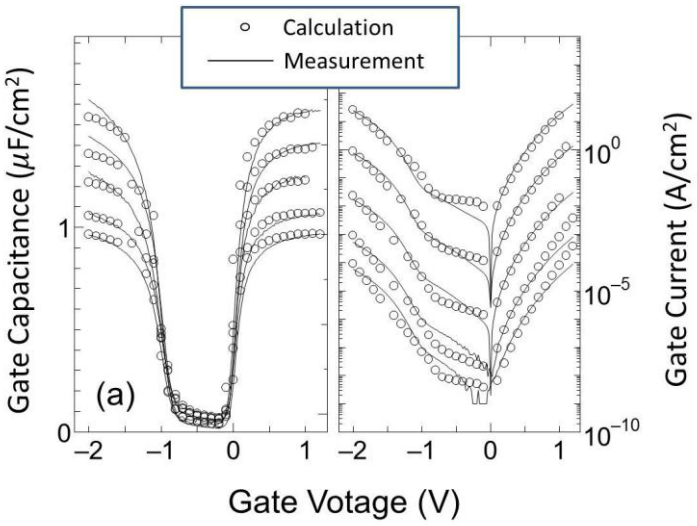


**Fig. 1**. Comparison of CV and JV curves using the unified model.

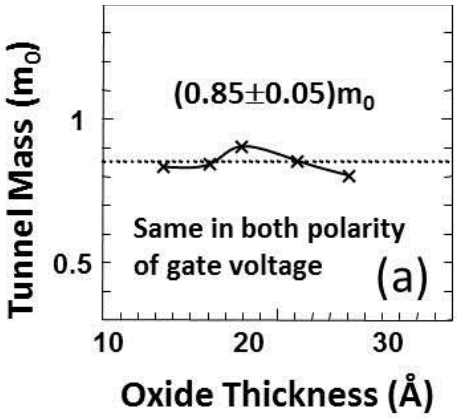


**Fig. 2**. Obtained tunnel mass using the unified model.

In Fig. 3, the options considered in the implementation of models for interfacial transition (IFT) layers and their corresponding equivalent circuits: (b) and (c) show the cases of removing the IFT layers from the poly-Si side and from both sides, respectively. In the upper line, are shown the corresponding equivalent circuits composed of capacitance of Si surface, of IFT layers, of pure oxide ($SiO_2$), and of poly-Si bottom. The IFT layers are considered in both of interfaces with Si substrate and with gate poly-Si, whose widths are four angstroms. The band gap (EG) of $SiO_2$ is assumed to be 8.95 eV from [17], while that of Si is 1.12 eV. Since the valence band affinity (VBA) is 4.49 eV from [18], the tunnel barrier (discontinuity of conduction band edges) is 3.34 eV. The oxide thickness ($T_{OX}$) is defined as the distance between the centers of the IFT layers. In other words, the interfaces are the centers of IFT layers, provided that the IFT layers have finite width. The dielectric constant (K) is 11.7 and 3.9 in Si and $SiO_2$, respectively. Here note that the conduction band edge, the valence band edge, and K are linearly changed within IFT layers from those values of pure Si to $SiO_2$ (**linear approximation**).

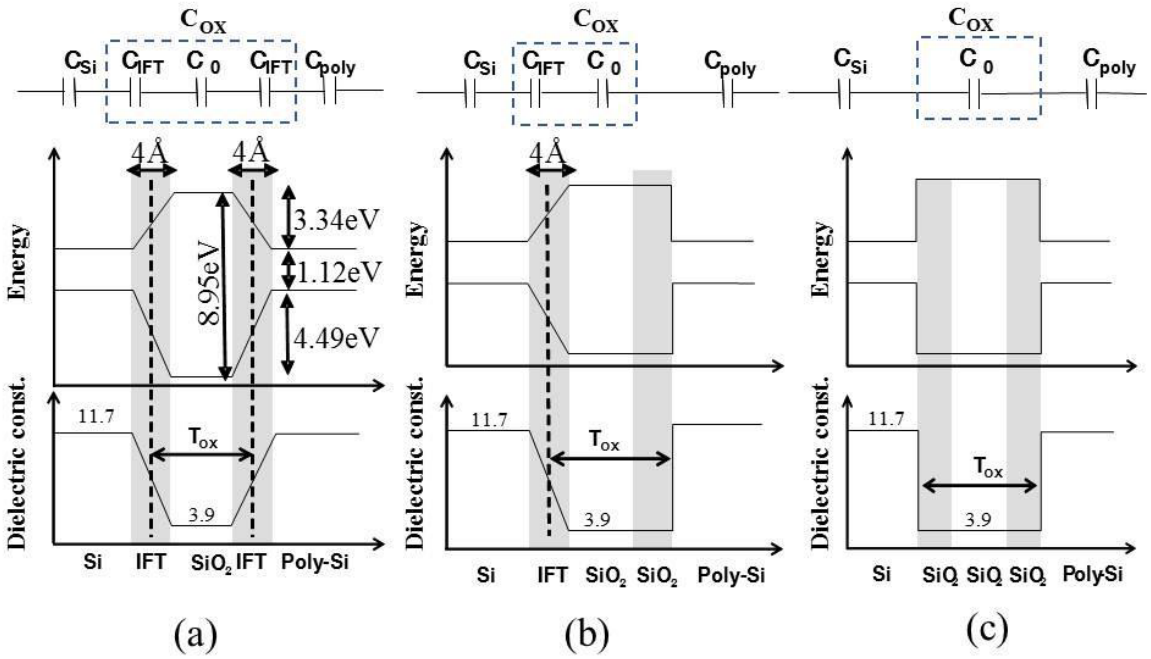


**Fig. 3**. Options considered in the implementation of models for IFT layers and their corresponding equivalent circuits.

CV-JV fitting

In option (a), we have adjusted $T_{OX}$ to fit the calculated CV-curves with the measured ones in a set of five samples (Sample No. 1, 2, …, 5) of MOS capacitar. Subsequently, we have adjusted the tunnel mass to fit the calculated JV-curves with the measured ones using the $T_{OX}$ calibrated in the CV-fitting in a set of five samples of MOS capacitor. As shown in Fig. 1, we have successfully reproduced the measured curves of both CV- and JV-characteristics in both polarity of gate voltage, irrespectively of oxide thickness. As shown in Fig. 2, the obtained tunnel mass is around 0.85 $m_0$ without $T_{OX}$-dependency. The $T_{OX}$ calibrated in the CV-fitting and used in the JV-fitting is plotted by diamond in Fig. 4. In ref. [15], it is reported that these $T_{OX}$ are consistent with measured by the

elipsometry method. It might appear that the elipsometry measures the thickness of pure oxide without the IFT layers.

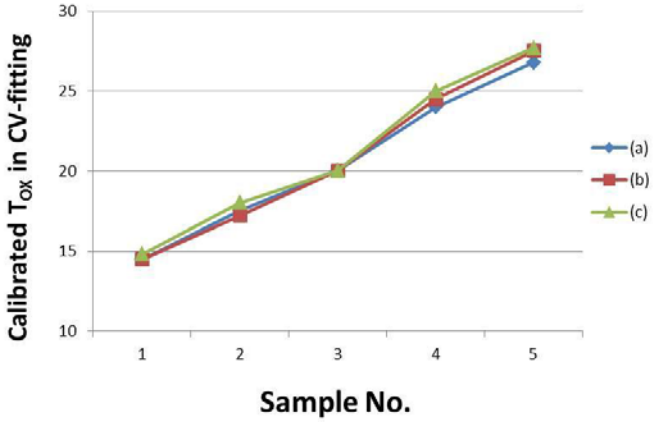


**Fig. 4**. $T_{OX}$ calibrated via CV-fitting and used in JV-fitting.

In option (b), the IFT layer is removed from the gate poly-Si interface, and the $T_{OX}$ is defined as the distance between the center of the Si IFT layer and the interface with poly-Si. We perform the subsequent fitting procedures of CV and JV characteristics in a similar manner with the option (a). The calibrated $T_{OX}$ (plotted by squares) is consistent with the option (a), as shown in Figure 4, whereas a notable discrepancy in JV-curve appears in a negative gate bias region, as shown in Fig. 5. Here we have fitted the calculated JV-curves with the measured ones in the positive gate bias region. If we fit the calcuated JV-curves with the measured ones in the negative gate bias region, the discrepancy appears in the positive gate bias region. The option (b), thereby, cannot fit the JV-curves, while the CV-curve can be fitted with $T_{OX}$ consistent with the option (a). The tunnel mass obtained in a case that the JV-curves are fitted in the positive gate bias region is dipicted by crosses in Fig. 6. It appears that this shows no $T_{OX}$-dependent tunnel mass in the positive gate bias case, around 0.59 $m_0$, whereas the negative gate bias case shows the $T_{OX}$-dependent tunnel mass appears, as depicted by squares in Fig. 6.

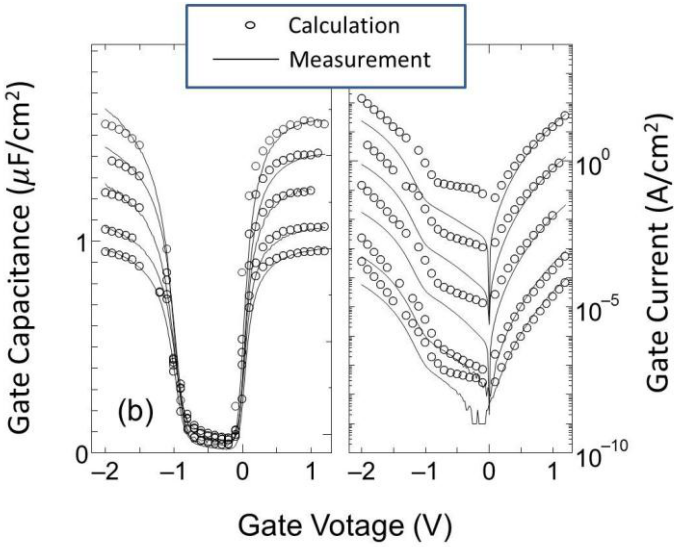


**Fig. 5**. Comparison of CV and JV curves in MOS capacitor in option (b).

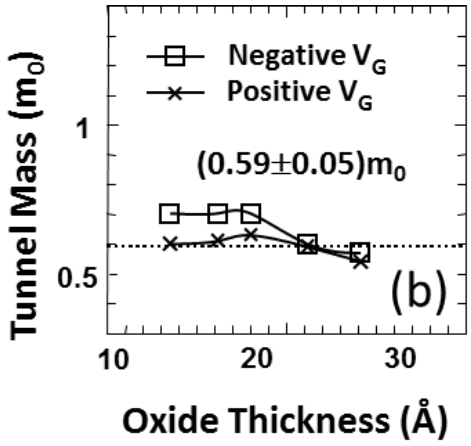


**Fig. 6**. Obtained tunnel mass in option (b).

In option (c), both IFT layers are removed, and the $T_{OX}$ is defined as the distance between the abrupt interfaces. We perform the subsequent fitting procedures of CV and JV characteristics in a similar manner with the option (a). The calibrated $T_{OX}$ (depicted by triangles) is consistent with the option (a), as shown in Fig. 4, whereas a notable discrepancy in JV-curve appears in a negative gate bias region, as shown in Fig. 7. Here we have fitted the calculated JV-curves with the measured ones in the positive gate bias region. If we fit the calcuated JV-curves with the measured ones in the negative gate bias region, the discrepancy appears in the positive gate bias region. The option (c), thereby, cannot fit the JV-curves, while the CV-curve can be fitted with $T_{OX}$ consistent with the option (a). The tunnel mass obtained in a case that the JV-curves are fitted in the positive gate bias region is dipicted by crosses in Fig. 8. It appears that this shows no $T_{OX}$-dependent tunnel mass in the positive gate bias case, around 0.49 $m_0$, whereas the negative gate bias case shows that $T_{OX}$-dependent tunnel mass appears, as dipicted by squares inFig. 8.

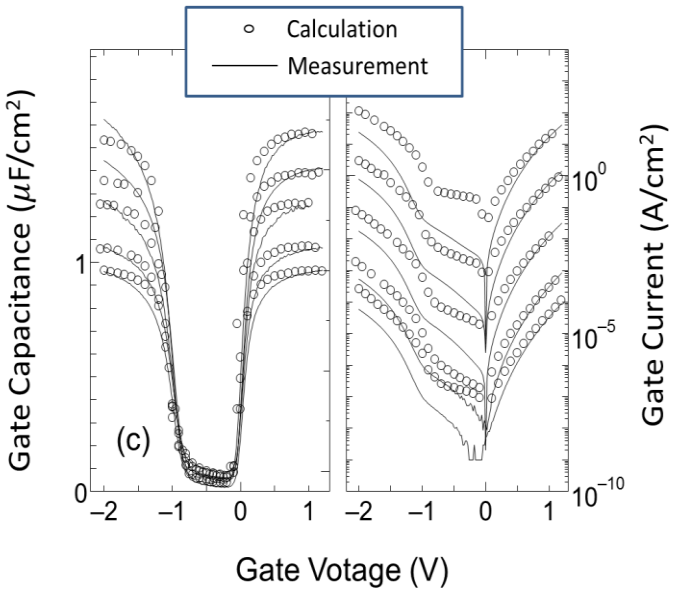


**Fig. 7**. Comparison of CV and JV curves in MOS capacitor in option (c).

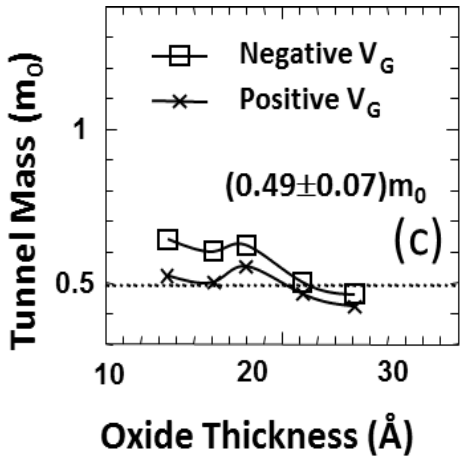


**Fig. 8**. Obtained tunnel mass in option (c).

The $T_{OX}$-dependent tunnel mass is not only unphysical, but also inconvenient to the device modeling. Among these options, it can be regarded the option (a) as closest to the actual profile of K and EG within a zero-th order approximation. We will assume the option (a) below in this paper, that is, the linear approximation.

## An extrinsic factor inside gate dielectric

As mentioned above, we have appropriately modeled the IFT layers, i.e., the intrinsic factor, which removes the $T_{OX}$-dependency from the calibrated tunnel mass. To carefully study the impact of extrinsic factors inside the gate dielectric, we need to control the issue of the inconsistency in lattice and traps. Firstly, we should remove the extrinsic issues from the interfaces. Second, we should measure the profile of extrinsic issues of sample capacitors that we will measure. Third, we should remove the issues related to contamination as possible as we can, because it is hard to control it in the fabrication process. If not, we need to know which contamination will enter into the dielectric film and its amount. Fourth, we should determine the issue of extrinsic factors. Fortunately, it is possible to fabricate an appropriate sample capacitor for this aim, that is, ultra-thin gate SiON [19]. It is reported in [20] that the hysteresis of the CV measurements shows less than 5mV flat-band potential shift. This means no evidence for slow state. Let us regard this as satisfying the first requirement, i.e., to remove the extrinsic issues from the interfaces.

Next, as shown in Figure 9, the profiles of the nitride atom concentration, [N], and the oxide atom concentration, [O], are measured by the angle-resolved X-ray photoelectron spectroscopy (AR-XPS) method [21]. The pure oxide ($SiO_2$) was made at the dielectric surface and may then absorb the boron atoms if the film is covered by the gate polysilicon where the boron atoms are doped. This means that we can regard no contamination in $n^+$ poly-Si gate, whereas we need to consider the influence of boron contamination from $p^+$ poly-Si gate. The shaded layers at the surface and the $Si/SiO_2$ interface depict the IFT layers, where EG and K are assumed to be linearly changed from the values of Si to those of $SiO_2$ [15]. Finally, we assume that the major extrinsic issue inside this film is dangling-bond of atomistic network composed of Si, N, and O atoms.

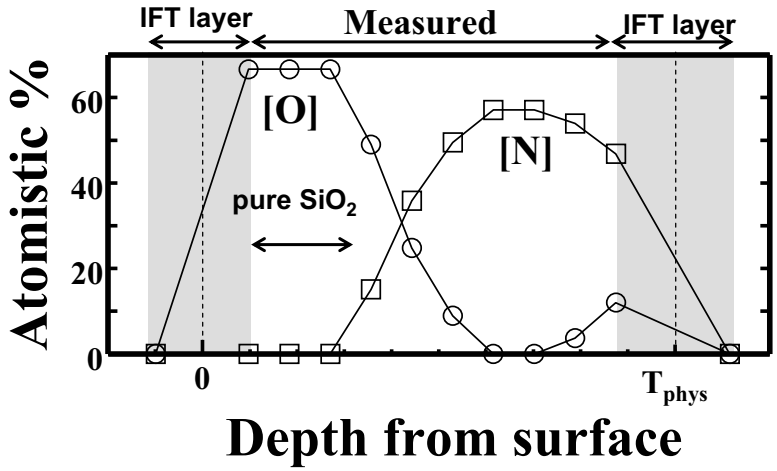


**Fig. 9**. Measured profile of [O] and [N].

Alloy Model for ultra-thin gate SiON film with IFT layers

The SiON film considered here basically stays on the tie-line of $(SiO_2)_{1-x}(Si_3N_4)_x$. The K on the tie-line is dependent of Si-N bond rate (R) but not of the molecular compound ratio (x) [22], [23]. An excellent agreement is thereby achieved between the calculated and measured values of K in the literature [23]-[25]. We, a priori, regard this property as valid in the following quantities, e.g., EG, K, VBA, the tunnel masses of electrons and holes ($m_e$ and $m_h$, respectively), and the IFT-layer width ($W_{IFT}$). They are accordingly assumed to satisfy the tie-line law:

$$Q = (1 - R)Q_{OX} + RQ_{SiN} \tag{1}$$

$$R = \frac{3x}{1+2x}, \quad x = \frac{0.75[N]}{1-[N]} \tag{2}$$

with Q being K, EG, VBA, $m_e$, $m_h$, and $W_{IFT}$ on the tie-line, $Q_{OX}$ being those at x=0, and $Q_{SiN}$ being those at x=1. These quantities can be estimated on the tie-line according to Table I with [N] shown inFig. 9.

**TABLE I.** Material Variable: (*) Present results.

| Variables | $SiO_2$ | $Si_3N_4$ | Si |
|---|---|---|---|
| K | 3.9 | 7.5 | 11.7 |
| EG (eV) | 8.95 | 5.4 | 1.12 |
| VBA (eV) | 4.49 | 1.9 | - |
| $m_e$ (m0) | 0.85 | 0.85* | - |
| $m_h$ (m0) | 0.85* | 0.85* | - |
| $W_{IFT}$ (nm) | 0.4 | 0.5 | - |

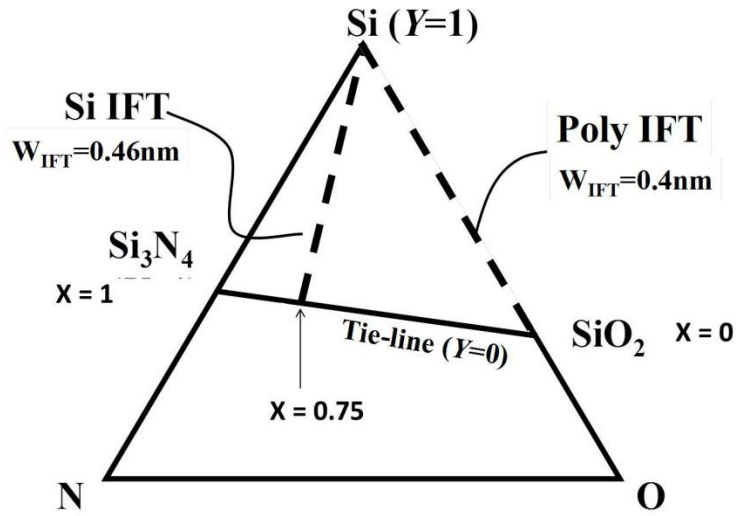


**Fig. 10**. Tie-line of SiON with IFT layers.

The IFT layers become notable as the gate dielectric film is thinned. Accordingly, we should take into account IFT layers assuming the extension of alloy-model, i.e., $[(SiO_2)_{1-x}(Si_3N_4)_x]_{1-y}Si_y$. As shown in Fig. 10, we have the tie-line at y = 0 and Si irrespective of x at y = 1. The IFT layers belong to the broken lines with $0 < x < 1$. The physical thickness of this film ($T_{phys}$) is regarded as the distance between the centers of the IFT layers in a similar manner with gate oxide. In this work, we prepared four samples of $T_{phys}$ = 1.1 nm and 1.3 nm each having $n^+$ poly gate and $p^+$ poly gate. The $W_{IFT}$ at the surface is therefore regarded as 0.4 nm (pure oxide value) from Table I, whereas that at the interface is found to be 0.485 nm using the tie-line law mentioned above since the measured profile of [N] is 46% (R = 0.85) at the interface. In Fig. 11, we show the profiles of x and R that are calculated by substituting the profile of [N] shown in Fig. 9 to (2). The calculated profile of R is more rounded than that of x and no Si-N atomistic bonds exist at the surface, i.e., R = 0, whereas they exist at the interface (R = 0.85). In Fig. 12, we show the profiles of K and EG that are calculated by using the profile of R shown in Figure 11 according to (1). The K is decreased as EG is increased. The profile of VBA is also calculated in a similar way and shown in Fig. 13. The VBA is changed with Eg, but not with K, as expected.

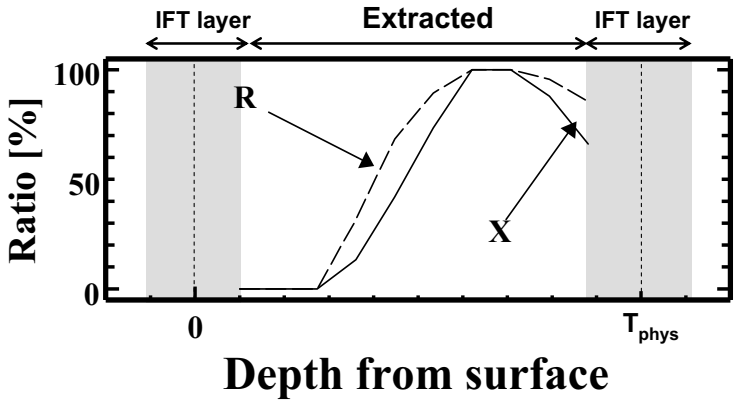


**Fig. 11**. Extracted profiles of x and R.

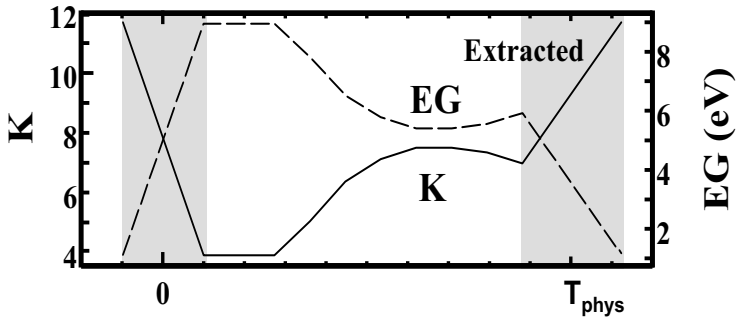


**Fig. 12**. Extracted profiles of EG and K in SiON.

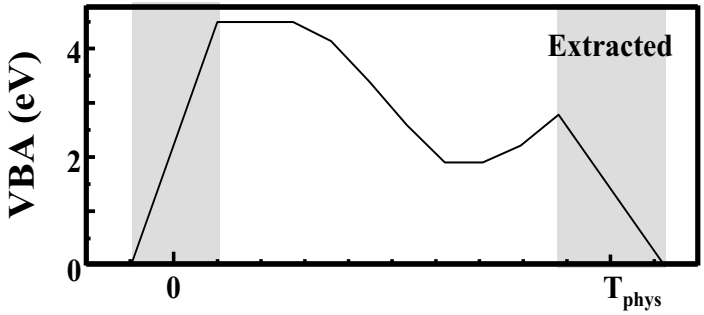


**Fig. 13**. Extracted profile of VBA.

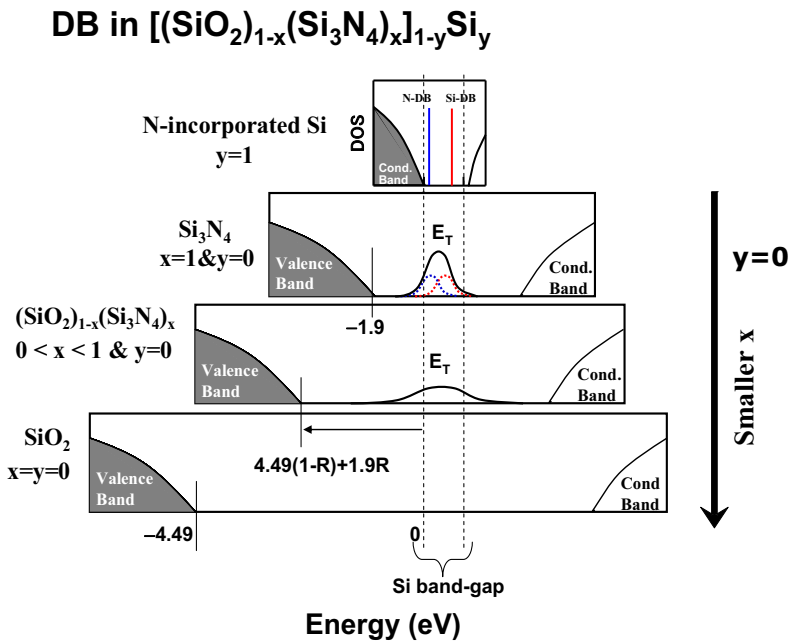


**Fig. 14**. Illustration for traps owing to dangling bond in SiON.

CV-fitting with Charge Trapping Model

Let us consider the breaking of Si-N atomistic bond in N-incorporated Si crystal. It is considered that we have two types of dangling bond, i.e., N-DB and Si-DB, as shown at the top line in Fig. 14 [26]. In the first step, the band structure is extended from N-incorporated Si-crystal (y=1) to $Si_3N_4$ (x=1 and y=0), in which EG is increased by nearly 5 times (according to the ratio of EG, 5.4/1.12) and the two sharp peaks due to N-DB and Si-DB become broader in proportion to the spread of EG, as shown at the second line. We can thereby consider that these peaks make a combined broader peak, the center of which is the trap level ($E_T$). According to [27], $E_T$ is the level 0.4eV lower than the Si mid-gap with the half-value width being 0.1eV. On the other hand, let us regard the peak height in the distribution as proportional to the profile of R, that is, the number of Si-N atomistic bonds. Since the half-value width of the distribution is also extended as EG is increased according to $\Delta E_T = 0.1eV \times EG / 1.12eV$, that is, 0.5eV in $Si_3N_4$ (x = 1 and y = 0). Next, the film is changed from $Si_3N_4$ (x = 1) to SiON (x < 1) at the third line. As EG and VBA are increased according to the tie-line law mentioned above, the combined peak is further broadened and lowered. The height of the peak is proportional to the trap density. At the last line, the film merges to pure oxide with no traps as the limit of the trap peak height disappears.

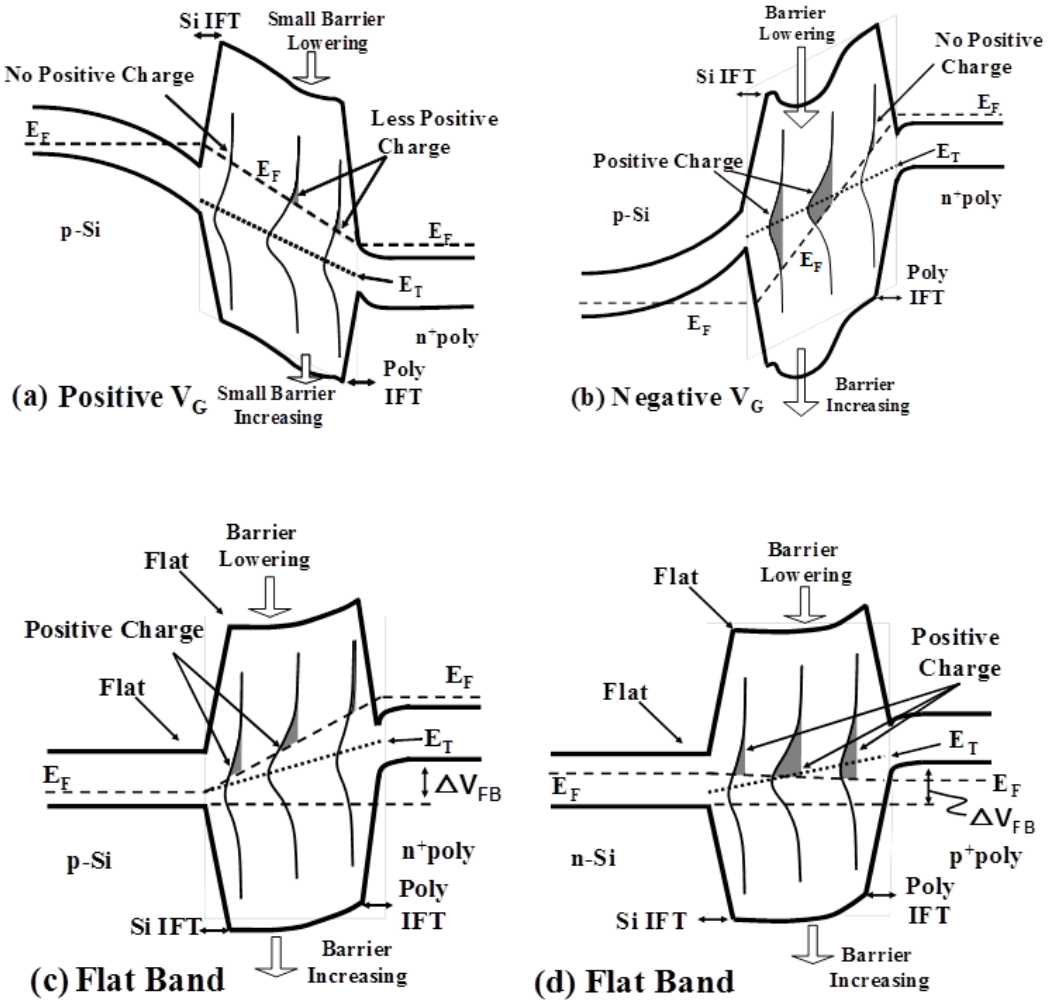


**Fig. 15**. Illustrations for trapped positive charge. The nMOS case is dealt with in (a) to (c), and the PMOS case corresponds to (d).

We can thus consider that the upper tail of the combined peak above the Fermi level ($E_F$) contributes to the positive charge, as shown in Fig. 15. The lines of $E_T$ and $E_F$ inside SiON film are represented by straight lines. The relation between $E_T$ and $E_F$ are dependent of bias condition, which affects the profile of charge and barrier modulation. From (a)-(c), we illustrate the band structure of an nMOS at a positive gate voltage ($V_G$), at a negative $V_G$, where the absolute value of $V_G$ is larger than that of flat-band potential ($V_{FB}$), and at the flat-band, respectively. Here note that the flat-band means no electric field at the Si interface, while the electric field at the gate polysilicon ($n^+$ poly) interface and the amount of trapped charges are cancelled, as illustrated in (c). In these figures, we assumed the Si-N atomistic bond profile has a peak inside the film. In (a), since $E_F$ is made higher than $E_T$ by the band bending of inversion layer at the substrate surface, we have less amount of the positive charges, which is in proportion to that of the dangling bonds with $E_T > E_F$. This positive charge lowers the barrier height for tunneling electron and increases that for tunneling holes slightly at the $n^+$ poly side. In (b), since $E_F$ is made much lower than $E_T$ by the depletion layer at the substrate surface, we have a much greater amount of positive charge inside the film. This lowers the tunnel barrier for electrons and increases that for holes much more. In (c), $E_F$ is still so high at the $n^+$ poly side that the positive charge lowers the tunnel barrier for electrons and increases that for holes, and negates the electric field at the interface with $n^+$ poly to make the flat-band at the Si interface. In (d), we illustrate the band structure of pMOS at the flat-band, where we have a greater amount of positive charge compared with nMOS at the side of gate polysilicon ($p^+$ poly), since $E_F$ there is much lower in pMOS than in nMOS. The positive charge lowers the tunnel barrier for electrons and increases that for holes much more than in nMOS.

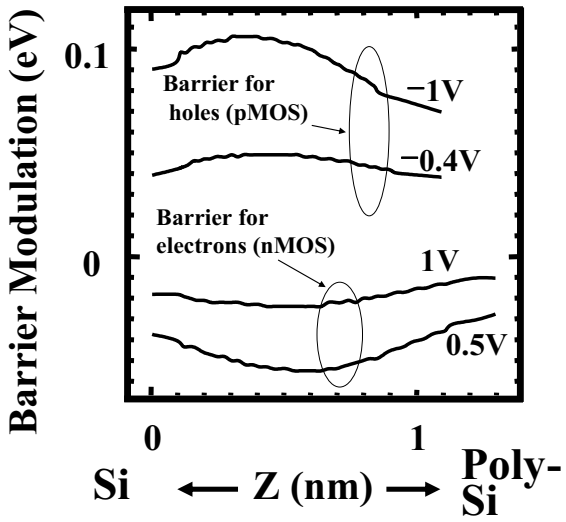


**Fig. 16**. Calculated barrier modulation due to the trapped positive charge.

The calculated barrier modulation is shown in Fig. 16. This clearly shows that the barrier modulation is more notable in negatively-biased pMOS than in positively-biased nMOS. The positive charge stored by dangling bonds is, in this way, dependent of the electric field that determines $E_T$ - $E_F$ inside the SiON film, which has a notable influence on the gate current through the SiON film, as discussed below.

It is noteworthy that the precise calculation of $E_F$ is indispensable for estimating the amount of the positive charge, which is described in detail in [28], [29]. In addition, $E_F$ has a significant influence on the estimation of the incomplete depletion layer [30] and

the weak accumulation layer [31] at the interface with the gate polysilicon. The subband at the Si interface is calculated by the real-space transfer matrix method [32]. The IFT layers are self-consistently implemented with these detailed-advanced models [15].

Influence of boron-contamination on flat band potential

Dividing the film into the grids (i=1, 2…M), the Poisson equation is found to be

$$K_i \varepsilon_0 \frac{\Delta V_i}{\Delta T_i} = -q\Delta N_i \,, \tag{3}$$

where $\varepsilon_0$ is the vacuum permittivity, q is the elementary charge, and $\Delta T_i$ is the width of i-th grid layer. The $\Delta N_i$ and $\Delta V_i$ are the local amount of charges divided by q in the i-th grid layer and the potential drop across the i-th grid layer related to $\Delta N_i$, respectively. The $K_i$ is the dielectric constant of i-th grid layer. Integrating these grid layers, we have the flat-band shift,

$$\Delta V_{FB} = \sum \Delta V_i = -\frac{q}{\varepsilon_0 T_{phys}} \,, \tag{4}$$

where

$$\gamma = \frac{\sum \Delta N_i}{K_i M} \,. \tag{5}$$

In Fig. 17, it is found that the measured flat-band shift is clearly proportional to $\gamma T_{phys}$. The proportional coefficients are 0.7 MV/cm with the fit-variance being $3.1\times10^{-3}$ in nMOS and 1.4 MV/cm with the fit-variance being $7.8\times10^{-3}$ in pMOS. This means that $\Delta N_i$ in pMOS differs from that in nMOS. If the amount of positive charge was equivalent to the number of Si-N bonds, these amounts in nMOS and pMOS would be almost the same. However, the slope in pMOS is twice that in nMOS, as shown in Fig. 17. This may come from the boron-contamination, because p+ poly is fabricated on the oxide surface of the film in pMOS capacitor samples.

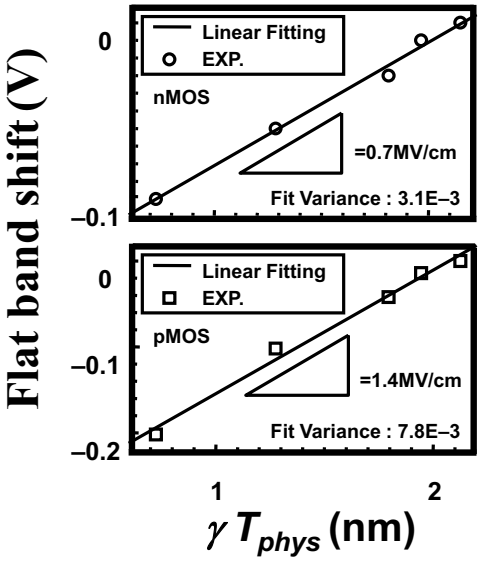


**Fig. 17**. Analysis of flat-band shift by linear fitting.

On the other hand, since all of the Si-N bonds cannot give the dangling bonds, we cannot directly extract $\Delta N_i$ from the measured profile of R. We should therefore carry out a careful study of the trap density ($N_T$) that is equal to $Y_{DB} \times R$, where $Y_{DB}$ is the dangling-bond (trap site) yield from Si-N atomistic bonds. In such a way, we self-consistently solve (3) considering $Y_{DB}$ as well as all the above-mentioned physical models [28]-[32], and can then obtain CV-characteristics. Fig. 18 is the test calculation of CV-characteristics of an nMOS capacitor. The flat-band potential is decreased as $Y_{DB}$ is increased, since the positive charge inside the gate dielectric SiON film is increased. The influences in inversion and accumulation layers are opposite.

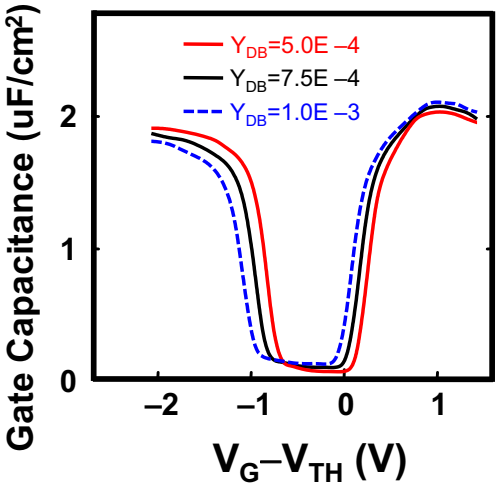


**Fig. 18**. Influence of $Y_{DB}$ on CV-characteristics.

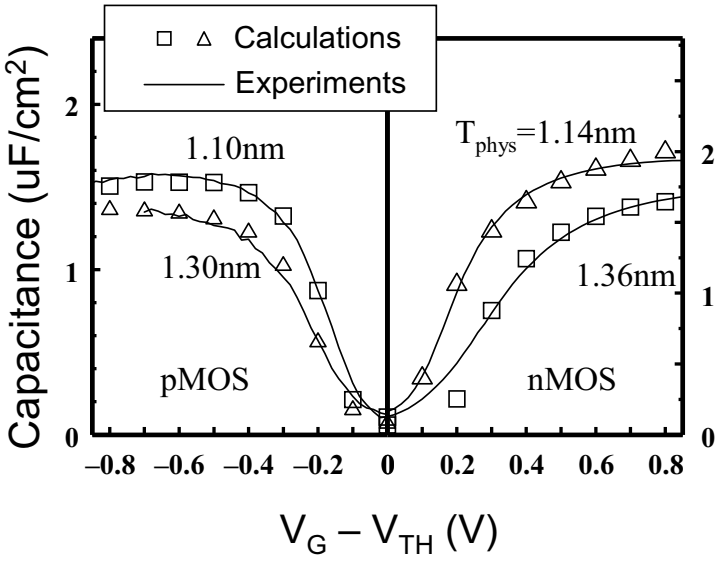


**Fig. 19**. Comparison of calculated and measured CV-characteristic.

As mentioned above, experimental and analyzing technique of molecular composition of dielectric film has been notably improved. Nowadays, we can measure the profile of Si-N atomistic bonding distribution (R) in ultrathin SiON dielectric film, as shown in Fig.

11. The energy band structure and the dielectric constant (K) are extracted according to the Si-N bonding profile, as shown in Fig. 12. The shaded regions are inserted as models for the IFT layers at polysilicon/dielectric and dielectric/Si in the unified modeling [16]. Provided that the SiON dielectric partially differs from the stoichiometric of $(SiO_2)_{1-x}$ $(Si_3N_4)_x$, some of Si-N bonds are broken; then leaving the dangling bonds in dielectric. Thus, $Y_{DB}$ (dangling bond number / Si-N bond number) can be regarded as the off-stoichiometric ratio. Using this $Y_{DB}$ as fitting parameter in the CV-fitting, the unified modeling can predict the CV-characteristics. As shown in Fig. 19, we have an excellent agreement between the measured CV characteristics and those calculated with the parameters summarized in Table II and the nitride profile measured by AR-XPS. It is found from the present analysis that 0.075% and 0.17±0.02% of Si-N bonds are broken to be dangling bonds in nMOS and pMOS, respectively. The extracted $Y_{DB}$ in pMOS is much larger than in nMOS, which corresponds to the slopes shown in Fig. 17. It appears that the boron atoms diffused from $p^+$ poly cause the extrinsic dangling bonds inside the SiON dielectric film, which may be associated with B-N-B bonds [33]. As shown in Fig. 9, we have pure $SiO_2$ at the poly-Si side, which degrades the barrier for boron penetration. The boron contamination can therefore penetrate from $p^+$ poly. In addition, the dangling bonds at the $p^+$ poly side contribute to more positive charges at the flat-band in pMOS, as illustrated in Fig. 15 (d). This extrinsic dangling bond causes the excess charge at the $p^+$ poly side, which results in an apparent increase of $Y_{DB}$. In other words, *$Y_{DB}$ can compensate the influence of boron contamination on the calibration of universal tunnel mass*.

**TABLE II.** Parameters used in the present analysis

| $Y_{DB}$ (%) | $T_{Phys}$ (nm) | $N_{poly}$ ($cm^{-3}$) | $N_{sub}$ ($cm^{-3}$) |
|---|---|---|---|
| 0.19 | 1.10 | $6\times10^{19}$ | $5\times10^{16}$ |
| 0.15 | 1.30 | $4\times10^{19}$ | $7\times10^{16}$ |
| 0.075 | 1.14 | $1\times10^{20}$ | $2.6\times10^{16}$ |
| 0.075 | 1.36 | $3\times10^{20}$ | $2.6\times10^{19}$ |

## JV-fitting composed of trap-assisted tunneling and direct tunneling

The comparison of the calculated CV-curves with the measured ones has determined $Y_{DB}$, as mentioned above. *Regarding the product of $Y_{DB}$ and R as the profile of local traps caused*, we can take into consideration the location effect of local traps causing the trap-assisted tunneling (TAT) through the SiON dielectric film. Before demonstrating this, let us extract the tunnel masses for electrons and holes from an individual experiment. We compare the calculated and measured gate currents of samples in which the profiles of nitride are uniform [21], taking into consideration the IFT layers. In Fig. 20, we plot the four graphs to depict the electron currents and hole ones at 5 MV/cm, which are normalized by the electron current at [N] = 0 %. In the top graph ($m_h$ / $m_e$ = 0.75/0.85), we have the off-set between the electron currents and the hole ones at [N] = 23%. Since the tunnel barrier for holes, i.e., VBA, is decreased with the increase of [N], this off-set is caused by the turnover of the hole current and the electron one. In the second graph ($m_h$ / $m_e$ = 0.85/0.85), we have the off-set at [N] = 31%, which is consistent with the experiment shown at the bottom graph. In the third graph ($m_h/m_e$ = 0.95/0.85), we have the off-set at [N] = 40%. It is therefore found that the tunnel masses for electrons and holes are the same, $0.85m_0$, in the SiON gate dielectric film.

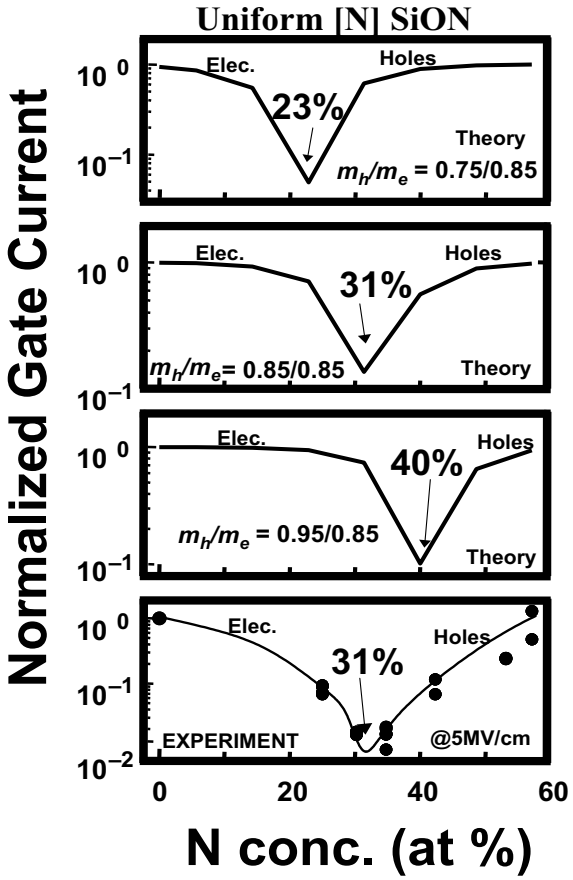


**Fig. 20**. Extraction of holes tunnel mass.

Since the TAT occurs when an electron scatters with a trap (dangling bond) having the scattering cross-section (σ), the total tunneling probability ($D_{TOT}$) is written by:

$$D_{TOT}(z,E) = \sigma Y_{DB} R(z) D_{TAT}(E) + (1-\sigma) D_{DT}(E)\,, \qquad (6)$$

where E is the energy of tunneling electron, z is a spatial location of dangling bond, and $D_{TAT}$ and $D_{DT}$ depict the tunneling probabilities of trap-assisted tunneling and direct tunneling, respectively. While $D_{DT}$ is calculated using the Wenzel-Kramers-Brillouin (WKB) approximation, $D_{TAT}$ is calculated by $D_{TAT} = 1/ (D_1^{-1}+D_2^{-2})$, where $D_1$ and $D_2$ are the tunneling probability from the beginning of tunneling to the considered dangling bond and that from the dangling bond to the end of tunneling, respectitively. Both $D_1$ and $D_2$ are calculated in the same manner as $D_{DT}$. The formula for leakage current ($J_G$) is, therefore,

$$J_G = \sigma Y_{DB} \int dE \int dz R(z) D_{TAT}(E) + (1-\sigma) \int dE\, D_{DT}(E). \qquad (7)$$

This formula is also used in the analysis of tunnel mass shown in Fig. 2, and thereby, we have $m_e = m_h = 0.85m_0$. Here we assume that σ is a constant in the integrals of E and z. In Fig. 21, we show the influence of σ on the current. It is found that the TAT vanishes, while σ is less than $10^{-15}$ $cm^2$, i.e., the capture radius is a few Å. If we can reproduce the

leakage current with σ being less than this value, the leakage mechanism is not TAT but direct tunneling.

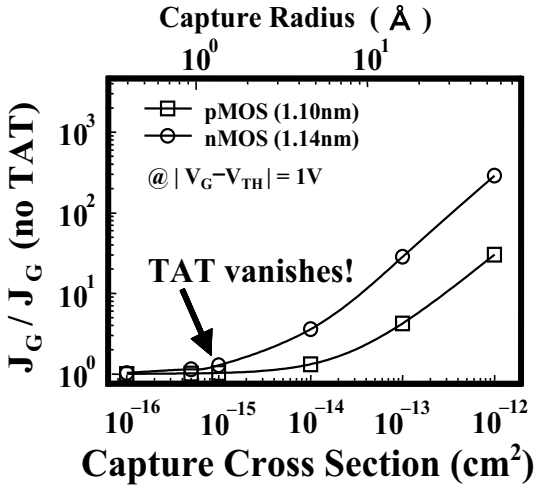


**Fig. 21**. Impact of capture-cross section on current.

In Fig. 22, we compare the calculated currents with the measured ones, using the measured profiles of R, the parameters shown in Table II, the universal tunnel mass ($0.85m_0$) and $\sigma = 0$. The excellent agreement is obtained, irrespective of film thickness. This decisively suggests that the leakage mechanism of ultra-thin SiON film is the direct tunneling enhanced by barrier modulation due to the positive charges trapped by dangling bonds whose profile is proportional to that of Si-N atomistic bonds with the proportional coefficient being $Y_{DB}$. This is quite similar to the degradation mechanism of data retention of floating gate memory cell [34].

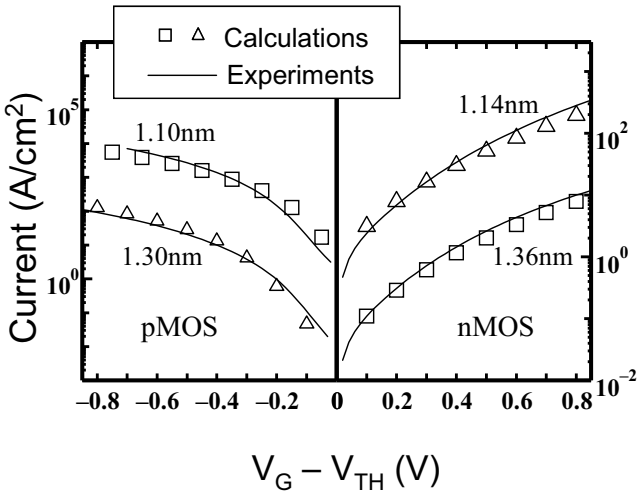


**Fig. 22**. Comparison of calculated and measured gate currents

## Conclusion

From the literature where the IFT layers are ignored, the tunnel masses for holes and electrons in $Si_3N_4$ have been regarded as 70% and 54.3% of the electron tunnel mass in

$SiO_2$, respectively [35]. If the electron tunnel mass in $SiO_2$ was $0.42m_0$ [36], then the hole tunnel mass in $Si_3N_4$ would be $0.3m_0$ [37]. The unified model with the IFT layers makes the calibrated values of tunnel masses for electrons and holes are the same, $0.85m_0$, irrespective of film thickness as long as the film component exists around the tie-line of $(SiO_2)_{1-x}(Si_3N_4)_x$ with the IFT layers.

In conclusion, we have unified the physical models co-working in MOS/MIS capacitor, to reproduce CV- and JV-characteristics. The parameters calibrated individually are the tunnel masses for electrons and holes, and the off-stoichiometric ratio of dielectric material (abbreviated $Y_{DB}$). Expanding the present achievement to general dielectric film, the requirement for "universal" tunnel mass would be:

1) Same between electrons and holes.
2) Independent of dielectric thickness.
3) Irrespective of dielectric material.

Further study of metal gate with high-K dielectrics is indispensable for validating the universal tunnel mass. The $Y_{DB}$ assumed as the discrepancy from the stoichiometry is also important to distinguish the intrinsic factors from the extrinsic factors. If we can establish this universality, the device modeling would be much advanced.

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