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The Degradation of MILC P-Channel Poly-Si TFTs under Dynamic Hot-Carrier Stress Using a Novel Test Structure

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In this study, dynamic hot carrier effect in the MILC p-channel TFT device has been characterized by the unique struture. This novel structure is capable of spatially resolving the hot carrier effect and is highly sensitive to detect the defect-rich region. The dynamic hot carrier stress has been focused on the impacts of the frequency, the rise time and the fall time. In varied frequency stress condition, the degradation in the drain-sided monitor transistor (DMT) increases monotonically with increasing frequency, infering that more defects are generated by extra dynamic stress contribution in the drain side and degrade the characteristic of device. Under varied fall time stress condition, the on-current degradtion is severe with decreasing fall time due to the extra voltage drop during voltage switch. The final part is effect of rise time. While device switches, the large voltage drop exists in the junction between the channel and the drain, which resulted in anothor hot carrier degradation.

Introduction

In the past several decades, the amorphous silicon thin film transistor (TFT) was the main building block for manufacturing active-matrix liquid crystal display (AMLCD). However, the lower field-effect mobility prohibits the integration of amorphous silicon TFTs in the peripheral driver circuit. In this regard, the high-mobility polycrystalline silicon (poly-Si) TFTs prepared by excimer laser anneal (ELA) and metal-induced lateral crystallization (MILC) are desirable for integration of system on the panel to enhance device and circuit performance [1]. For MILC, low cost and low process temperature are its unique advantages for practical production [2]. While the mobility has improved with the advances in crystallization method, the reliability issues become one of the major concerns during device operation[3]. Recnetly, more studies has focused on the reliability of the n-channel poly-Si TFTs. In this work, we employed a novel test structure previously proposed by our group [4][5] to analyze the hot-carrier degradation in the MILC p-channel poly-Si TFTs.

Experimental

First, a 100 nm thermal oxide was grown on the Si wafer. Next, a 100 nm amorphous silicon layer was deposited by LPCVD at 550^{o}C, followed by the deposition of a 100 nm PECVD oxide as the blocking layer. After formation of the seeding windows,

a thin 5 nm Ni layer was deposited by E-gun. And then, the amorphous silicon layer was crystallized into polycrystalline silicon by annealing in a furnace at 540°C for 24 hours in N_2 ambient. Next, an isolation region was patterned after removing the blocking oxide and the Ni layer. Afterwards, a 30 nm-thick silicon oxide layer was deposited by PECVD, followed by the deposition of 150 nm-thick poly-Si layer for gate material. Then, a self-aligned BF_2^+ implantation was performed with a dose of 5×10^{15} /cm^2, and the dopant was activated at 600°C for 12 hours in N_2 ambient by furnace. Next, a PECVD silicon oxide layer of 200 nm thickness was deposited which served as the passivation layer to prevent the penetration of humidity and impurities. After opening the contact hole in the passivation layer, metallization was performed, followed by a sintering treatment at 400°C for 30 minutes in H_2 ambient.

Fig.1 shows the structure of the tester, consisting of one lateral transistor, denoted as TT, and three monitor transistors, denoted as SMT, CMT, and DMT. The dynamic stress is exerted on the TT, and the hot carrier effect is analyzed by the monitor transistor.

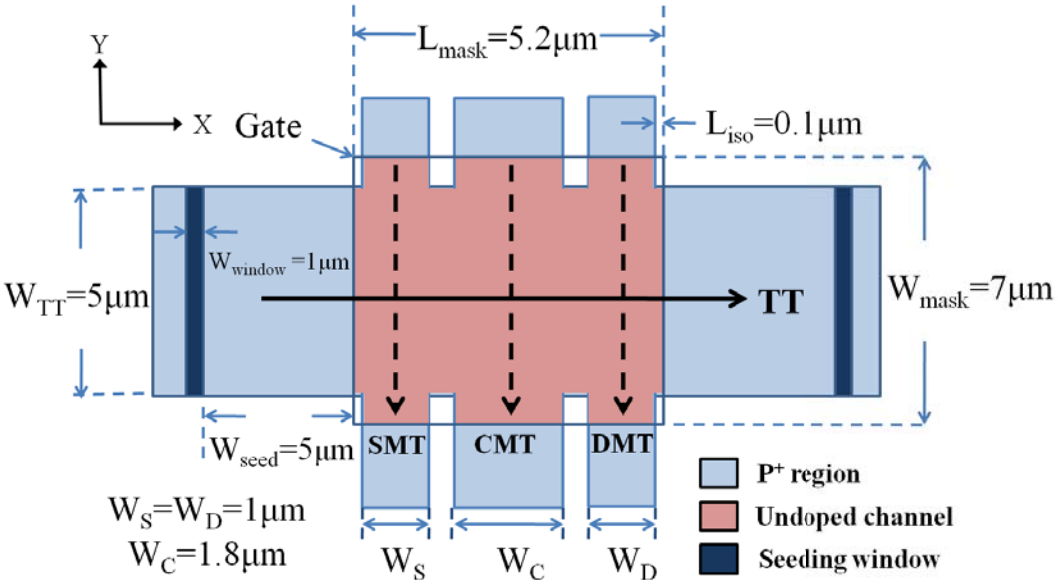

Fig.1 Top view of the test structure

Fig.2 shows the waveform of the AC signal applied during stress. The standard AC stress condition used in the experiment is set with V_G from -7.5 V (V_{G_low}) to 0 V (V_{G_high}) and set with V_D at -20 V for 1000s. The frequency is set at 500 kHz with fall time (ft) and rise time (rt) is equal to 100 ns, and the duty ratio is 50%. Fall time is the time that voltage signal falls from 90% to 10% of the amplitude ($V_{G\_high} - V_{G\_low}$), and vice versa for rise time. Subsequently, the information that should be required in the above parameters is varied to study their impact on the device degradation. The frequency is varied from 100 kHz to 1MHz, and both rise time and fall time are varied from 100 ns to 10 ns.

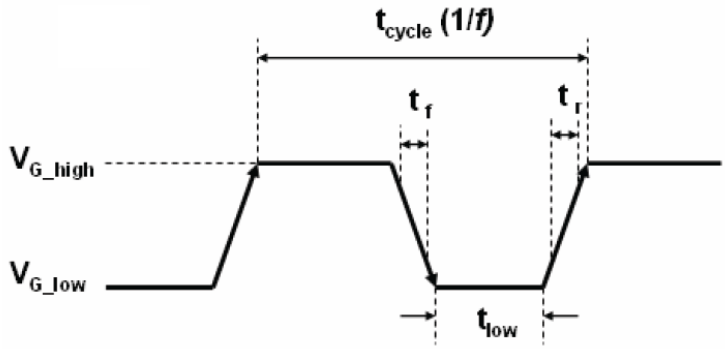

Fig.2 The waveform of AC stress signal

Results and Discussion

Frequency

Fig. 3(a) shows electrical characteristics of the TT before and after AC stress. The stress condition is V_G = -7.5 V and V_D = -20 V with rise time and fall time equal to 100ns at 100kHz for 1000s. With such stress condition, less hot-carrier induced degradation is observed by the TT, because the grain size in the MILC device is large, implying less grain boundary in the channel. Once the device is exerted hot carrier stress, less defects generate in the grain boundary. The monitor transistors embedded in the same test structure can be employed to help address the issue, and the results observed by CMT and DMT are shown in Fig. 3(b) and (c), respectively. The typical cahracteristic of SMT(not shown) is the same as that of CMT, which exhibits negligible degradation in the typical characteristic curves after AC stress. Apparently, Fig. 3(c) shows significant shift in subthreshold characteristics of DMT. Device degradations in terms of on-current degradation and threshold voltage shift are observed obviously after AC stress. This indicates that defects, like interface states and traps in the grain-boundaries are generated and form a defect-rich region. Moreover, electrons are trapped in the gate oxide near the drain side of TT after the AC stress.

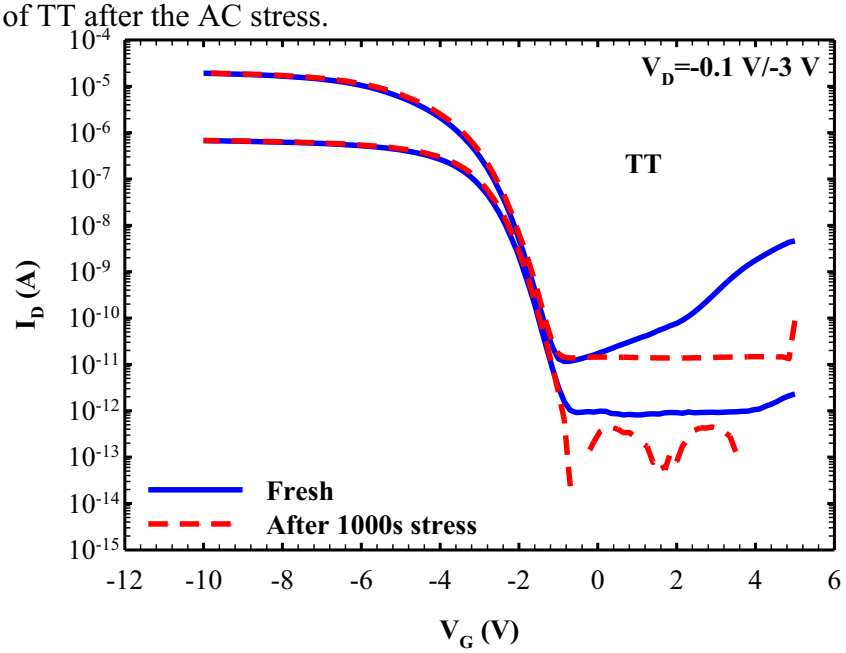

Fig.3 (a) The electrical characteristics of the TT before and after AC stress with V_G = -7.5 V and V_D = -20 V at 100kHz for 1000s.

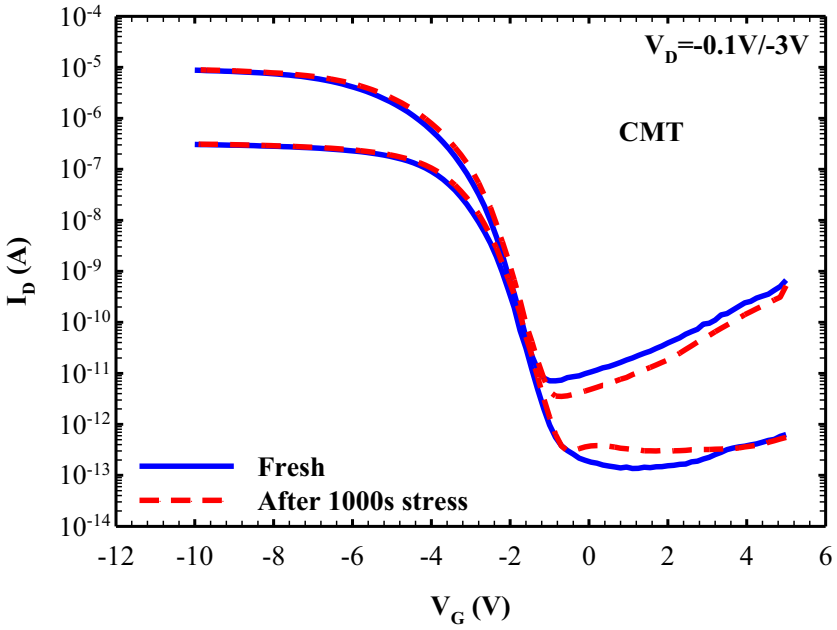

Fig.3 (b) The electrical characteristics of the CMT before and after AC stress with V_G = -7.5 V and V_D = -20 V at 100kHz for 1000s.

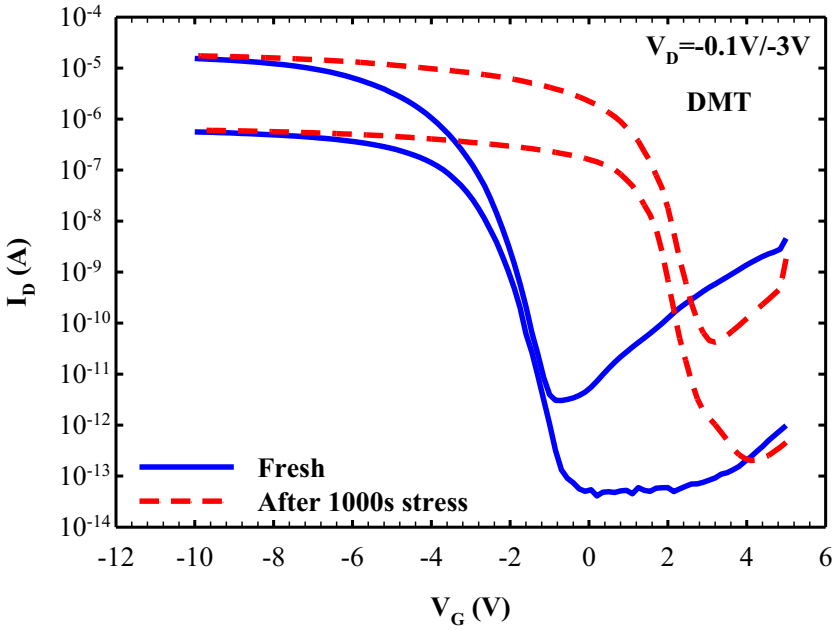

Fig.3 (c) The electrical characteristics of the DMT before and after AC stress with V_G = -7.5 V and V_D = -20 V at 100kHz for 1000s.

Fig. 4 and Fig. 5 show the on-current degradation and threshold voltage shift of TT and MTs after 1000 sec AC stress as a function of frequency. The results indicate that the damage induced in SMT and CMT is negligible and almost independent of the frequency. The on-current degradation is significant for the DMT, and it increases with increasing

frequency, inferring that additional damage is caused near the drain side as the frequency increases. This inference is the same as the trend verified by the unique structure as shown in Fig. 5, where the DMT shows significant shift. These results clearly demonstrate that the MTs of test structure can definitely resolve the non-uniform damage location and their excellent sensitivity for detecting the frequency-dependent degradation.

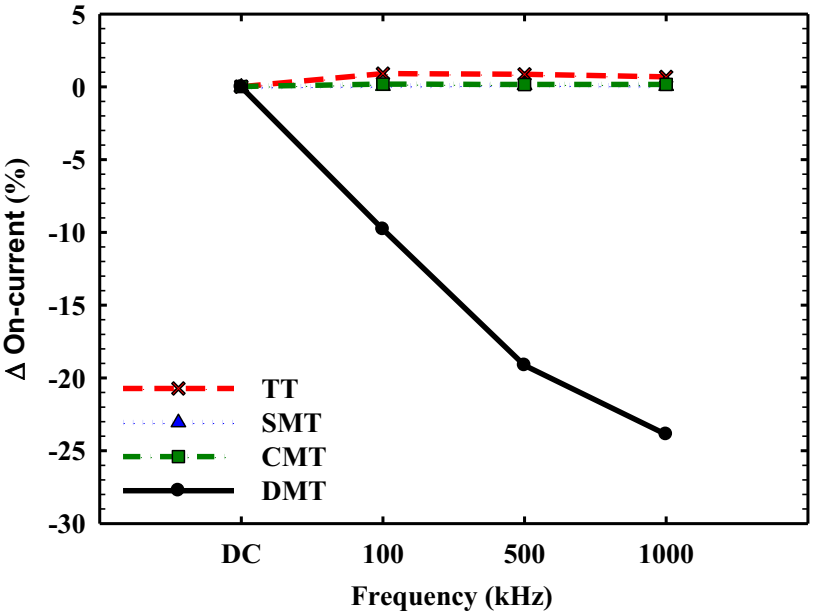

Fig.4 The on-current degradation of TT and MT after 1000 sec AC stress as a function of frequency

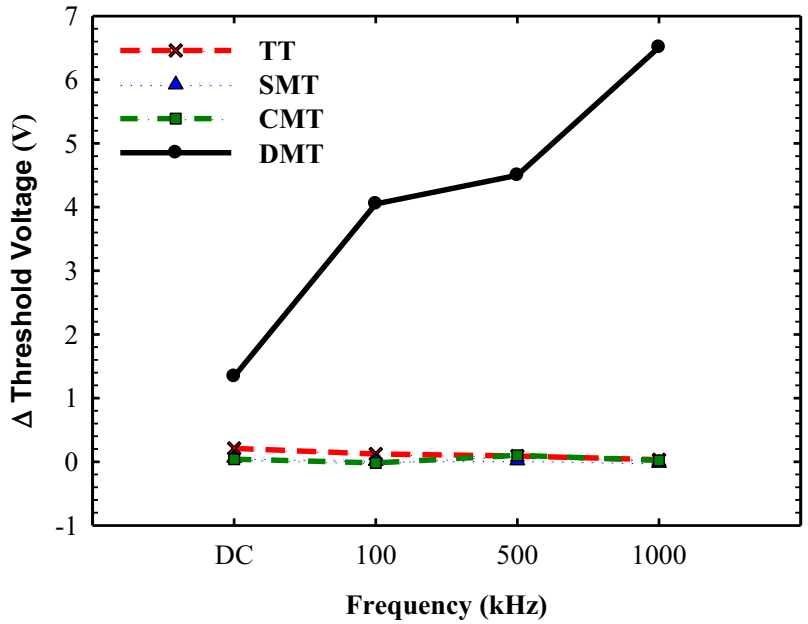

Fig.5 The threshold voltage shift of TT and MT after 1000 sec AC stress as a function of frequency

Rise Time

In this section, we investigate the effect of rise time. The AC stress condition is the same as the standard one except the rise time. Fig. 6 and Fig. 7 show subthreshold characteristics of DMT before and after AC stress with the rise time of 100 ns and 10 ns, respectively. The results show that the device performance degrades more under a faster rise time of AC stress. Fig. 8 and Fig. 9 show the on-current degradation and threshold voltage shift, respectively, under AC stress with fall time = 100 ns but with varying rise time. Still, the DMT exhibits the most serious degradation. Moreover, the damage becomes even more severe as the rise time is shortened.

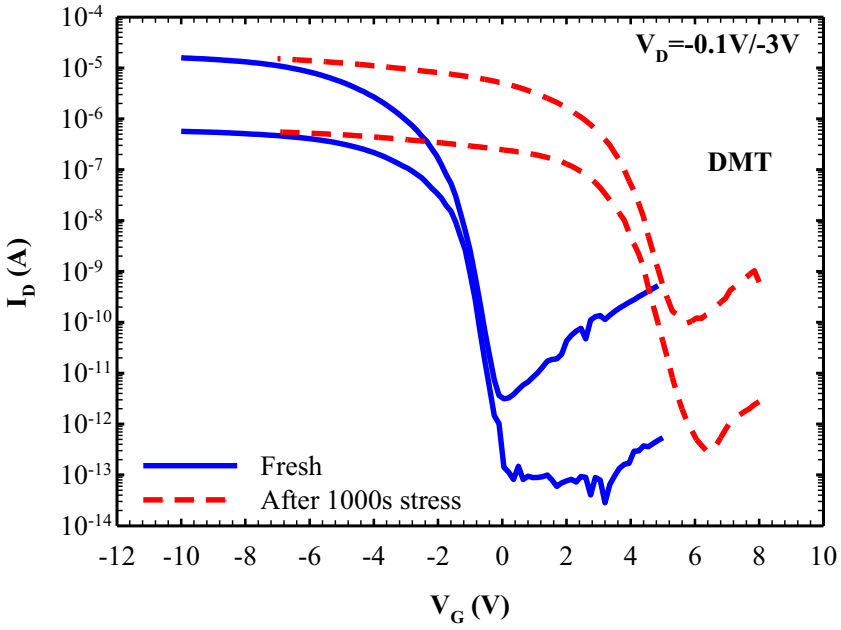

Fig.6 The electrical characteristics of the DMT before and after AC stress with the rise time of 10 ns

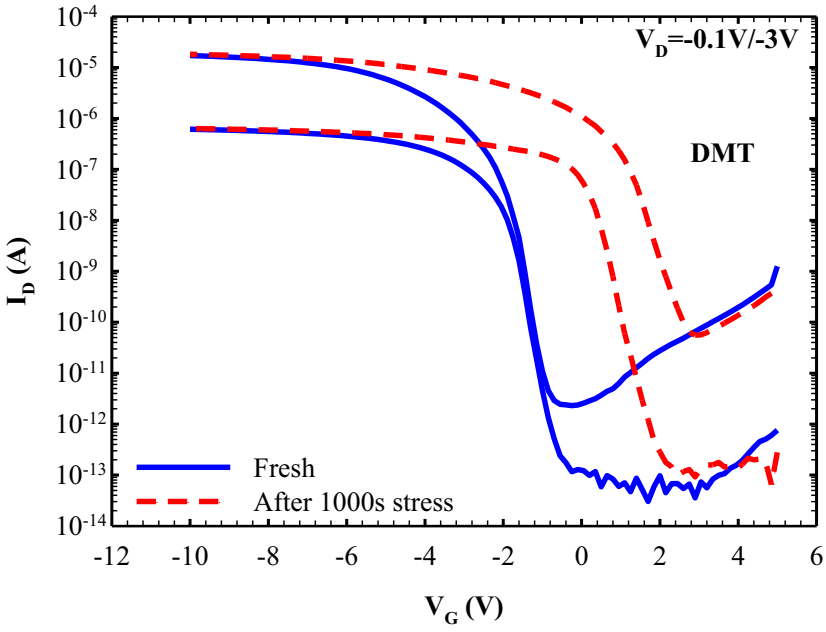

Fig.7 The electrical characteristics of the DMT before and after AC stress with the rise time of 100 ns

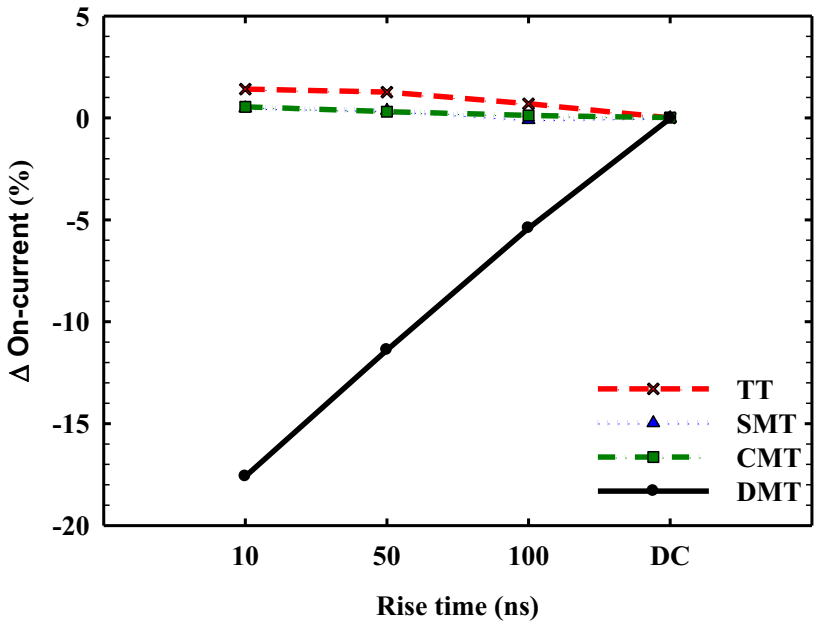

Fig.8 The on-current degradation of TT and MT after 1000 sec AC stress as a function of rise time

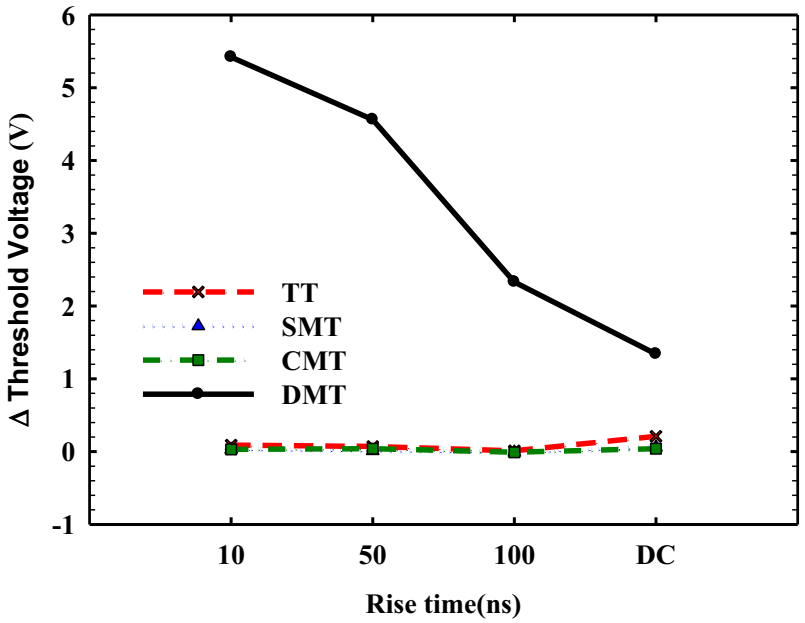

Fig.9 The threshold voltage shift of TT and MT after 1000 sec AC stress as a function of rise time

The degradation mechanism in the transient stage from VG_low to VG_high under AC stress is illustrated in Fig. 10[6]. As shown in the illustration, a high absolute pulse voltage is applied to the gate while the source is grounded and a high absolute bias is applied to the drain. For gate pulse at VG_low of -7.5 V, a sheet of holes is induced in the

channel and the defects are attributed to the impact ionization occurring near the drain, as shown in Fig. 10(a). Defect generation results in on-current reduction. Some portions of electrons induced by impact ionization may trap in the gate oxide and resulted in shift of threshold voltage. During the transient period (VG_low rise to VG_high), the inversion holes remained in the channel are mainly attracted by the negative drain bias and accelerated toward the drain, resulting in additional damages and more electrons trapped in the gate oxide, as shown in Fig. 10(b). In the case of a slow rise time, most of the holes have enough time to relax through collisions. Thus, the hot-carrier issue is also relaxed. On the other hand, in the case of a fast rise time, the voltage drop across the drain junction is increased by ΔE (Fig. 10) in a short time, and more hot holes are expected to be generated, causing more damage in the regions of channel near the drain of the TT. For this reason, the on-current degradation of DMT, and the threshold voltage shift of DMT are related to rise time during AC stress.

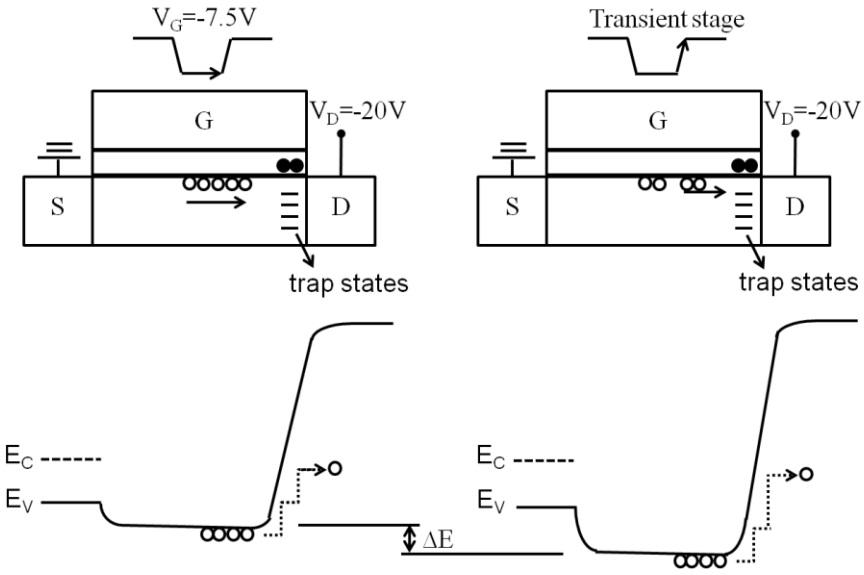

Fig.10 Degradation mechanism of variable rise time under AC stress

Fall Time

Here, the effect of fall time is discussed. The AC stress condition is the same as the standard one except the fall time. Fig. 11 and Fig. 12 show typical characteristics of DMT before and after AC stress with fall time of 100 ns and 10 ns, respectively. The results indicate that the degradation of device under the AC stress is higher as the fall time becomes shorter. Figure 13 and Fig. 14 show the on-current degradation and threshold voltage shift, respectively, under AC stress with fixed rise time = 100 ns as function of fall time. Comparing the on-current degradation and threshold voltage shift of the three MTs under AC stress, only those of the DMT increase dramatically with decreasing fall time, indicating that additional defect generation and electron trapping in gate oxide occur as the fall time is shortened.

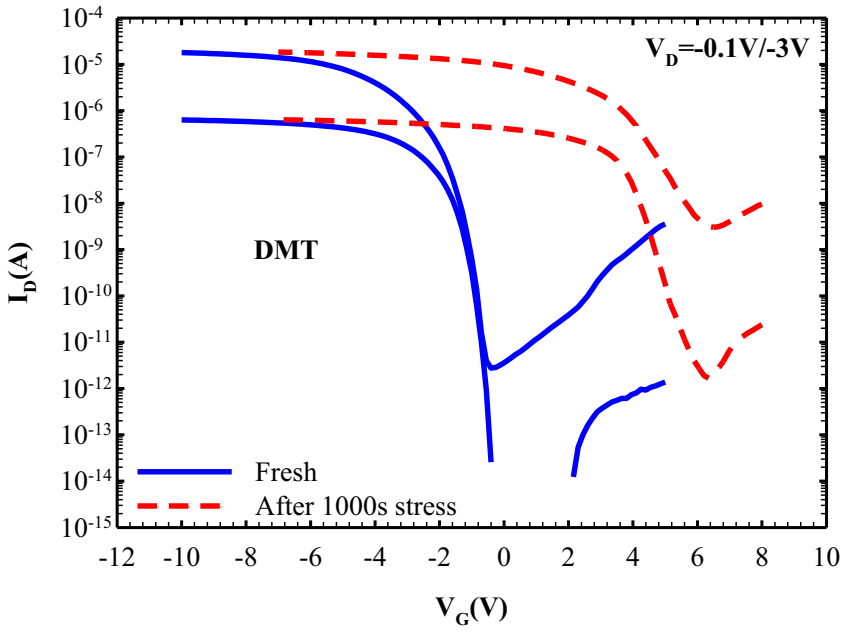

Fig.11 The electrical characteristics of the DMT before and after AC stress with the fall time of 10 ns

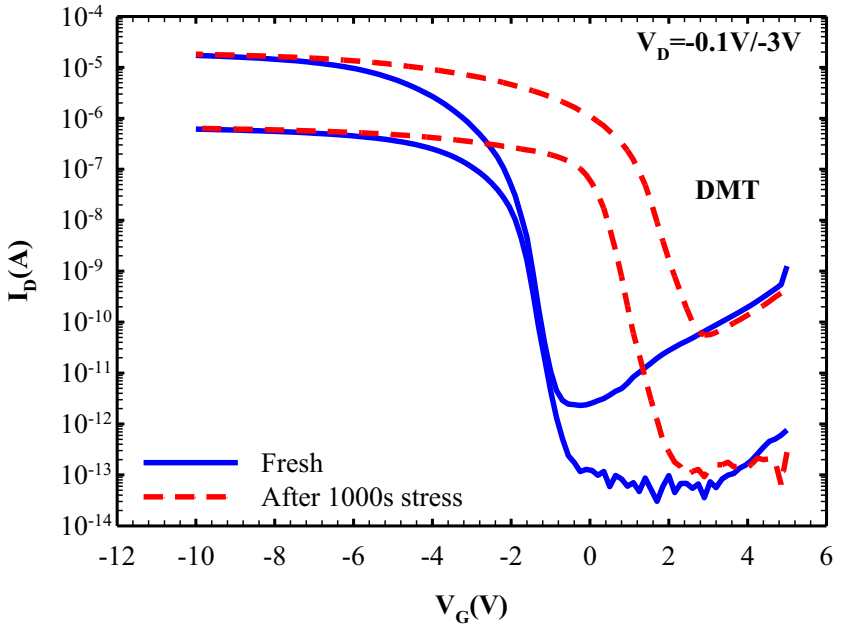

Fig.12 The electrical characteristics of the DMT before and after AC stress with the fall time of 100 ns

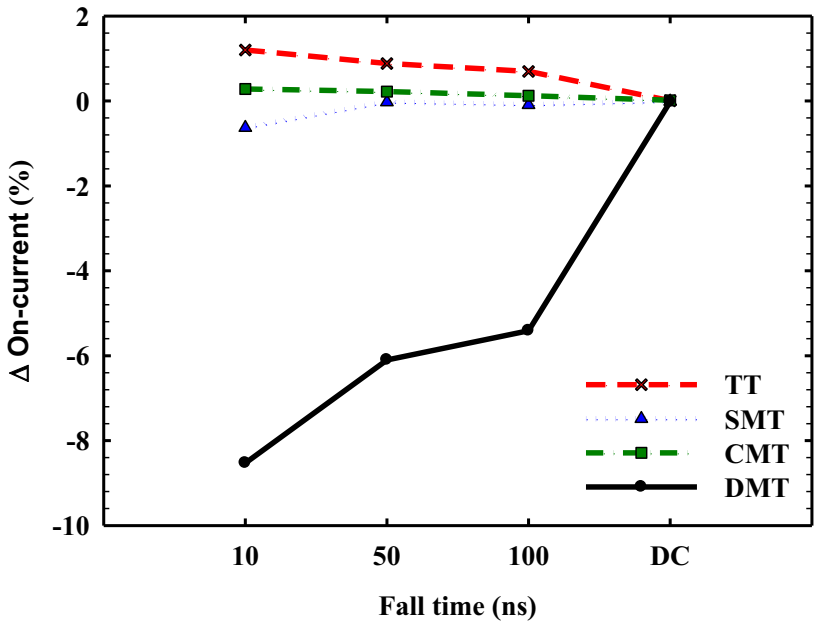

Fig.13 The threshold voltage shift of TT and MT after 1000 sec AC stress as a function of fall time

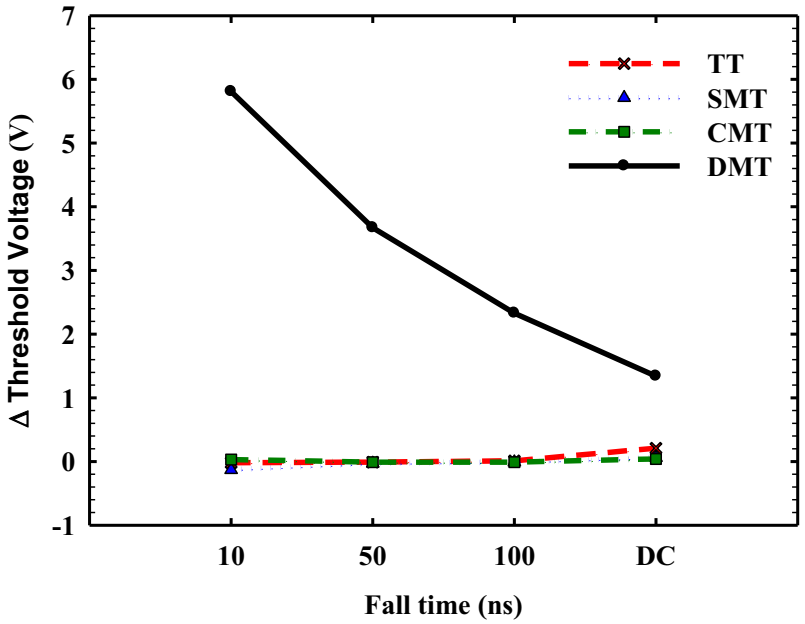

Fig.14 The threshold voltage shift of TT and MT after 1000 sec AC stress as a function of fall time

Fig. 15 shows a proposed scenario for explaining the effect of fall time under AC stress. When a VG_high = 0 V is applied to the gate, high gate-induced drain leakage by band to band tunneling (BTBT) dominates the conduction due to the high voltage difference between the gate and the drain, as shown in Fig. 15(a). Under the situation, the channel field is more or less uniform, and the electrons appear at the tunneling junction (i.e., drain junction of the TT) would drift toward the source by the field. When the gate voltage is switched from VG_high to VG_low, a high voltage drop is developed at the channel/drain junction in a short time due to the formation of the inversion hole layer, as shown in Fig. 15(b). Portions of the electrons coming from the gate-induced-drain-leakage (GIDL) current remained at the original tunneling junction would be accelerated by the suddenly presenting field. This leads to the generation of hot electrons, which create defects in the channel and trapped into the oxide (near the drain of the TT). Such phenomenon becomes more significant as the fall time is reduced. This explains why the on-current degradation of DMT shown in Fig. 13, and threshold voltage shift of DMT shown in Fig. 14.

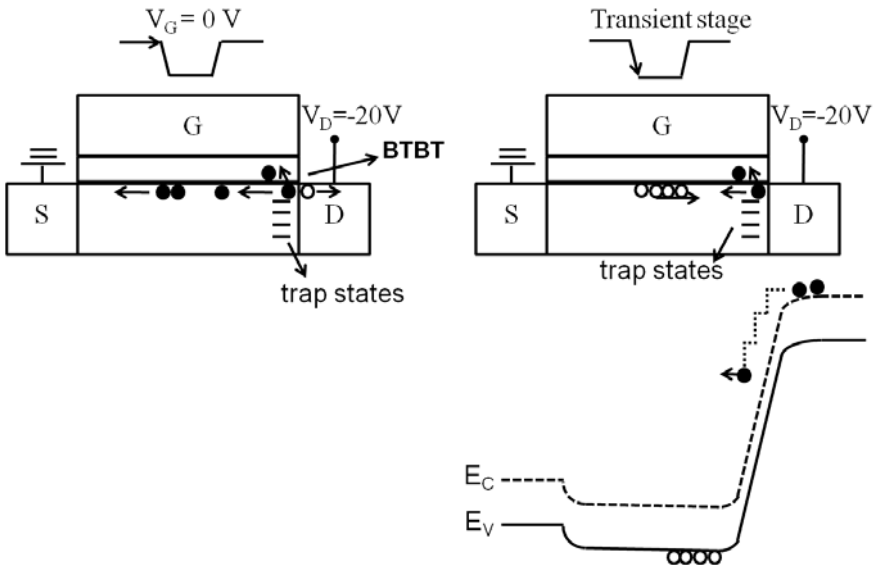

Fig.15 Degradation mechanism of variable fall time under AC stress

Conclusions

A new approach for characterizing and resolving the hot-carrier degradation in thin-film transistors is proposed and sucessfully demonstrated using a novel test structure. With AC stress, we can identify the relationship between the frequency, the fall time, and rise time for the AC hot carriers. In this work, the major damage induced near the drain side of the TT and the trapping of electrons in the gate oxide can be accutely resolved by means of the DMT embedded in the test structure. The new test structure is highly sensitive for detecting degradations in the device.

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