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Preparation of IGZO sputtering target and its applications to thin-film transistor devices

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Abstract

Nano-scale In_2O_3, Ga_2O_3 and ZnO powder mixture prepared by a hybrid process of chemical dispersion and mechanical grinding was adopted for the In–Ga–Zn–O (IGZO) sputtering target fabrication. A pressure-less sintering at 1300 °C for 6 h yielded the target containing sole $InGaZnO_4$ phase with relative density as high as 93%. Consequently, the thin-film transistor (TFT) devices containing amorphous IGZO channels were prepared by using the self-prepared target and the electrical measurements indicated the TFT subjected to a post annealing at 300 °C exhibits the best device performance with the saturation mobility = 14.7 cm^2/V s, threshold voltage = 0.57 V, subthreshold gate swing = 0.45 V/decade and on/off ratio = 10^8. Capacitance–voltage measurement indicated that post annealing effectively suppresses the interfacial traps density at the IGZO/SiO_2 interface and thus enhances the electrical performance of TFT.

Keywords: IGZO; Thin-film transistor; Interfacial traps density

1. Introduction

Recently, amorphous oxide semiconductors (AOSs) such as Sn–Zn–O (SZO), In–Zn–O (IZO) and In–Ga–Zn–O (IGZO) have received a considerable attention in the large-area flat panel display (FPD) industry since they may overcome the difficulties encountered in the amorphous and polycrystalline silicon thin-film transistor (*a*-Si:H and poly-Si TFT) technologies [1]. The poor field-effect mobility (<1 cm^2/V s) and small on-current property are drawbacks of *a*-Si:H TFTs although their processing temperature is low and may save the product cost [2]. The poly-Si possesses a much higher carrier mobility (>10 cm^2/V s) than that of *a*-Si:H; however, its processing temperatures are comparatively high and the complicated recrystallization methods to eliminate the grain boundaries in the poly-Si layer might escalate the cost of TFT production [3].

As the attractive active channel materials for TFT in FPD products, AOSs provide the advantages including high saturation mobility (μ_{sat} > 10 cm^2/V s), low deposition temperatures, good film uniformity and compatibility to conventional sputtering processes [4–6]. Among various AOS types, the quaternary IGZO system based on In_2O_3, Ga_2O_3 and ZnO oxide components is of particular interest because of its relatively high μ_{sat} property in the range of 10–50 cm^2/V s, high transparency in visible-light wavelength region and capability to produce the films with various conductivities [7]. Nomura et al. prepared the transparent and flexible TFTs on a polyethylene terephthalate (PET) substrate by a room-temperature physical vapor deposition process [1]. In their TFT devices, amorphous $InGaZnO_4$ (*a*-IGZO) served as the channel layer and the μ_{sat} about 12 cm^2/V s was achieved. TFTs containing *a*-IGZO channels were also reported by Abe et al. and their devices exhibited the μ_{sat} > 9.0 cm^2/V s, off current <10 pA and subthreshold gate swing (*S.S.*) <0.2 V/decade [8]. Jeong et al. prepared the *a*-IGZO TFT devices *via* a co-sputtering of IGZO and indium zinc oxide (IZO) targets [9]. By adjusting the IGZO/IZO ratio in the channel layer, they were able to improve the μ_{sat} and *S.S.* parameter up to 19.3 cm^2/V s and 0.35 V/decade, respectively.

Highly transparent feature facilitates another promising application for IGZO as the transparent conducting oxide (TCO) electrode which is an essential part to FPDs and photovoltaic devices. Indium tin oxide (ITO) is the most common TCO; nevertheless, the scarcity of In and recent

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flourishing of FPD and solar cell industries drastically tightens the supply of ITO. Besides, the deposition temperature of ITO layer is relatively high for optimizing the optical and electrical properties [10]. Presently, the doped ZnO such as aluminum-doped ZnO (ZnO:Al or AZO) and multi-component oxides such as IGZO are recognized as the promising alternatives for ITO. However, their physical properties are still required further refinement for practical applications.

Nano-scale In_2O_3, Ga_2O_3 and ZnO oxide powders were prepared in this study *via* a hybrid process of chemical dispersion and mechanical grinding and applied to the IGZO sputtering target fabrication. Sintering process to form the sputtering target comprised of sole $InGaZnO_4$ phase was also established and the TFT devices containing *a*-IGZO channel layers were prepared by using the sole-phase target. The microstructure, composition and transmittance of *a*-IGZO layers, the transfer characteristics of *a*-IGZO TFTs as well as the influence of post annealing on the defect configurations of samples were characterized and presented as follows.

2. Experimental

As-received ZnO (purity = 99.999%, Seedchem/Australia), Ga_2O_3 (purity = 99.995%, ELECMAT/USA) and In_2O_3 (purity = 99.99%, CERAC/USA) raw oxide powders were first rinsed in ethanol. The oxide powders were mixed at the molar ratio = 1:1:2 (*i.e.*, the stoichiometric ratio of $InGaZnO_4$ phase) and then transferred to a hybrid process of chemical dispersion and mechanical grinding [11] to form the aqueous suspension containing nano-scale In_2O_3–Ga_2O_3–ZnO powder mixture. Such a hybrid process was able to produce the oxide particles with average diameter of 74 ± 10 nm as determined by the particle size analyzer (BECKMAN COULTER Delsa^{TM} Nano C) and a representative micrograph obtained by scanning electron microscopy (SEM, JEOL-6700) is given in Fig. 1(a). In comparison with oxide powders prepared by traditional ball milling method, the nano-scale oxide powders subjected to surface modification exhibited good dispersion behaviors and allowed the formation of compact green body with uniform composition distribution. Moreover, the high specific-surface-area feature of nano-scale oxide powders might promote the sintering process and effectively suppress the sintering temperature for desired phase formation [11]. This provides an efficient method for preparing the high-density, sole-phase IGZO sputtering target with the saving of thermal budget.

After drying, the powder mixture was pressed into the disc form at pressure = 100 MPa and consequently sintered without external pressure at temperatures ranging from 900 to 1300 °C for various time spans. Phase constitutions of the sintered IGZO targets were analyzed by *x*-ray diffraction (XRD, MacScience M18XHF) within the Cu-K_α radiation (wavelength = 0.154 nm) at scanning rate of 3°/min. The relatively densities of target samples were measured by the Archimedes method with the aid of an electronic balance (Ax105,

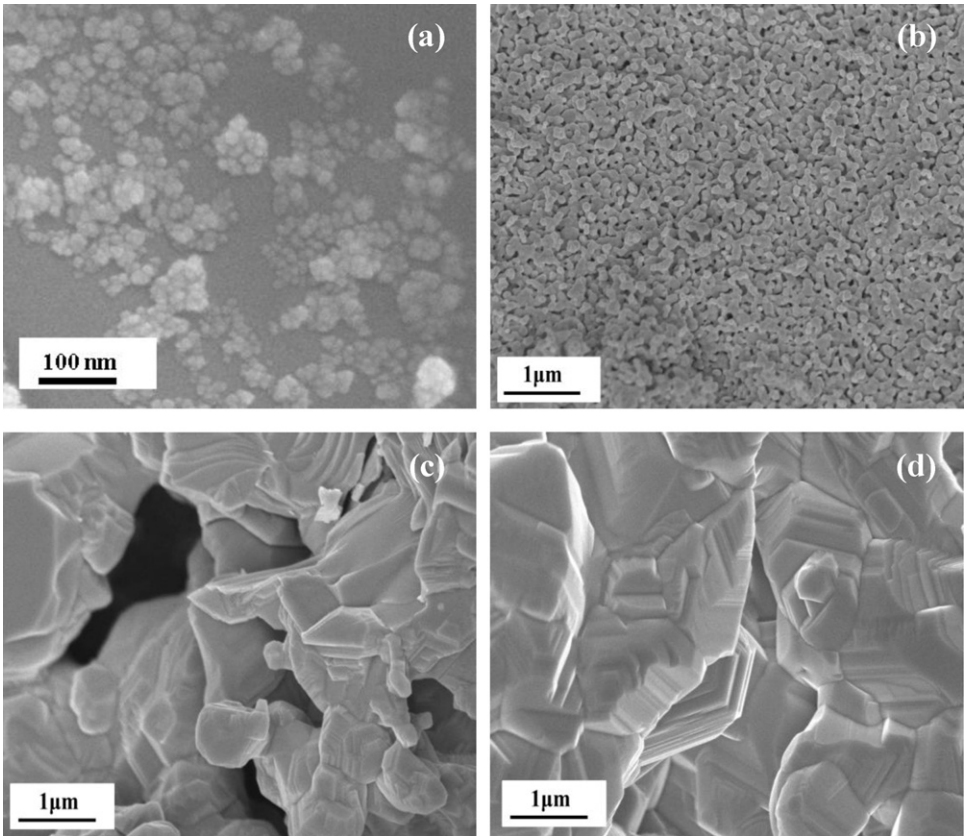

Fig. 1. SEM micrographs of (a) as-prepared In_2O_3–Ga_2O_3–ZnO powder mixture and morphologies of IGZO targets subjected to sintering treatments at (b) 1100 °C, (c) 1200 °C and (d) 1300 °C for 6 h.

Delta Range). Consequently, the target containing sole $InGaZnO_4$ phase was transferred to a sputtering system at background pressure better than 1×10^{-6} torr and the TFT devices containing 15-nm thick *a*-IGZO active channel layers were fabricated on the heavily doped n^+-Si substrates clad with 200-nm thick thermally grown SiO_2 layer. The *a*-IGZO layers were also deposited on glass substrates for physical property characterizations. The sputtering deposition was carried out at RF gun power of 80 W, working pressure of 1 mtorr and a mixed O_2/Ar inlet gas flow at the ratio of 0.06. Afterward, 300-nm thick Al metal strips serving as the source and drain electrodes were formed on *a*-IGZO layers by the *e*-beam evaporation using the shadow mask technique. The channel length and width of TFT devices were 0.1 and 1.4 mm, respectively. Prior to the Al electrode deposition, a post annealing at 300 °C for 1 h in atmospheric ambient were carried out for part of TFT samples in order to investigate its effects on the device property improvement.

The transfer characteristics of the *a*-IGZO TFTs were measured at room temperature in a probe system containing a Keithley 4200 precision sourcemeter. In order to clarify the role of bulk defects or interfacial traps on the TFT performance improvement, the metal–oxide–semiconductor (MOS) and metal–insulator–metal (MIM) samples containing various *a*-IGZO layers were separately prepared for capacitance–voltage (*C–V*) and current–voltage (*I–V*) characterizations. The *C–V* and *I–V* measurements were separately performed by using an Wayne Kerr 6520B precision LCR meter and an HP 4156B semiconductor parameter analyzer in conjunction with a probe station (SANWA, WM-365A-1). Microstructures of TFT samples were examined by a transmission electron microscope (TEM, JEOL-2100) operating at 200 kV. UV–Vis spectrometer (Hitachi, U3900H), X-ray photoelectron spectroscopy (XPS, PHI-1600) and atomic force microscopy (AFM, NS4/D3100CL/MultiMode) were adopted to characterize the transmittances, chemical compositions and surface roughness of *a*-IGZO layers in TFT samples, respectively.

3. Results and discussion

3.1. Characterizations of IGZO target and sputtering deposited films

Fig. 1(b)–(d) separately presents the morphology of IGZO target sintered at 1100 °C, 1200 °C and 1300 °C for 6 h. As shown in Fig. 1(b), coalescence of oxide particles with insignificant increase of grain size was observed in the sample sintered at 1100 °C. Grain growth became rather obvious in the samples subjected to the sintering at temperatures higher than 1200 °C that the grains with several micrometers in size can be readily seen as shown by Fig. 1(c) and (d). Notably, the increase of sintering temperature was relevant to the densification of sintered body. As revealed by the density measurement, the relative density of sample was 79, 88 and 93% for the IGZO sample sintered at 1100 °C, 1200 °C and 1300 °C, respectively.

Fig. 2 presents the XRD patterns of as-prepared In_2O_3–Ga_2O_3–ZnO powder mixture and the IGZO targets subjected to sintering treatments at various temperatures for 6 h. With the aid

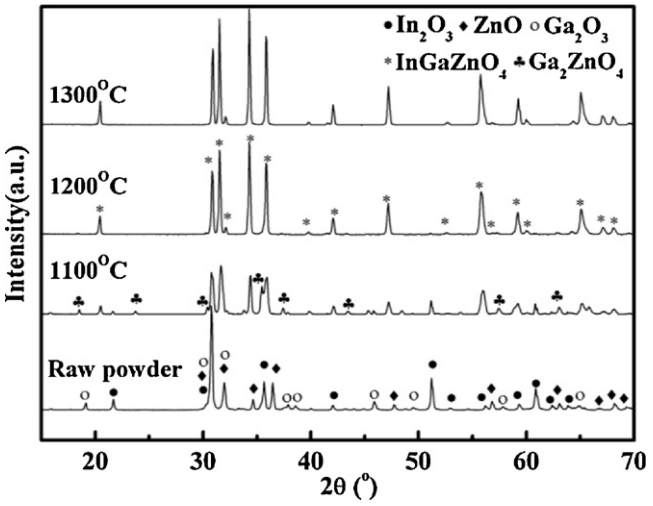

Fig. 2. XRD patterns of as-prepared In_2O_3–Ga_2O_3–ZnO powder mixture and the IGZO targets subjected to sintering treatment at various temperatures.

of Joint Committee of Powder Diffraction Standard (JCPDS) file Nos. 860410 and 381104, cubic Ga_2ZnO_4 spinel and rhombohedral $InGaZnO_4$ phases were identified in the 1100 °C-sintered sample in addition to the as-prepared oxide powder phases. The $InGaZnO_4$ became the dominant phase in the samples when sintering temperatures exceeded 1200 °C. In this study, the appropriate sintering condition was identify as 1300 °C/6 h since the target sample containing sole $InGaZnO_4$ phase with relatively density as high as 93% could be achieved at such a condition.

Fig. 3 shows the XRD patterns of as-deposited and the 300 °C-annealed *a*-IGZO layers prepared by using above-mentioned sole-$InGaZnO_4$-phase sputtering target. Lack of distinctive diffraction peaks in the XRD profiles implies the oxide layer annealed at high temperature of 300 °C remains amorphous without the presence of secondary phase. The amorphism of *a*-IGZO layer was further confirmed by the cross-sectional TEM characterization of a TFT sample containing the annealed *a*-IGZO channel layer as shown in Fig. 4. The absence of grain contrast in *a*-IGZO layer and the

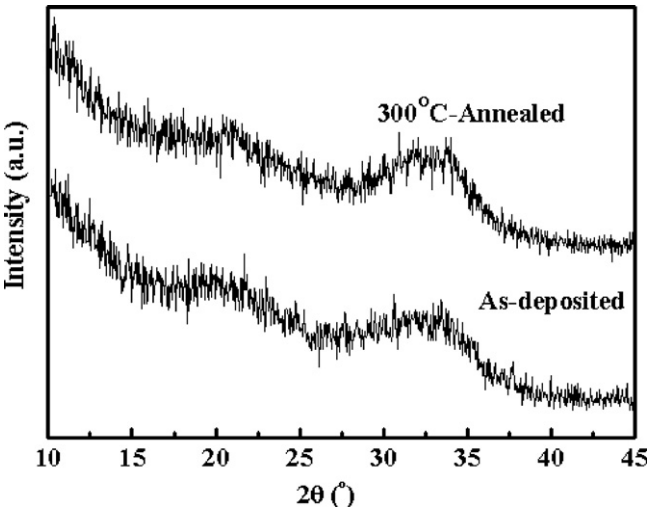

Fig. 3. XRD patterns of as-deposited and the 300 °C/1-h annealed *a*-IGZO layers (sample thickness = 100 nm).

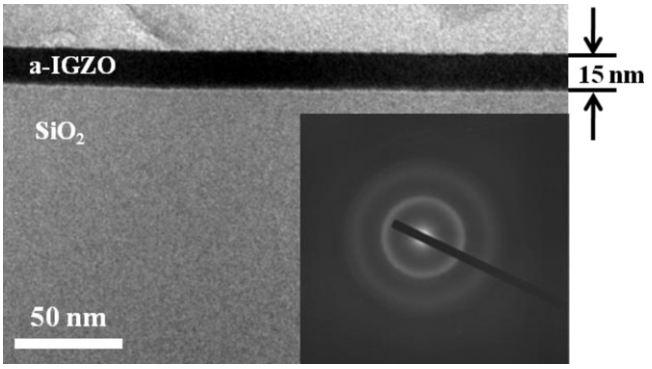

Fig. 4. Cross-sectional TEM micrograph of a 15-nm thick *a*-IGZO layer in a TFT sample subjected to 300 °C/1-h annealing treatment.

fuzzy diffraction rings in the selected area electron diffraction (SAED) pattern taken from the region of channel layer evidence the amorphous feature of *a*-IGZO layer. Moreover, the *a*-IGZO layer exhibited a relatively smooth surface with average roughness about 0.15 nm as revealed by the AFM measurement. The *a*-IGZO layers also possessed high optical transparency as indicated by the transmittance profiles (see Fig. 5) which show, regardless of the annealing treatment, the average transmittance of *a*-IGZO layers remains as high as 85% in visible-light region. This illustrates the feasibility of *a*-IGZO layer to the fabrication of fully transparent TFTs.

Table 1 summarizes the stoichiometric ratios of In, Ga, Zn and O elements in IGZO target sample, as-deposited and annealed *a*-IGZO layers deduced by the XPS analysis. In considering the detecting error, the similar atomic ratios of In, Ga, Zn and O elements listed in Table 1 illustrate the good consistency in chemical compositions of the quaternary sputtering target and corresponding thin-film samples.

3.2. Electrical Performance of a-IGZO TFTs

Fig. 6(a) and (b) depict the transfer characteristics of *a*-IGZO TFT devices prior and posterior to the post-annealing

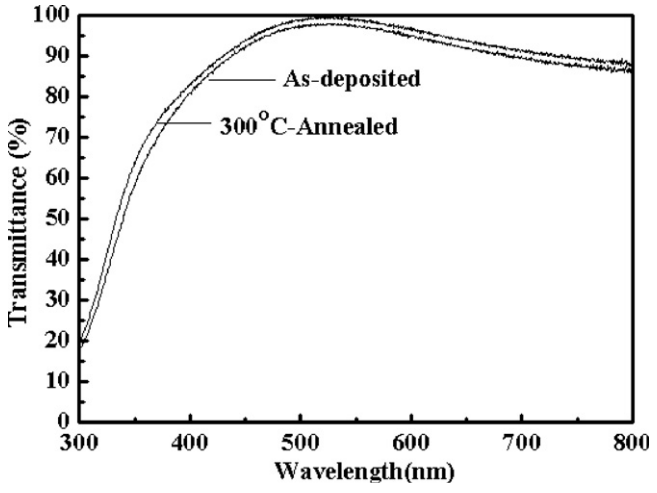

Fig. 5. Transmittance profiles of as-deposited and 300 °C/1-h annealed *a*-IGZO layers (sample thickness = 15 nm).

Table 1
Stoichiometric ratios of In, Ga and Zn elements in IGZO target, as-deposited and 300 °C-annealed *a*-IGZO layers analyzed by XPS (in at.%).

Sample type	In	Ga	Zn	O
IGZO target	1.07	0.84	1.00	4.3
As-deposited *a*-IGZO film	1.29	0.97	1.00	3.9
300 °C-annealed *a*-IGZO film	1.25	1.00	1.00	4.1

treatment measured at the drain-to-source voltage (V_{DS}) ranging from 5 to 15 V. According to the drain-to-source current *versus* gate-to-source voltage (I_{DS}–V_{GS}) profiles shown in Fig. 6(a), the TFT containing as-deposited *a*-IGZO layer possesses the $\mu_{sat} = 1.2\ cm^2/V\ s$, threshold voltage ($V_{th}$) = 1.85 V, *S.S.* = 0.85 V/decade and on/off ratio = 5×10^4

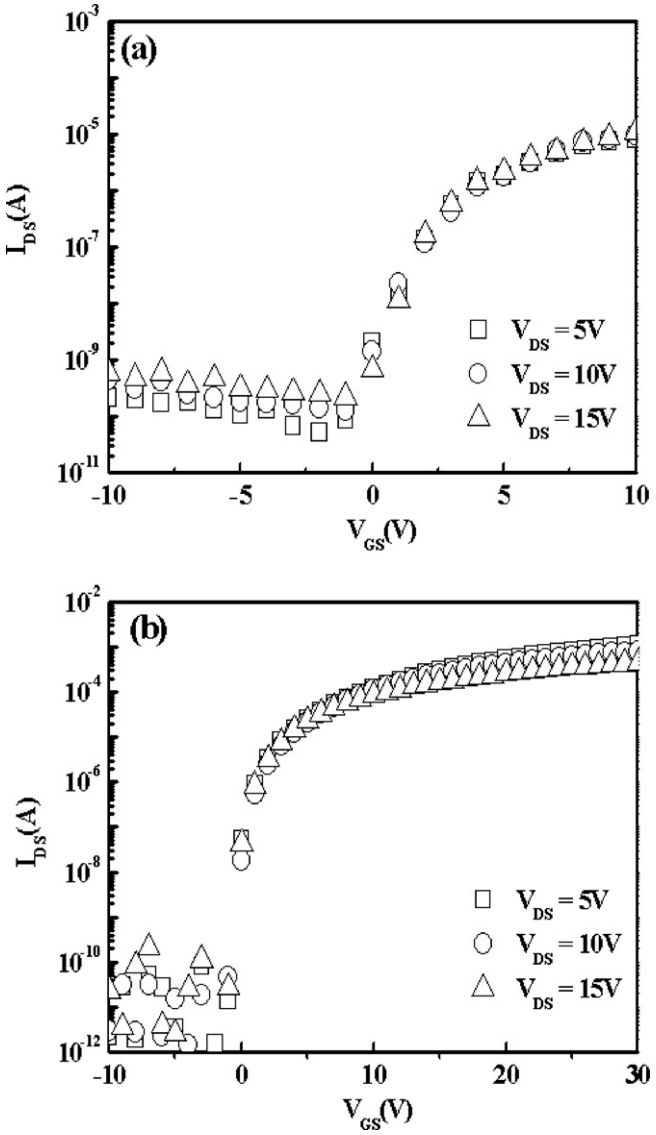

Fig. 6. Transfer characteristics of TFT samples containing (a) as-deposited and (b) 300 °C/1-h annealed *a*-IGZO channel layers measured at V_{DS} ranging from 5 to 15 V.

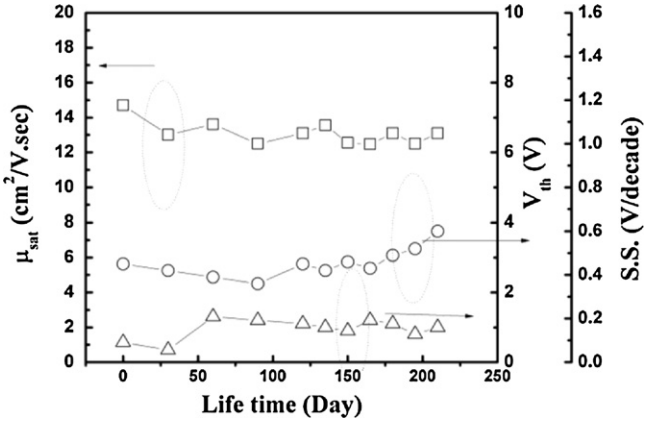

Fig. 7. Variation of μ_{sat}, V_{th} and *S.S.* of as a function of storage time for *a*-IGZO TFT stored in atmospheric ambient at room temperature.

while the device containing the 300 °C-annealed *a*-IGZO layer exhibits dramatically improved electrical performance with μ_{sat} = 14.7 cm^2/V s, V_{th} = 0.57 V, *S.S.* = 0.45 V/decade and on/off ratio = 10^8.

The TFT sample containing annealed IGZO channel layer was also stored in atmospheric ambient at room temperature and their electrical properties were constantly monitored. Fig. 7 shows the variations of μ_{sat}, V_{th}, and *S.S.* of the devices as a function of storage time. It can be seen that μ_{sat} remains at a relatively stable value about 13.1 cm^2/V s whereas V_{th} shifts toward the positive bias of about 1.5 V after seven-month storage. We note that the V_{th} shift should result from the environmental attack since no passivation layer is coated on our TFT device. The absorbed oxygen atoms diffused into the *a*-IGZO/SiO_2 interface, interrupted the interface trap states, and consequently degraded the TFT performance [12].

3.3. Effects of post annealing on the defect configurations of samples

Fig. 8(a) presents the *C–V* profiles (at 1 MHz) of MIM sample with the device structure depicted in the inset of this figure. As indicated by Fig. 8(a), the samples containing as-deposited and 300 °C-annealed *a*-IGZO layers exhibit similar capacitances density (C_{ox}) about 100 nF/cm^2. It is known that the C_{ox} is correlated to the trap density in the bulk of sample [13] and, hence, the post annealing up to 300 °C negligibly affects the bulk defects in *a*-IGZO layer. This is ascribed to the amorphous feature of annealed *a*-IGZO layer in which the structure irregularity prevails.

The *C–V* profiles of MOS samples containing as-deposited and 300 °C-annealed *a*-IGZO layers obtained at 100 kHz and 1 MHz are depicted in Fig. 8(b). A comparatively sharp transition from depletion region to accumulation region could be observed in the annealed sample, implying the post annealing might result in a well-formed *a*-IGZO/SiO_2 interface in TFT sample [14]. The trap density at *a*-IGZO/SiO_2 interface (D_{it}) was calculated in terms of the *C–V* data shown in Fig. 8(b)

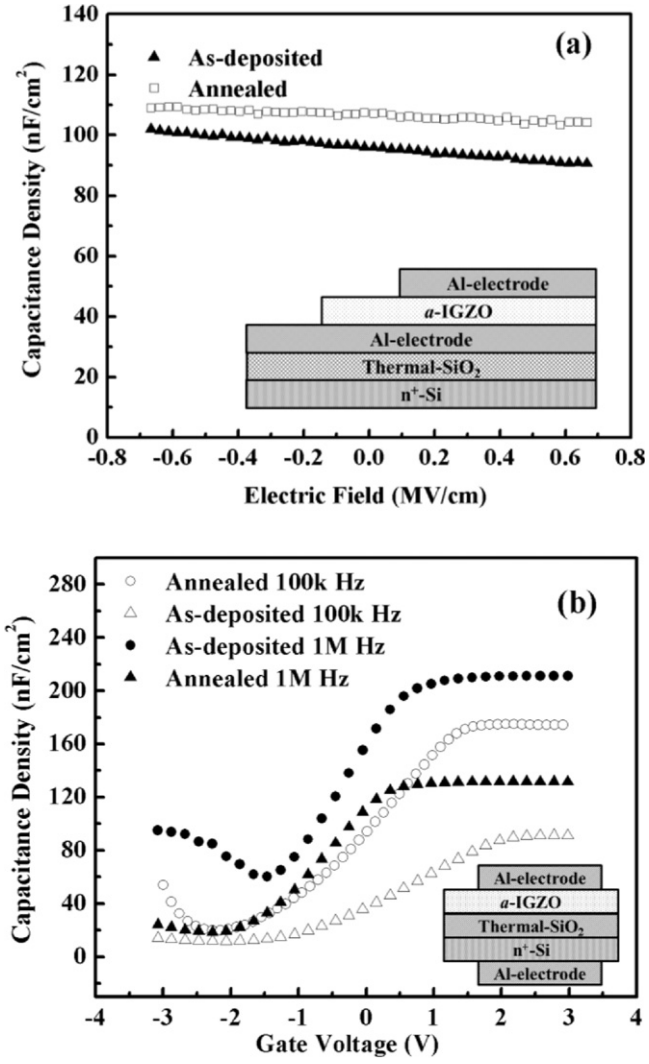

Fig. 8. *C–V* profiles of (a) MIM samples (at 1 MHz) (b) MOS samples (at 100 kHz and 1 MHz) containing as-deposited and 300 °C-annealed *a*-IGZO layers.

using the following equation [13]:

$$D_{it} = \frac{1}{q^2}\left(\frac{1}{C_{LF}} - \frac{1}{C_i}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_i}\right)^{-1} \quad (1)$$

where q is electron charge, C_i is the insulator layer capacitance, and C_{LF} and C_{HF} are the capacitance of the MOS sample obtained at the low and high frequencies, respectively. It was found that $D_{it} = 7.1 \times 10^{10}$ eV^{-1} cm^{-2} for annealed *a*-IGZO sample whereas $D_{it} = 2.8 \times 10^{11}$ eV^{-1} cm^{-2} for as-deposited sample. This indicates the improvement of TFT performance is mainly correlated to the suppression of defect traps at *a*-IGZO/SiO_2 interface of annealed sample.

The profiles of leakage current densities *versus* applied electric bias (*J–E*) deduced from the *I–V* measurement of MOS samples containing as-deposited and 300 °C-annealed *a*-IGZO layers are presented in Fig. 9(a). Note that the asymmetry in the *J–E* profiles is attributed to the difference in the material properties and conduction mechanism across the Al/IGZO and

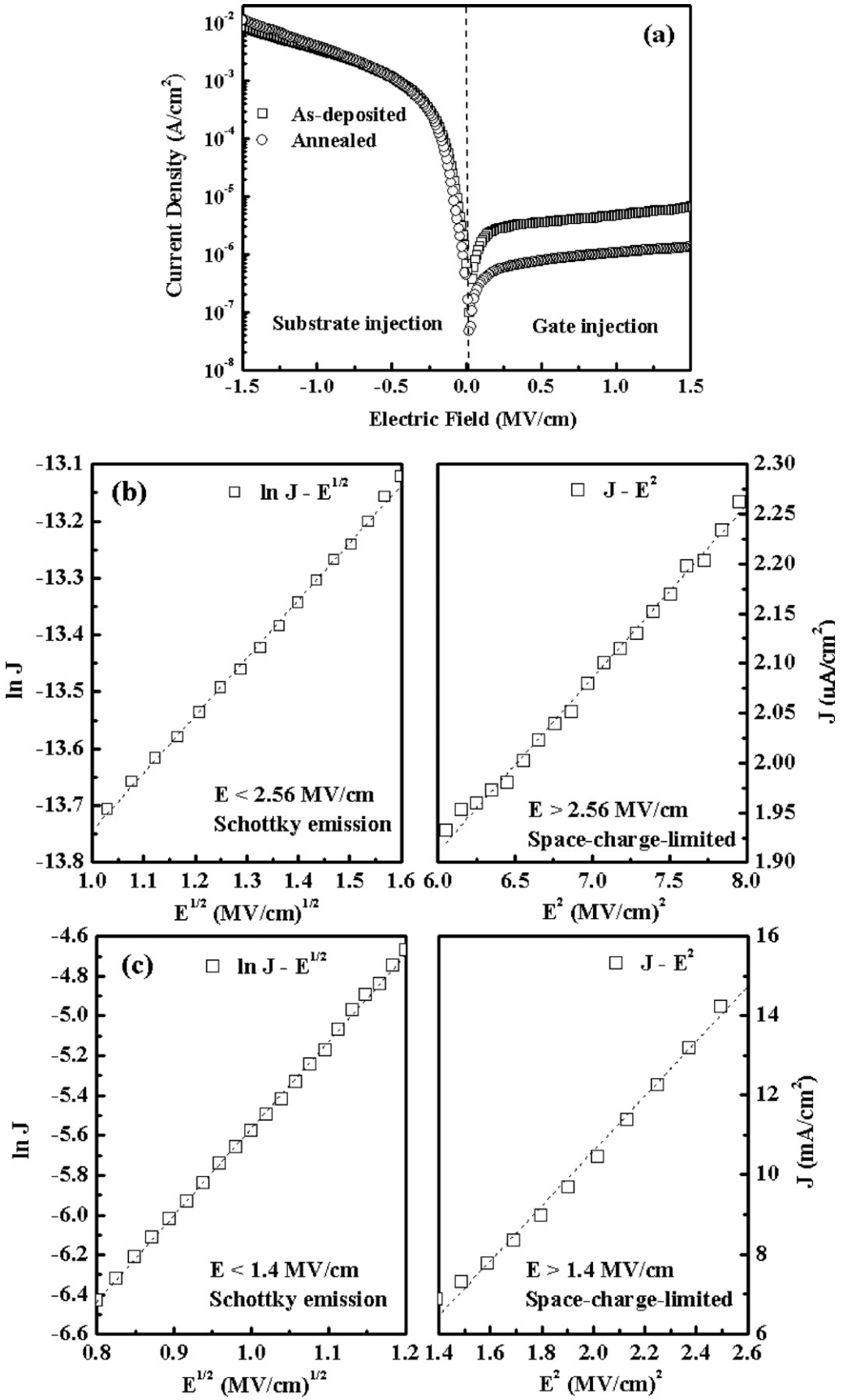

Fig. 9. (a) *J–E* profiles of MOS samples and curve fitting results in the cases of (b) positive and (c) negative bias on top Al electrode for analyzing the conduction mechanisms in the sample containing 300 °C-annealed *a*-IGZO layer.

IGZO/SiO_2 interfaces [14,15]. It can be seen that the value of J for as-deposited sample is higher than that of the annealed sample, in particular at the case of positive bias on top Al electrode. Curve fittings of J–E data were performed in order to identify the conduction mechanisms of the samples and representative results for the annealed sample are shown in Fig. 9(b) and (c). The analysis revealed the same conduction mechanisms in as-deposited and annealed samples, *i.e.*, Schottky emission at low applied bias and space-charge-limited conduction (SCLC) at high applied bias. Moreover, the curve fitting indicated the annealed sample exhibits higher threshold bias field (E_{th}) for the switching of conduction mechanism, *e.g.*, E_{th} = 1.0 MV/cm and 2.56 MV/cm for as-deposited and annealed samples, respectively, in the case of positive bias on top Al electrode whereas E_{th} = 1.2 MV/cm and 1.4 MV/cm for as-deposited and annealed samples, respectively, in the case of negative bias on top Al electrode. Presence of SCLC mechanism has been ascribed to a well-formed interface in between *a*-IGZO layer and underlying substrate [12,13]. Hence, in conjunction with the calculation of D_{it} presented previously, the high E_{th} for conduction mechanism switching observed in annealed sample iterates the beneficiary of post annealing on the remedy of interface imperfection in *a*-IGZO TFT sample.

4. Conclusions

In this work, sputtering target containing sole $InGaZnO_4$ phase was fabricated *via* a hybrid process of chemical dispersion and mechanical grinding in conjunction with the 1300 °C/6-h sintering treatment. The self-prepared target was then applied to the preparation of *a*-IGZO TFT devices and their electrical properties were investigated. Post annealing was found to improve the TFT performance that satisfactory transfer characteristics with μ_{sat} = 14.7 cm^2/V s, V_{th} = 0.57 V, *S.S.* = 0.45 V/decade and on/off ratio = 10^8 were achieved in the device containing 300 °C/1-h annealed *a*-IGZO active channel layer. Such a *a*-IGZO TFT sample also exhibited a relatively stable electrical performance as indicated by the long-term storage test. C–V and I–V analyses indicated that the device performance improvement is mainly ascribed to the reduction of trap states at *a*-IGZO/SiO_2 interface, rather than the reduction of bulk defects in the *a*-IGZO layer. Moreover, TEM and XRD revealed the *a*-IGZO layer subjected to 300 °C-annealing remains amorphous. The *a*-IGZO layer also possessed a high optical transmittance (>85%) in visible-light region that it is a promising material for the preparation of fully transparent TFTs.

Acknowledgements

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