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A calibrated direct conversion front-end transmitter with resonant matching techniques for mobile WiMAX/WiBro applications

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Abstract A direct conversion front-end transmitter with the properties of high linearity and high single sideband rejection ratio is described in this paper. The transmitter employs two resonant matching techniques to improve its operating bandwidth. The first resonant circuit design is applied at the inter-stage of the LO input buffer in order to achieve a wideband frequency response which ranges from dc to 6 GHz. The second resonant circuit is applied at the power amplifier (PA) driver output stage to increase the matching bandwidth and meet both the Worldwide Interoperability for Microwave Access (WiMAX) and Wireless Broadband (WiBro) applications simultaneously. In addition, the sideband signal and carrier leakage of this transmitter are further minimized by a proposed calibration circuit design to achieve the error vector magnitude (EVM) specifications. The measured single sideband performance with calibration mechanism demonstrates approximately 15 dB improvement on sideband and carrier suppression. The rejected sideband and carrier signals can be up to 55.19 and 56.31 dBc, respectively. The measured dynamic gain range of the transmitter is 53 dB in 1-dB step with a maximum relative gain error lower than 0.4 dB. The transmitter delivers +0.766 dBm output power with EVM of −34.687 dB for the orthogonal frequency division multiple access (OFDMA) 64QAM-3/4 modulated signals. The measured constellation is minimized to be <1.5% with output power from −2.3 to −36.2 dBm.

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1 Introduction

The tendency towards high speed and broadband wireless communication systems such as the IEEE 802.16e mobile WiMAX and WiBro systems have been developed to replace cable or DSL network [1]. The 802.16e standard technology provides high capability and long distance applications based on the OFDMA modulation technique. In comparison with the 3G and Wi-Fi applications, the mobile WiMAX has higher transmission bandwidth and higher mobility, respectively. The MIMO technique can be also applied in the WiMAX system to increase the data rate. However, the stringent linearity requirement is necessary for a WiMAX/WiBro transmitter. For example, to maintain a good communication quality, for a WiMAX OFDMA 64QAM-3/4 modulation signals, the required EVM is suggested to be lower than 2.7% [2] at the highest output power level. The greater than 50 dB wide dynamic range of the transmitter with 1 dB resolution is to support the roam application [3, 4].

This paper describes a direct conversion front-end transmitter with the characteristics of high linearity, high sideband and carrier suppression ratio, which operates between 2.3 and 2.7 GHz frequencies. The quadrature signal compensation and dc offset cancellation are obtained by the calibration circuits in a divide-by-2 circuit and an in-phase/quadrature (I/Q) modulator, respectively. The wide range of the output power is also taken into account by using the current steering method in the radio frequency variable gain amplifier (RF VGA) [5]. An over 53 dB gain change can be realized in the way of 1-dB step with a maximum relative gain error of 0.4 dB.

An RF wideband amplifier is widely used in the LO input path to provide additional voltage gain. A broadband design is essential over the entire frequency range. An inductive load with multi-bit binary weighted capacitors is one of the solutions to achieve wideband performance. However, it increases the complexity of circuit implementation. Reducing the quality factor of a loaded RLC tank is another means to extend bandwidth. Although a loaded RLC tank may have wide bandwidth and small gain variation, however, the resistive loss can cause reduced voltage gain of the entire circuit, which in turn raises the power consumption to achieve an adequate gain. An alternative solution uses inductor peaking techniques in the output of a traditional cascode topology [6–10], which allow higher speeds. In this paper, an inter-stage resonant network is proposed to incorporate in the cascode amplifier to meet a broadband specification. The resonant cascode amplifier forms an RLC tank at higher operational frequencies to boost high frequency gain. Furthermore, the topology exhibits a conventional cascode amplifier at relatively low frequencies. Consequently, the combination of high and low frequency responses achieves a wideband amplifier design.

For the output power matching, two-component matching networks, known as L-sections, are often used in the transmitter output. However, the limited bandwidth is difficult to meet the desired 400 MHz bandwidth for both the WiMAX and Wibro applications. Although multi-element matching networks translate into a wider bandwidth, passive components occupy a fairly large chip area. In this transmitter design, the PA driver's output matching network with a resonant matching scheme is proposed to gain a wider bandwidth. Because a series or shunt resonator reduces the sensitivity of the imaginary part of the reflection coefficient and forms an approximately real number, 50 ohm, as its frequency varies. Therefore, a wider output matching could be realized by this resonant technique. Furthermore, an on-chip matching network facilitates further integration with PA, even though the quality factor of the output matching network dominates the linearity of an amplifier [11].

The paper is organized as follows. Section 2 describes the transmitter architecture. The detail circuit designs of the transmitter are depicted in Sect. 3. Section 4 summarizes the measured performance. Finally, Sect. 5 concludes the paper.

2 Architecture

In the wireless communication design, the super-heterodyne [12, 13] and direct conversion (Zero IF) [14, 15] architectures are commonly used. The super-heterodyne topology suffers from the image problem such that band-pass filters are required to reject the unwanted signals. Furthermore, more circuits or external components are also required in the transmit path, which not only increase the overall complexity, but also the power dissipation, and the chip size of circuits. In contrast to the super-heterodyne method, the direct conversion architecture is suitable for low power and low cost requirements. In this transmitter design, thus, considering high integration and low power consumption requirements, the direct up-conversion architecture is chosen, as shown in Fig. 1. The transmitter is composed of a LO input buffer followed by a divide-by-2 circuit, an I/Q modulator, a three-stage RF VGA, and a PA driver. The LO input buffer serves the purpose of boosting sufficient gain in case of signal loss due to a long path with the synthesizer in layout, and also mitigate the sensitivity of the divide-by-2 circuit. The baseband signals are modulated to RF frequency by the I/Q modulator and the RF signal strength is adjusted by the following RF VGA. Finally, the PA driver enhances the output power level of the transmitter.

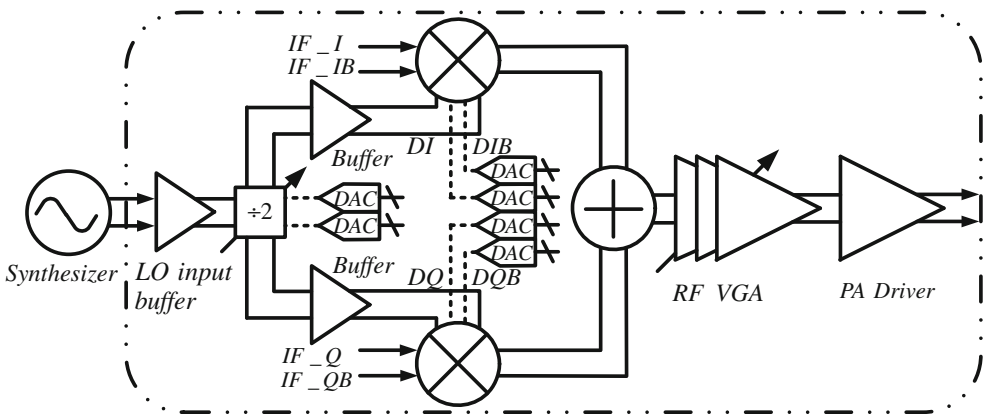

Fig. 1 Transmitter architecture

The carrier leakage, however, determined by the up-converted dc offset voltage and the direct coupling of the LO signal to the output of the I/Q modulator, is one of severe problems in the zero IF architecture. To solve this problem, the LO input buffer + divide-by-2 circuit is inputted with a synthesizer operated with doubled the LO desired frequency. In this way, the LO pulling effect can also be reduced because of the different frequencies in PA and LO signal. Accordingly, the dc offset is the main contributor of the carrier leakage. Four digital-to-analog converters (DACs) are included in the I/Q modulator to correct the dc offset voltage. For relieving process variation, calibration mechanism is also applied in the divide-by-2 circuit to obtain accurate quadrature signals.

To consider the carrier leakage, especially in low gain mode, the leakage signals are difficult to scale down with decreased output signal as the gain varies at baseband [16, 17]. The gain control range is hence all implemented at RF band because the carrier leakage in the I/Q modulator output can be attenuated through the RF VGA.

3 Circuit designs

3.1 LO input buffer

An LO input buffer, which provides enough voltage gain in front of the I/Q divider, is designed for further integration in case of a small output power from synthesizer. Moreover, for applications requiring a better sideband suppression, the LO input buffer is utilized to mitigate the degradation of single-sideband performance due to the LO signal imbalance.

To prevent direct coupling of LO signal and injection pulling [18], the frequency in the synthesizer is twice of the desired frequency. Thus, the transmitter requires a wide-band LO input buffer which gives moderate and relatively uniform gain from 4.6 to 5.4 GHz.

Figure 2 shows the proposed resonant cascode amplifier with inter-stage-matched configuration to realize a wide-band circuit. The inter-stage inductors (*LP* and *LN*) with some unavoidable parasitic capacitors from the output of common emitter stage and the input of cascode devices are inserted to form a pi type resonant network, which provides a peaking and overshoot response. The parasitic capacitors from transistors, however, are uncontrollable values, which depend on device size and dc bias. As a consequence, another capacitor, $C1$, is added to achieve an adjustable transfer function and optimize the frequency selection for bandwidth extension. Figure 3(a) shows the equivalent half circuit small signal model of the proposed LO input buffer. The R_L and C_{div2} create a low-frequency pole at the output stage. However, while the LO buffer operates at higher

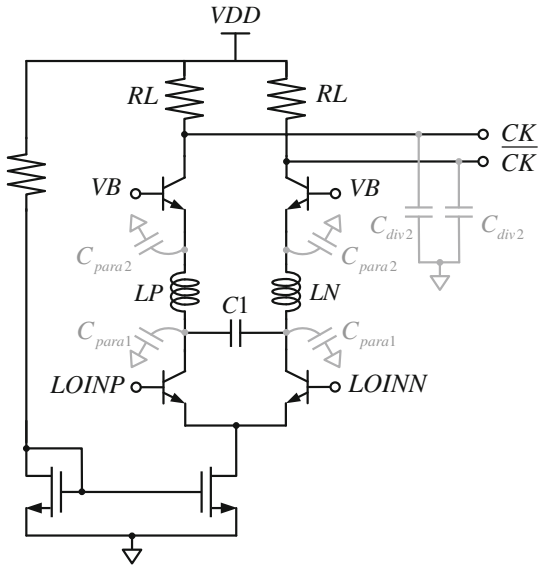

Fig. 2 Schematic of the LO input buffer with bandwidth extension technique

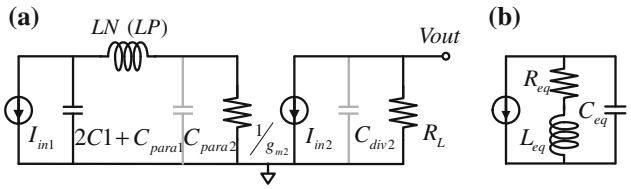

Fig. 3 **a** The equivalent half circuit small signal model of the proposed LO input buffer. **b** The equivalent model of the LO input buffer operated at relatively high frequency

frequency band, the inter-stage network with a load resistor configuration forms a resonator to compensate for higher frequency response, as illustrated in Fig. 3(b). In addition, the proposed circuit behaves like a conventional cascode topology, which can provide better isolation, higher output resistance, and sufficient voltage gain at relatively low frequency band. The simulation of the overall response, depicted in Fig. 4, exhibits a wide bandwidth characteristic with the gain flatness of less than 0.3 dB from dc to 6 GHz while the LO input buffer allows 0.36 pF loading parasitic capacitances (C_{div2}) from both the output of the cascode transistors and the input of the divide-by-2 circuit.

3.2 PA driver

Figure 5 shows the schematic of the proposed PA driver with a shunt resonator to improve its bandwidth. The key point of the design procedure is to eliminate the imaginary part of the load impedance and then to form an approximate real number of 50 ohm over an operational frequency range of 2.3–2.7 GHz.

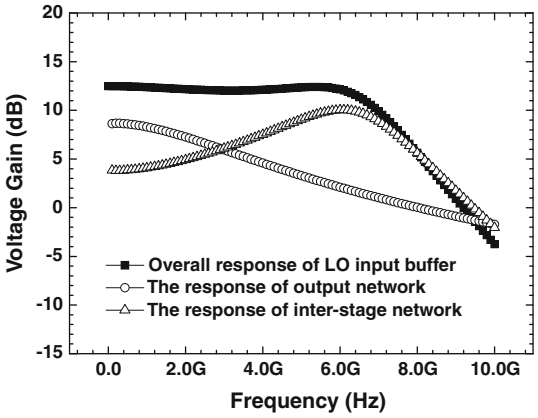

Fig. 4 Simulated voltage gain of the LO input buffer

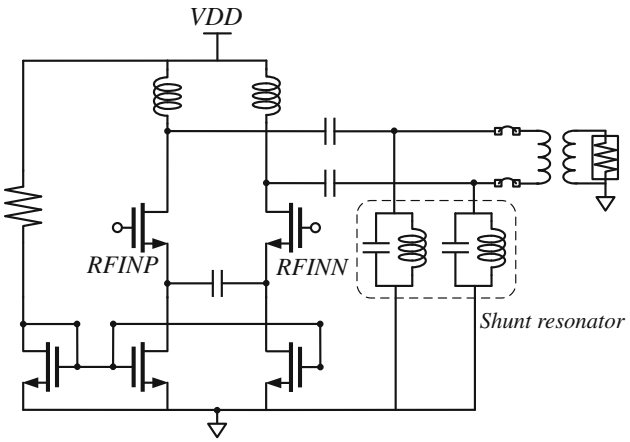

Fig. 5 PA driver with resonant matching

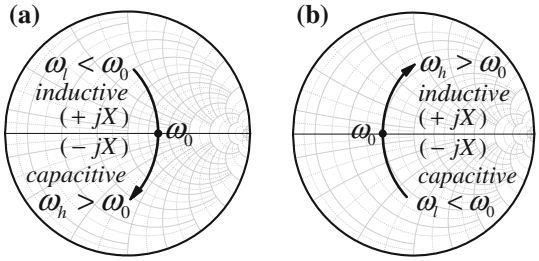

Fig. 6 Two types of the load impedance Z_L in Smith Chart **a** series resonator type and **b** shunt resonator type

The frequency response behaves a narrowband property for the case when the load impedance has inductive (jX_L) and capacitive ($-jX_L$) sections from low to high frequencies (ω_l and ω_h) in the Smith Chart, as shown in Fig. 6(a). A series resonator with $Z_R = j(\omega L - 1/\omega C)$ is thus proposed to be the output matching network. Given proper L and C values, the overall output impedance (Z_{out}) has a relative small reactance from low to high frequencies since the reactance from the series resonator and the load, (X_R and X_L), have opposite direction. The overall output impedance can be expressed as follows:

$$\begin{cases} Z_{out} = R_L + jX_L - jX_R & \text{(for lower frequency)} \\ Z_{out} = R_L & \text{(for center frequency)} \\ Z_{out} = R_L - jX_L + jX_R & \text{(for higher frequency)} \end{cases} \quad (1)$$

where the center frequency is the resonant frequency (ω_0). The inductance and capacitance from the series resonator are exploited to compensate for the capacitive and inductive sections from the load impedance, respectively. On the contrary, a shunt resonator with $Y_R = j(\omega C - 1/\omega L)$ is used, as the frequency increases from capacitive to inductive reactance, shown in Fig. 6(b). The load admittance (Y_L) reduces its imaginary part to a small value at the various frequencies because of the opposite reactance from the shunt resonator. Therefore, according to the previous analysis of the resonant matching, the series resonate matching network is used while the Smith Chart trace of a load impedance starts from inductive to capacitive region. By contrast, the shunt resonate matching network is suitable as the trace of a load admittance varies from capacitive to inductive region. Either the serious or shunt resonator brings the frequency nodes closer together, like a cross circle in the Smith Chart, so as to extend the matching bandwidth. However, an inductor with a relatively high resistance for the resonator results in a fairly small cross circle in the Smith Chart trace, which affects the matching performance. Hence, an inductor should be selected with a relatively low resistance to reduce mismatching.

3.3 I/Q divider

A divide-by-2 circuit, followed by an I/Q modulator, is employed to convert differential signals into accurate quadrature signals. However, due to the physical layout and process variation, any mismatch causes the amplitude and phase imbalance between the quadrature LO signals, which in turn further influences the single sideband performance. To minimize the I/Q imbalance, the layout should be compact and fully symmetric in an LO signal path. A larger transistor size in the divider is commonly determined to diminish current mismatch. Moreover, calibration techniques [19–22] such as pre-distortion or post-distortion are also supposed to be implemented in a transmitter chain to eliminate the sideband signal. The current mode logic (CML) divide-by-2 circuit with I/Q phase calibration mechanism, is therefore proposed to obtain the precise quadrature signals, as shown in Fig. 7. Phase mismatch can be improved by adjusting the current sources of two latches to calibrate the relative phase of the quadrature signals. As a consequence, in this transmitter design, the binary-weighted dc current sources are adopted

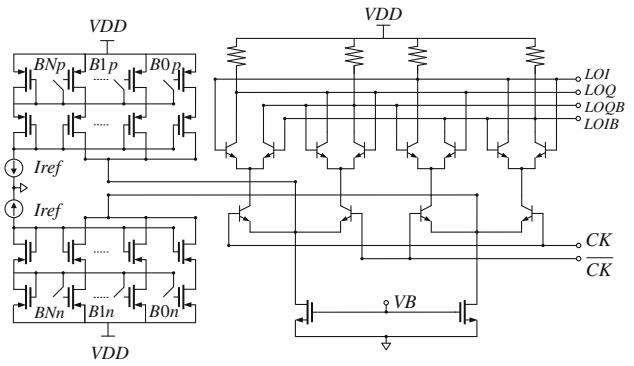

Fig. 7 Divide-by-2 circuit with I/Q phase calibration

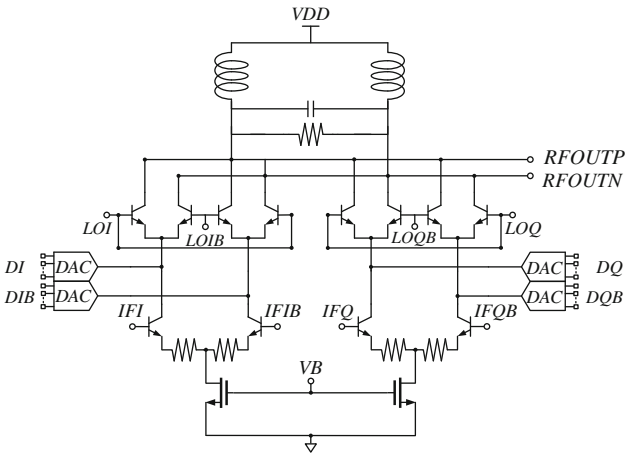

Fig. 8 I/Q modulation with 5-bit DACs

in each latch to digitally control the magnitude of the bias current. By injecting a small current into one of the latches to alter its bias current slightly, the high quadrature accuracy can be achieved, thereby enabling better sideband suppression at a desired frequency band.

3.4 I/Q modulator

An I/Q modulator is a key component for a transmitter, which is required to up-convert baseband I/Q signals directly to RF band from 2.3 to 2.7 GHz. Due to the requirement of the linearity, the I/Q modulator is configured as the double balance Gilbert mixer with resistive emitter degeneration in the transconductance stage, as depicted in Fig. 8, to handle larger baseband I/Q signals and to enhance the overall linearity.

The dc offset is a significant factor to implement the I/Q modulator. Devices and current mismatch result in dc offsets, which are up-converted to RF band and then degrade EVM performance. Therefore, the calibration circuit is essential to correct imbalances. To further calibrate the dc offsets of the I/Q modulator, four DACs are also

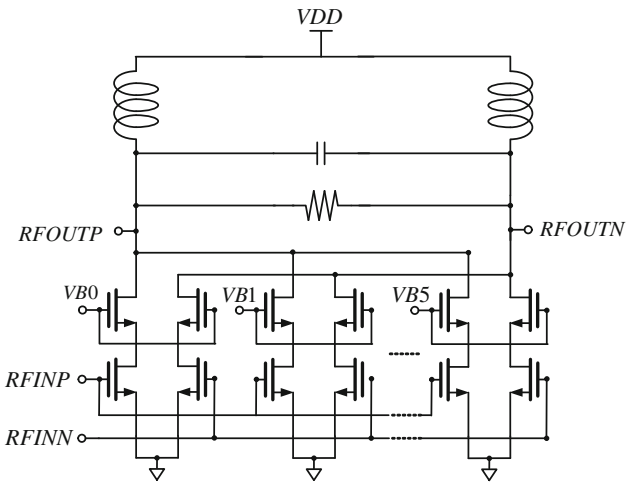

Fig. 9 Schematic of RF VGA

incorporated in the common mode node of LO switching quads by means of a digital control to perform the reduction of the carrier leakage, stemmed from the dc offsets. Moreover, larger devices are also employed in the modulator to reduce the variation in the transconductance stages as well as its corresponding tail current sources. Thanks to the calibration circuit and a well-matched layout, the carrier leakage can be suppressed substantially.

3.5 RF VGA

An RF VGA consists of three cascaded stages. Figure 9 illustrates the schematic of the first stage of the RF VGA chain with 5 dB gain control range and 1 dB resolution. The current ratio is 24:3:3:4:4:4 in six differential amplifiers, which can be controlled digitally by switching cascode transistors. Similarly, the second and third stages of the RF VGA are designed to have a 48 dB gain-tuning range with 6 dB gain steps by reducing the half of total current dissipation in each step. Consequently, a 53 dB dynamic gain range with 1 dB resolution is obtained through the RF VGA. In addition, the loaded RLC tank has a lower quality factor providing gain flatness within an acceptable level at the operating frequency band. One decoder is also used in the RF VGA to save digital gain control pins.

4 Measurement results

A direct conversion front-end transmitter for WiMAX/Wibro applications is fabricated using TSMC 0.35 μm SiGe BiCMOS technology. The die photograph of the test chip is displayed in Fig. 10. The chip occupies 4.45 mm^2 of die area, including bonding pads, and consumes 121 mA

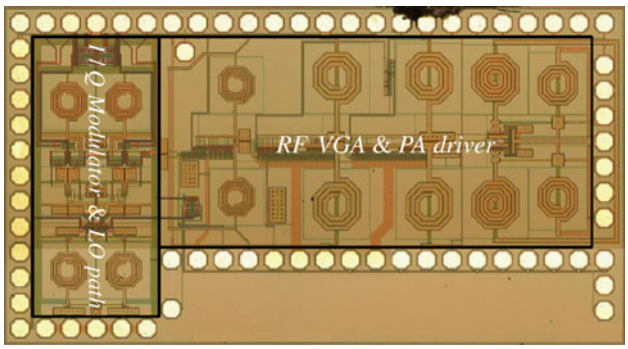

Fig. 10 Die photograph of the transmitter

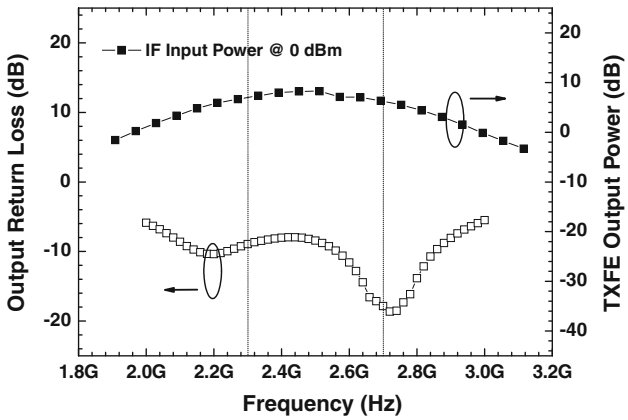

Fig. 11 Measured transmitter gain and output return loss

at the highest gain mode from a 3.3 V dc supply voltage. The chip is measured by mounting the die directly on a four layer FR-4 PCB. The signal generator generates an LO signal and base-band I/Q four phase signals, fed into the LO input buffer by an external 180° hybrid balun and I/Q modulator, respectively. The transmitter is only driven by a −15 dBm LO signal.

Figure 11 presents the full band frequency response of the measured transmitter output power with 0 dBm IF input power and output return loss. The highest transmitter gain is about 8.3 dB with gain variation of less than 2.75 dB from 2.3 to 2.7 GHz. The magnitude of reflection coefficient exhibits a broadband characteristic due to the resonant matching network in the output of the PA driver. The output return loss is less than −8 dB at the desired band. The RF VGA provides more than 53 dB gain control range with 1 dB resolution and the maximum relative gain error of less than 0.4 dB while the IF and LO input power at 10 MHz and 2.3 GHz are −10 and −15 dBm, respectively, as illustrated in Fig. 12. All the dynamic range, in the transmitter chain, is contributed by the RF VGA. For the measurement of linearity, the output 1 dB compression point (OP1 dB) is 10.63 and −36.49 dBm at the maximum and minimum gain state, respectively, as depicted in

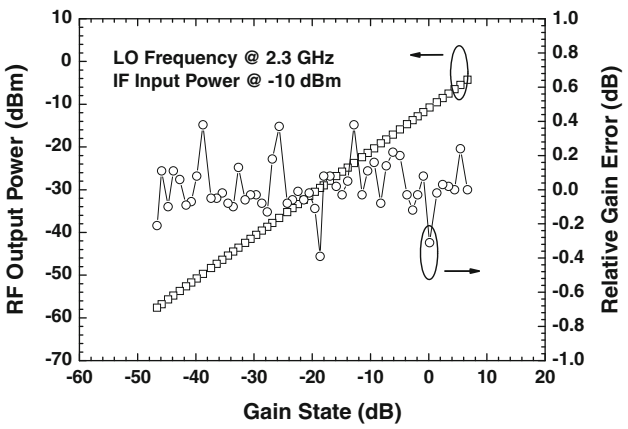

Fig. 12 Measured transmitter dynamic range and relative gain error

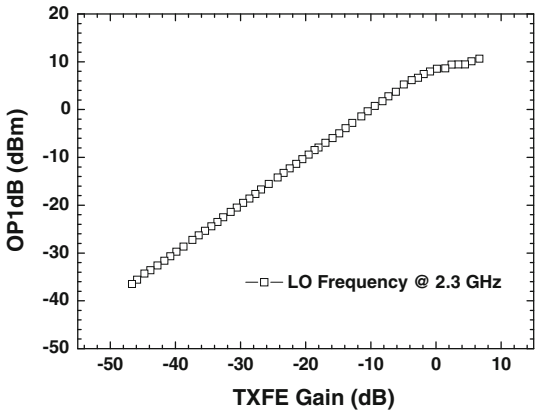

Fig. 13 Measured OP1 dB

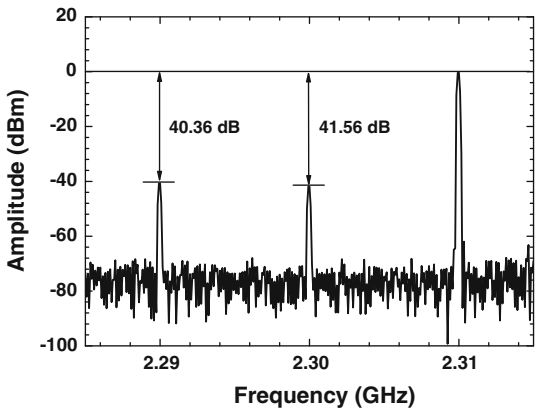

Fig. 14 Measured transmitter spectrum

Fig. 13, tested at 2.3 GHz. The OP1 dB is approximately linear with the lower gain states. For the single-sideband performance, Fig. 14 shows the measured transmitter spectrum at 2.3 GHz. Both the lower sideband and carrier can be suppressed greater than 40 dBc. The unwanted

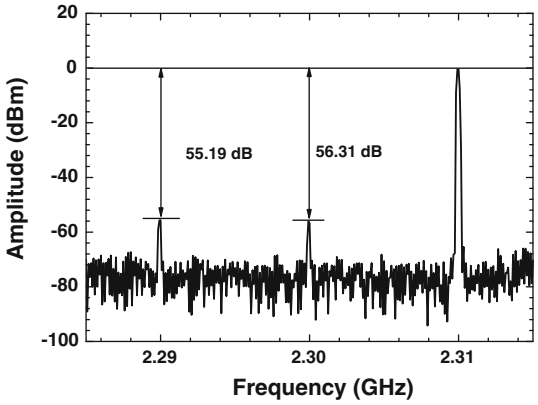

Fig. 15 Measured transmitter spectrum with calibration applied

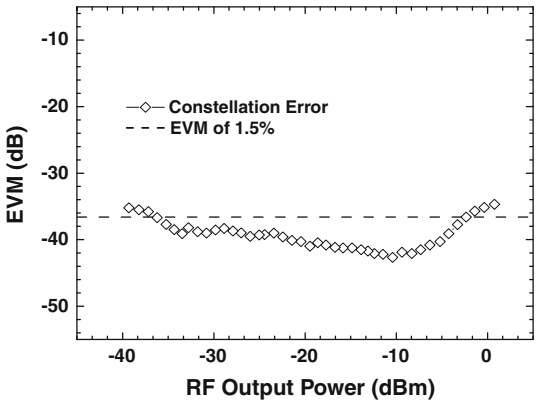

Fig. 16 Measured constellation versus RF output power

sideband and carrier signals are further rejected by the calibration circuits, which achieve 55.19 and 56.31 dBc, respectively, as shown in Fig. 15. According to the measured results, the high sideband and carrier suppression ratio reveal that the calibration techniques can not only provide excellent quadrature signals to the modulator but also balance the dc offset considerably.

The signal generator (Agilent E4438C), controlled by the Matlab code, generates the LO and baseband OFDMA 64QAM-3/4 modulated signals. The EVM performance is measured by the Agilent 89600 Vector Signal Analyzer. The measured constellation error versus RF output power, shown in Fig. 16, presents a wide dynamic range within EVM of 1.5% from −2.3 to −36.2 dBm. The EVM performance, operated at the higher output power, degrades slightly because of the nonlinear effect. The specification, however, is still met by the high linearity. The property of EVM is mainly determined by the single sideband performance at the low gain state. Therefore, the EVM of less than −38 dB can be achieved from −3.3 to −35 dBm. For the relatively low gain mode, the unwanted signals may not be suppressed as the same as the decreased gain, thereby resulting in an increase of the constellation error. Figure 17 shows the measured constellation at the highest transmitter gain. EVM of −34.687 dB is obtained with 0.766 dBm output power, which shows a good margin by the contribution of PA nonlinearity. Table 1 summarizes the measured performance of the transmitter at 2.3 GHz and compares with the prior works for WiMAX application.

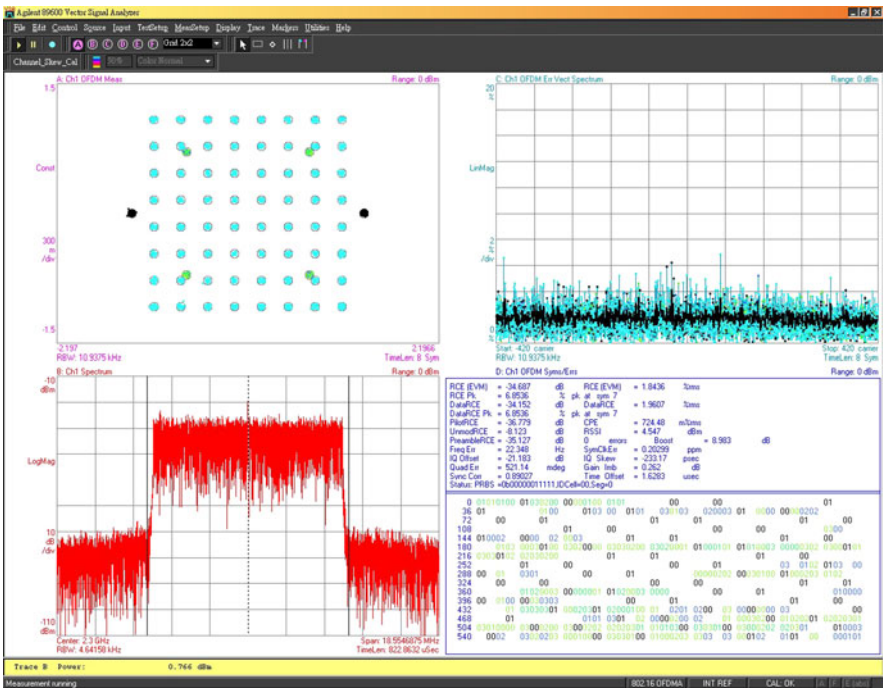

Fig. 17 Measured constellation @ highest gain

Table 1 Chip performance comparison

Ref.	Process	Frequency (GHz)	OP1 dB (dBm)	Carrier suppression (dBc)	Sideband suppression (dBc)	Gain control range (dB)	Relative gain error (dB)	EVM (dB)	P_{DC} (mW)	Chip area (mm^2)
[2]	CMOS	2.4	11	N/A	>50	50 dB/(N/A)	N/A	−36 @ Pout = −1 dBm	N/A	N/A
[3]	CMOS	5.8	N/A	28	13.7	27/2.13 dB step	<0.8 dB	N/A	149.24	2.64
[4]	CMOS	2.5	8	>30	N/A	45/1 dB step	<0.5 dB	−38 @ Pout = −2 dBm	169	N/A
[17]	CMOS	2.3	9.6	36	33	72/1 dB step	<0.5 dB	−36.6 @ Pout = −5 dBm	164	6.92[a]
[22]	BiCMOS	2.6	2.5 (OFDM)	>30	N/A	75/1 dB step	N/A	<−34 @ Pout = 1 dBm	484.4	9.4[b]
This work	BiCMOS	2.3	10.63	56.31	55.19	53/1 dB step	<0.4 dB	−34.7 @ Pout = 0.766 dBm	399.3	4.45

[a] With base-band filter

[b] Full chip with receiver and synthesizer

5 Conclusions

A calibrated direct conversion front-end transmitter with resonant matching techniques is proposed for dual mode WiMAX and WiBro applications. The resonant techniques are employed to extend the operating bandwidth in the LO input and to gain a wider matching in the PA driver's output, which cover from dc to 6 GHz and from 2.3 to 2.7 GHz, respectively. The calibration mechanisms are also incorporated to solve the problems of sideband signal and carrier leakage, which improve approximate 15 dB rejection ratio. The greater than 55 dB suppression of the single sideband performance is therefore obtained in this paper. In addition, the high linearity of the transmitter can deliver +0.766 dBm output power with EVM of −34.687 dB for the OFDMA 64 QAM-3/4 modulated signals. The transmitter demonstrates the high linearity and high single sideband rejection ratio to meet both the WiMAX and Wibro system requirements.

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