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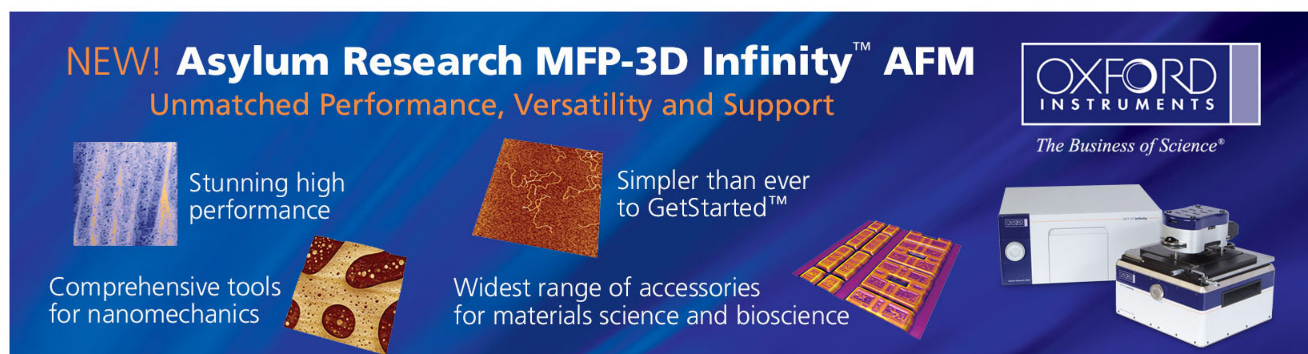

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Suppress temperature instability of InGaZnO thin film transistors by N_2O plasma treatment, including thermal-induced hole trapping phenomenon under gate bias stress

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An abnormal subthreshold leakage current is observed at high temperature, which causes a notable stretch-out phenomenon in amorphous InGaZnO thin film transistors (a-IGZO TFTs). This is due to trap-induced thermal-generated holes accumulating at the source region, which leads to barrier lowering on the source side and causes an apparent subthreshold leakage current. In order to obtain superior thermal stability performance of a-IGZO TFTs, conducting N_2O plasma treatment on active layer was expected to avert defects generation during SiO_2 deposition process. Reducing defects generation not only suppresses subthreshold current stretch-out phenomenon but also significantly improves the bias stress stability in a-IGZO TFTs at high temperature. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4709417]

Recently, there has been considerable interests in developing transparent flexible electronic devices, such as wearable computers and paper displays. The ZnO-based transistors have a great potential to be used in emerging electronic devices including thin film transistor (TFT) backplanes for flexible displays or transparent active matrix organic light-emitting diode (AMOLED) displays because they offer high mobility (>10 cm^2/V s, larger than the conventional amorphous Si TFTs with a low mobility of 1 cm^2/V s),[1] excellent uniformity (compared with polycrystalline Si TFTs), and good transparency to visible light.[2] Furthermore, devices fabrication at low temperature is also attractive for transparent flexible displays. Although oxide-based TFTs have shown high performance, some issues have to be researched and overcome, including environment gas, light, and thermal instability. In previous studies, only the instability caused by environment gas[3–7] and light issue[8,9] have been proposed as critical issues in the application of display industry. In this study, we investigate the thermal-instability caused by trap-induced thermal-generated hole accumulation at the source region, which leads to source side barrier lowering and causes an apparent subthreshold leakage current. In order to suppress the abnormal subthreshold leakage current, we developed a N_2O-plasma treatment to protect the active layer from generated defects during passivation (SiO_2) deposition process. Furthermore, the trap-induced thermal-generated hole trapping effect is suppressed to improve the negative bias stress stability in amorphous InGaZnO thin film transistors (a-IGZO TFTs) at high temperature.

Bottom gate coplanar a-IGZO TFTs were produced on glass substrate in this work. The plasma enhanced chemical vapor deposition (PECVD)-derived SiO_x (300 nm) film as gate insulator was grown at 370 °C, over the patterned Ti/Al/Ti trilayer gate electrodes. The Ti/Al/Ti source/drain electrodes were formed by sputtering and then patterned into the dimension of channel width (W) from 5 μm to 30 μm and with channel length (L) of 10 μm. A 30 nm thick a-IGZO film was deposited by dc magnetron sputtering system at room temperature, using a target of In:Ga:Zn = 1:1:1 in atomic ratio, a plasma discharge power of 300 W, and an ambient gas mixture of O_2/Ar at the ratio of 6.7% with a working pressure of 5 mTorr. After defining the active region, one group of the TFTs was treated by N_2O plasma on the channel surface of the a-IGZO active layer. Finally, all of device were capped with a 200 nm SiO_X layer by PECVD, and sequentially annealed in an oven at 330 °C for 2 h. The electrical properties of a-IGZO TFTs were analyzed using Agilent B1500A semiconductor device analyzer in dark.

Figure 1(a) shows the transfer characteristics of as-fabricated a-IGZO TFTs at the different temperatures between 300 K and 450 K. As seen in this figure, the I-V curves shift to the negative direction and drain current (I_D) raises with increasing temperature. The threshold voltage (V_T) is determined while the normalized drain current ($NI_D = I_D \times L/W$) reaching 10^{-10} A, and the delta threshold voltage is determined by subtracting the V_T at the higher temperature by that at 300 K. Below 375 K, the V_T decreases proportionally with increasing temperature as shown in Fig. 1(b). It is well known for oxide semiconductors that the free electrons in the materials are mainly due to the generation of oxygen vacancies.[10,11] Thermally excited oxygen atoms that leave their original sites move into the interstitial sites and cause vacancies with remaining free electrons at the corresponding sites. The lower threshold voltage observed at higher temperatures can be attributed to these free electrons generated along with the oxygen vacancies.[12,13]

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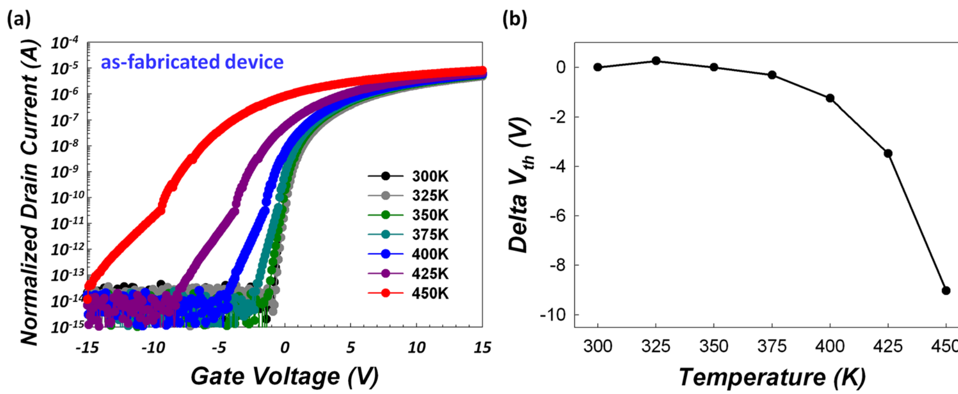

FIG. 1. (a) I_D-V_G curves of as-fabricated a-IGZO TFTs at the different temperatures. (b) The corresponding threshold voltage shift with the different temperatures.

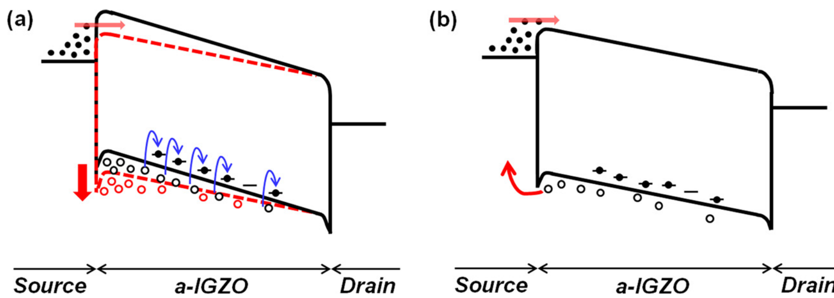

FIG. 2. The energy band diagrams of proposed mechanisms for these two distinctive regions: (a) the gate voltage is below V_T and (b) the gate voltage is above V_T.

Furthermore, the stretch-out phenomenon gets more serious with increasing temperatures. The stretching of transfer curves, indicating abnormal subthreshold leakage current, is significantly observed at 400 K. On the other hand, this temperature effect is reversible. The transfer characteristics at room temperature (300 K) can be restored after the high temperature measurements.

Next, we discuss the unique behavior of the subthreshold leakage current for a-IGZO TFTs at high temperature. The transfer characteristics can be separated into stretch-out and normal regions by threshold voltage shown in Fig. 1(a). The mechanisms for these two distinctive regions are proposed in Fig. 2. As shown in Fig. 2(a), when the gate voltage is below V_T, the trap-induced thermal-generated holes move to the source side due to the transverse electric field. Then, the holes accumulated at the source region lead to barrier lowering. The source side barrier lowering enhances electrons injection from the source and causes an apparent subthreshold leakage current. As for the normal region where $V_G > V_T$, the transfer characteristics are dominated by the barrier between the a-IGZO and source. The holes accumulated near the source side would flow to the source when the a-IGZO TFTs turned on. The barrier height becomes much lower with the increased gate voltage, which prohibits the accumulation of holes at the source side, as shown in Fig. 2(b). Therefore, the transfer curve separates into two regions at high temperature.

The subthreshold leakage current stretch-out phenomenon is observed at high temperature due to thermal-induced holes generation from defects. In order to improve the thermal stability of a-IGZO TFTs, we developed a N_2O-plasma treatment method, which suppressed the subthreshold leakage current at high temperature as shown in Fig. 3(a). Compared with as-fabricated a-IGZO TFTs, the curves only slightly shifted to the left with increasing temperature. Also, the subthreshold leakage current stretch-out phenomenon was significantly suppressed at high temperature. For as-fabricated devices, the passivation layer deposition process

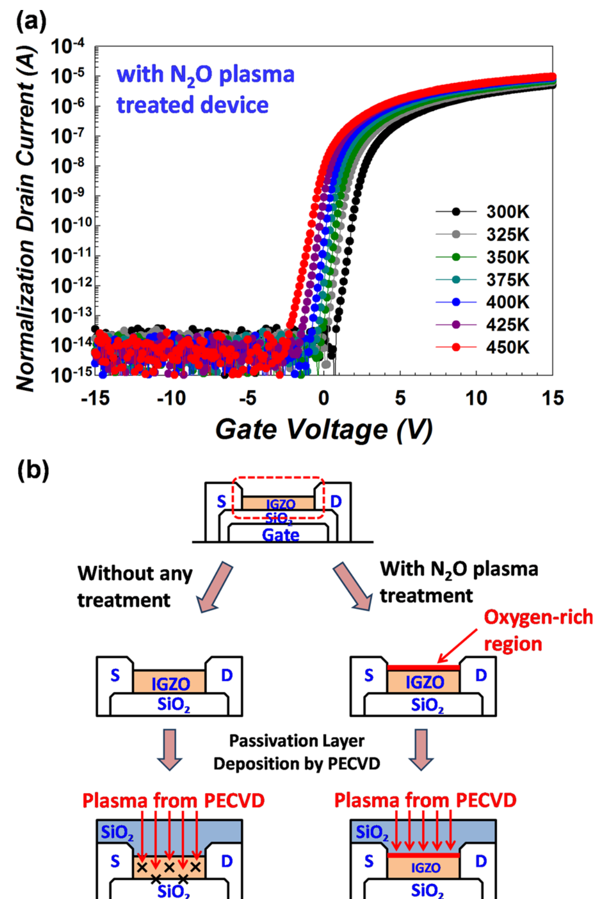

FIG. 3. (a) I_D-V_G curves of N_2O plasma treatment a-IGZO TFTs at the different temperatures. (b) Schematic passivation layer deposition process of as-fabricated and N_2O plasma treatment devices.

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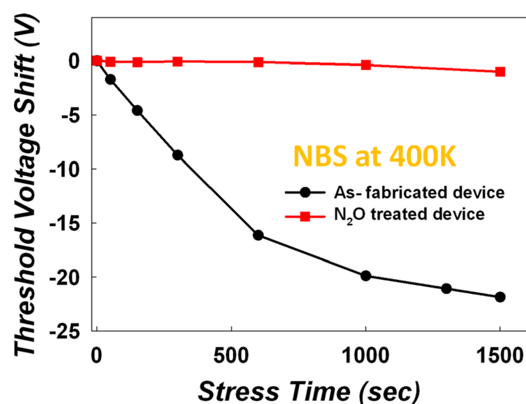

FIG. 4. Threshold voltage shift under negative gate bias at 400 K with as-fabricated and N_2O plasma treatment devices.

as shown in Fig. 3(b), which used PECVD system, could cause extra defects due to PECVD plasma damage[14] and results in significant subthreshold leakage current stretch-out phenomenon at high temperature. On the contrary, for N_2O-plasma treatment devices, N_2O-plasma treatment is applied to a-IGZO active layer. An oxygen-rich region is formed near the back channel by the N_2O-plasma treatment, which effectively prevents damages in the active layer during SiO_2 deposition process.[15,16] It implied that N_2O-plasma treatment could enhance the atomic bonding strength, which suppresses defect generation during SiO_2 deposition process. Therefore, the subthreshold leakage current can be reduced significantly because the lack of defects cannot induce enough thermal-generated holes to lower the source side barrier.

In order to confirm that the N_2O plasma treatment can effectively reduce defects generation during SiO_2 deposition process, the negative bias temperature stress (NBTS) experiment is conducted with $Vg = -30\,V$ at 400 K for as-fabricated and N_2O plasma treatment devices. The V_T was measured before and after NBTS. The V_T shift (ΔV_T) is plotted against stress time in Fig. 4. For as-fabricated devices, the V_T shifts towards the negative direction significantly in the experiment. At high temperature, the thermal-generated holes from defects are accumulated by the negative gate voltage and trapped in the gate dielectric or at the dielectric/channel interface. The trapped holes then induce more electrons to shift V_T negatively with stress time. For N_2O plasma treatment devices, the ΔV_T hardly shifts under negative gate bias stress. It again suggested that N_2O plasma treatment can reduce defects generation during SiO_2 deposition process and further suppress the trap-induced thermal-generated holes at high temperature. Therefore, N_2O plasma treatment, which is applied to a-IGZO active layer, can significantly enhance the bias stress stability of a-IGZO TFTs at high temperatures.

The transfer curve exhibits an apparent subthreshold current stretch-out phenomenon, which becomes more serious with increasing temperatures. In order to obtain superior thermal stability performance of a-IGZO TFTs, N_2O plasma treatment on active layer was expected to avert defect generation during SiO_2 deposition process. The a-IGZO TFTs with N_2O plasma treatment can effectively reduce defect generation to suppressed subthreshold current stretch-out phenomenon and improve the bias stress stability of a-IGZO TFTs at high temperatures.

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