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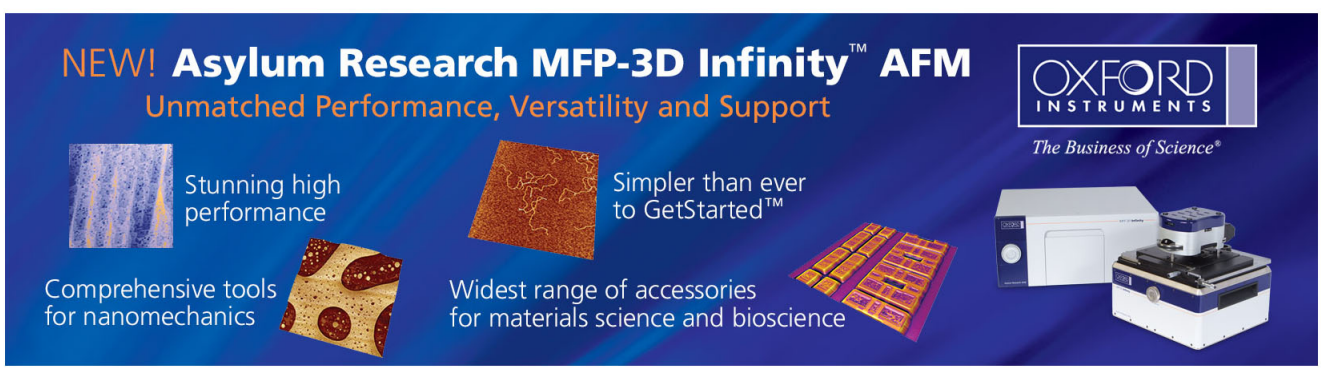

Electrical and reliability characteristics of polycrystalline silicon thin-film transistors with high-κ Eu_2O_3 gate dielectrics

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In this study, we developed a high-performance low-temperature polycrystalline silicon thin-film transistor (LTPS-TFT) incorporating an ultra thin Eu_2O_3 gate dielectric. High-κ Eu_2O_3 LTPS-TFT annealed at 500 °C exhibits a low threshold voltage of 0.16 V, a high effective carrier mobility of 44 cm^2/V-s, a small subthreshold swing of 142 mV/decade, and a high I_{on}/I_{off} current ratio of 1.34×10^7. These significant improvements are attributed to the high gate-capacitance density due to the adequate quality of Eu_2O_3 gate dielectric with small interfacial layer of effective oxide thickness of 2.5 nm. Furthermore, the degradation mechanism of positive bias temperature instability was studied for a high-k Eu_2O_3 LTPS-TFT device. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4705472]

Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) are known as attractive candidates for active matrix liquid-phase crystal display panel, three-dimensional (3-D) circuit integration, and system-on-panel (SOP) applications.[1–3] The ultra-thin SiO_2 (<2 nm) is inevitable to excessive leakage current due to the direct tunneling.[4] A low dielectric constant and high leakage current of thin SiO_2 gate oxide in complementary metal-oxide-semiconductor (CMOS) devices hinder it to be used in low power and high performance applications. In contrary, high-κ gate dielectrics can significantly reduce the gate leakage current for a given effective oxide thickness (EOT) and increase the gate capacitance density, causing high performance in LTPS-TFT. Rare-earth oxide materials, such as La_2O_3,[5] CeO_2,[6] and Dy_2O_3,[7] have been recently studied extensively as promising gate dielectrics in advanced CMOS technology due to their high permittivity, large energy bandgap, and high thermodynamic stability with Si.[8] Although many research efforts have been explored to improve the electrical performance of TFT devices,[9,10] few investigations have been conducted on the positive bias temperature instability (PBTI) in high-κ gate oxide LTPS-TFTs, and the mechanism of bias and temperature induced instabilities in the TFT devices is still not clear. In this paper, a high-performance LTPS-TFT device incorporating a high-κ Eu_2O_3 gate dielectric is demonstrated. Furthermore, the most important bias temperature instabilities are investigated in high-κ Eu_2O_3 LTPS-TFTs.

The n-channel LTPS-TFTs were fabricated on 6-in. Si substrates. A 500 nm-thick SiO_2 was grown on the Si wafer by a standard wet oxidation process. A 50 nm-thick undoped amorphous-Si (α-Si) layer was deposited on SiO_2 using low-pressure chemical vapor deposition at 550 °C. The deposited α-Si layer was then re-crystallized by the solid-phase-crystallization (SPC) process at 600 °C for 24 h in N_2 ambient. The phosphorous ion implantation was done with an energy of 80 keV and a dose of 5×10^{15} cm^{-2} to define source/drain (S/D) regions. The implantation was activated by the thermal treatment at 600 °C for 12 h. The Eu_2O_3 gate dielectric (~2.4 nm) was deposited on the polycrystalline silicon film by electron-beam evaporation method, followed by thermal annealing at 500 and 600 °C for 30 min in N_2 ambient to improve the gate dielectric quality. An interfacial layer (~2 nm) was observed between poly-Si film and Eu_2O_3 dielectric, which was confirmed by cross section TEM image in Fig. 1(a). Subsequently, Eu_2O_3 film was removed in the S/D regions by dry etching system. Finally, 300 nm-thick Al was deposited by physical vapor deposition to pattern the gate and S/D electrodes. The schematic cross-sectional view of the Eu_2O_3 LTPS-TFT device structure was shown in Fig. 1(b). The threshold voltage (V_{TH}) was defined as the gate voltage at which the drain-current reaches 100 nA·W/L at $V_{DS} = 0.5$ V. The field effect mobility (μ_{FE}) is derived from the value of maximum transconductance of the TFT device.

The well-behaved I_{DS}–V_{GS} transfer characteristics of the high-κ Eu_2O_3 LTPS-TFT devices annealed at 500 and 600 °C are shown in Fig. 2. The TFT device annealed at 500 °C exhibits high performance, including a very low V_{TH} of 0.16 V, a high field effect mobility (μ_{FE}) of 44 cm^2/V-s, and a small subthreshold swing (S.S.) of 142.2 mV/decade, compared with the device annealed at 600 °C. This may be attributed to the superior gate dielectric and low interface trap density at the dielectric/poly-Si interface.[11] In addition, these devices show a low gate-induced drain leakage current of $\sim 10^{-12}$ A. The EOT and the dielectric constant (κ) of Eu_2O_3 film annealed at 500 °C were evaluated as ~2.5 nm and 19, respectively, corroborated well with the above results. The I_{on}/I_{off} value of 1.34×10^7 in the LTPS-TFT device annealed at 500 °C is larger than that of device annealed at 600 °C (8.44×10^6). The positive threshold voltage shift in these LTPS-TFT devices can be ascribed by the interfacial electron trapping due to the presence of an unrestrained silicate layer at the dielectric/poly-Si interface.[12,13] For the

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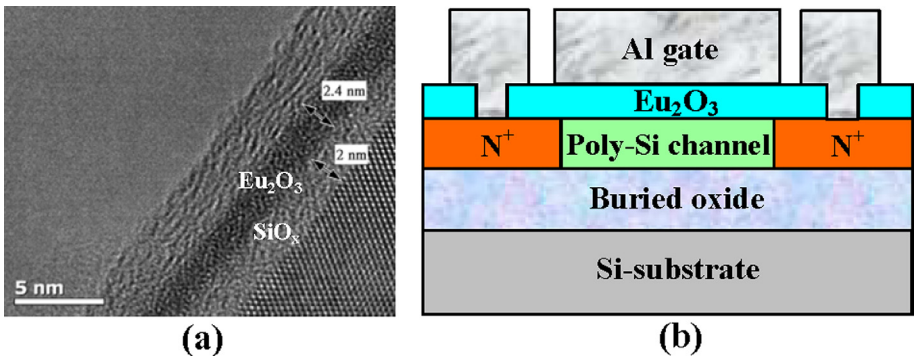

FIG. 1. (a) TEM cross-sectional image of the stacked Eu_2O_3/SiO_x gate dielectric annealed at 500 °C and (b) cross-sectional view of the high-κ Eu_2O_3 LTPS-TFT device structure.

Eu_2O_3 film annealed at 600 °C, a higher V_{TH} shift was observed. This behavior may be due to the formation of thicker silicate layer at the oxide/poly-Si interface.[14]

Figure 3 shows the output characteristics (I_{DS}–V_{DS}) of the high-κ Eu_2O_3 LTPS-TFTs annealed at 500 and 600 °C. It can be seen that the driving current of LTPS-TFT device annealed at 500 °C increases significantly compared to that of device annealed at 600 °C. The plausible mechanism may be the higher field effect mobility of charge carrier and the smaller threshold voltage of the device. The high driving current would be very promising for the application of SOP and 3-D circuit integration. The important device parameters of Eu_2O_3 dielectric incorporated LTPS-TFTs are listed in Table I. An improvement in device performance is observed compared with other recently published works with different gate dielectrics including SiO_2,[15] Y_2O_3,[16] HfO_2,[17] and Pr_2O_3.[18] The Eu_2O_3 LTPS-TFT can speedily fill the trap states at the grain boundary and fast turn on the device due to the ultra thin EOT and large gate capacitance density.[17]

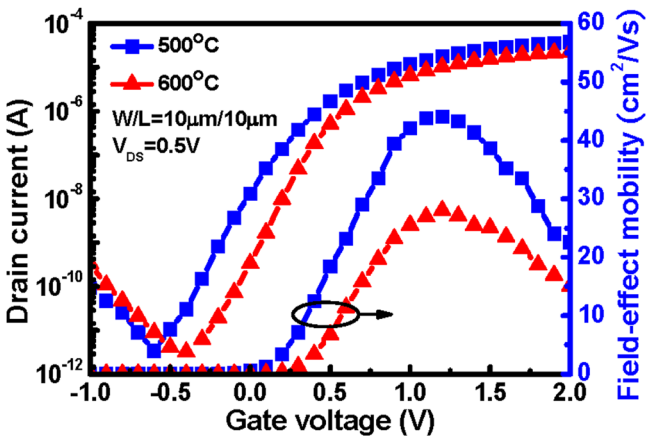

FIG. 2. Transfer characteristics (I_{DS}–V_{GS} and μ_{FE}) of the Eu_2O_3 LTPS-TFT devices annealed at 500 and 600 °C, measured at $V_{DS} = 0.5$ V.

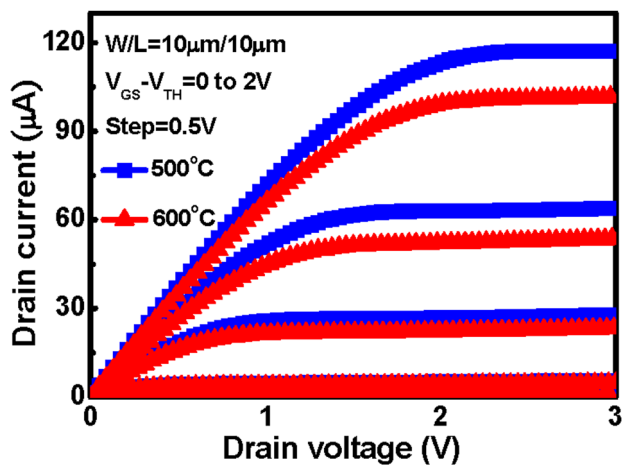

FIG. 3. Output characteristic I_{DS}–V_{DS} of high-κ Eu_2O_3 LTPS-TFT devices annealed at 500 and 600 °C.

The bias temperature instability of the high-κ Eu_2O_3 LTPS-TFT device is investigated under 25 and 85 °C. A dc voltage in the range between 1.5 and 2 V was applied to the gate with the source and drain grounded. Fig. 4(a) shows the threshold voltage shift of the high-κ Eu_2O_3 LTPS-TFT device under constant voltage stress (CVS) for different conditions. The turn-around phenomenon was observed for 1.5 V stress voltage at 25 °C. The injected electrons from substrates are trapped in the interfacial layer without Si-O bonds breaking, which cause the positive V_{TH} shifts. This phenomenon can be interpreted by the modified reaction-diffusion model based on electric stress induced defect generation mechanism.[19] After 100 s of CVS, the threshold voltage shift direction switches from positive to negative with increasing stress time, suggesting the electron detrapping from Eu_2O_3 film. On the other hand, the PBTI measurement shows that a larger stress gate voltage leads to a more severe degradation in the V_{TH} shift, which indicates that bias temperature instabilities for high-κ Eu_2O_3 LTPS-TFT are electrically activated. Fig. 4(b) shows the effect of PBTI stress on the transfer characteristics of the n-channel LTPS-TFTs. It was found that the V_{TH} value changes from positive to negative after PBTI stress, indicating that the PBTI stress generates more positive interface trap states in the device. In addition, the field effect mobility degrades after the PBTI stress. For positive bias stress, the accelerated electrons would break the weak grain boundary bonding, resulting in a large

TABLE I. Comparison of device parameters for LTPS-TFTs fabricated with a SiO_2, Y_2O_3, HfO_2, Pr_2O_3, and Eu_2O_3.

	SiO_2	Y_2O_3	HfO_2	Pr_2O_3	Eu_2O_3
W/L	10/10	10/5	0.1/1	10/10	10/10
V_{TH} (V)	12	1.76	0.3	1.58	0.16
S.S. (mV/decade)	2060	269	280	276	142.2
EOT (nm)	50	8.6	7.3	6.5	2.51
μ_{FE} (cm^2/V-s)	11	32.7	39	28.33	44.07
I_{on}/I_{off}	4.65×10^6	1.83×10^7	9.7×10^6	3.9×10^6	1.34×10^7

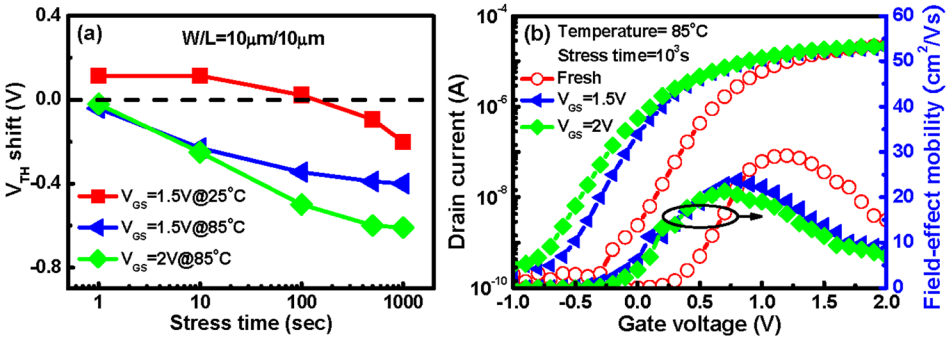

FIG. 4. (a) Threshold voltage shift as a function of stress time for high-k Eu_2O_3 LTPS-TFT devices annealed at 500 °C under various positive biases and temperatures. (b) Transfer characteristics of the high-κ Eu_2O_3 LTPS-TFT device before and after PBTI stress.

number of defects into the poly-Si channel film and/or the interfacial layer to generate the oxygen vacancy (V_O^{2+}) and interstitial oxygen (I_O^{2-}).[20] The V_O^{2+} would accumulate in the interfacial layer and the I_O^{2-} would diffuse/drift into Eu_2O_3 bulk under positive bias, as shown in Fig. 5(a). The V_O^{2+} is a shallower defect compared with the V_O^0 in the energy-band diagram, as illustrated in Fig. 5(b). This negative shift may be attributed to electron de-traps from deep level I_O^{2-}, possibly indicating that it occupied at a lower level than the work function of Al. Under PBTI stress, the electron de-trap film in the Eu_2O_3 is dominant than electron trapping.

In summary, a high-performance LTPS-TFT device featuring an ultra thin Eu_2O_3 gate dielectric is demonstrated. High μ_{FE}, low V_{TH}, large I_{on}/I_{off}, and excellent S.S. are achieved in the n-channel poly-Si LTPS-TFT due to the adequate quality of the gate dielectric with some unrestrained silicate layer served as stacked gate dielectric. Consequently, it is very promising for the application of SOP technology due to the high electron mobility of the device. In addition, the mechanism of PBTI in high-κ Eu_2O_3 LTPS TFT is investigated. PBTI may be attributed to the creation of defects in poly-Si TFT channel by breaking of Si–O bonds at the grain boundaries and/or the interfacial layer between

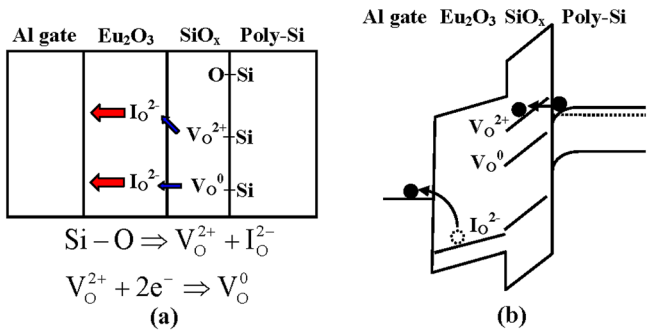

FIG. 5. (a) Modified reaction-diffusion model and (b) energy-band diagram of the high-κ Eu_2O_3 LTPS-TFT device under PBTI stress.

Eu_2O_3 and poly-Si film, and thus, the oxygen ions or vacancies will diffuse/drift into the Eu_2O_3 film to degrade the device performance.

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