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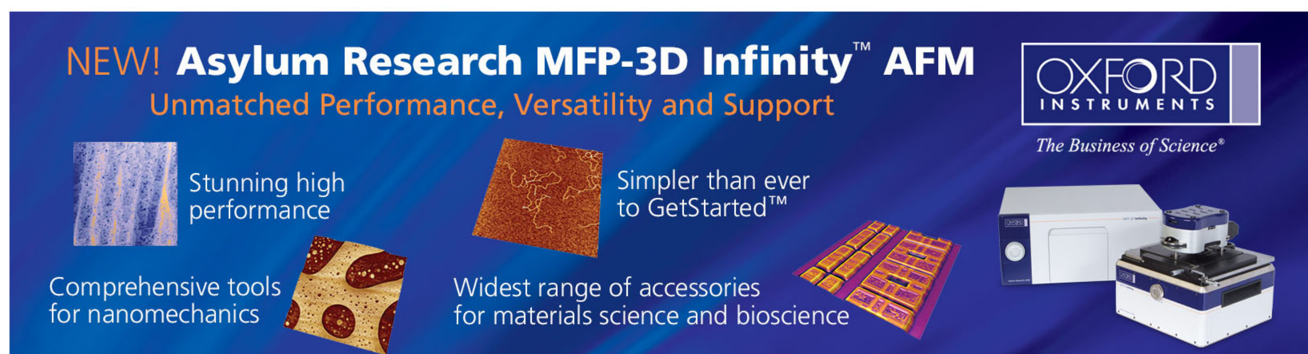

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Charge trapping induced drain-induced-barrier-lowering in HfO_2/TiN p-channel metal-oxide-semiconductor-field-effect-transistors under hot carrier stress

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This letter studies the channel hot carrier stress (CHCS) behaviors on high dielectric constant insulator and metal gate HfO_2/TiN p-channel metal-oxide-semiconductor field effect transistors. It can be found that the degradation is associated with electron trapping, resulting in G_m decrease and positive V_{th} shift. However, V_{th} under saturation region shows an insignificant degradation during stress. To compare that, the CHC-induced electron trapping induced DIBL is proposed to demonstrate the different behavior of V_{th} between linear and saturation region. The devices with different channel length are used to evidence the trapping-induced DIBL behavior. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3697644]

The physical limitation of the silicon dioxide (SiO_2) as gate insulator has achieved the point where its thickness is approaching to a few atomic layers thick.[1,2] Below the physical thickness 12 Å, the significant gate leakage current results in a volume active power consumption, leading a worse reliability of metal-oxide semiconductor field effect transistors (MOSFETs). To avoid this serious issue, high-k dielectrics have been introduced as hafnium (Hf)-base, zirconium, aluminum oxides[3–6] and heavily investigated as a replacement for conventional SiO_2 gate insulator. However, high-k/metal gate stack has to face many critical issues such as defects in high-k material which can lead to undesired transport through the dielectrics and trapping-induced instabilities.[7–10] As MOSFETs scaling down, not only the BTI reliability at gate terminal but also hot carrier effect (HCE) which is associated with lateral electric field is important issue in MOSFETs. Therefore, hot carrier effect in high-k/metal gate n-MOSFETs was still one of major device reliability concern. As is well known, under hot carrier injection, a high lateral electric field in pinch-off region accelerates the electrons sufficiently to gain enough energy to damage the drain side, resulting in the degradation of I-V characteristics. However, most of the studies were concentrated on n-MOSFETs.[11–14] The degradation due to hot carrier effect in p-MOSFETs with high-k/metal gate stacks has not received as much attention. Therefore, the aim of this letter is to investigate the effects of channel hot carrier stress (CHCS) on HfO_2/TiN p-MOSFETs. It was found that the CHC-induced electron trapping dominates the degradation during stress, instead of interface states (N_{it}) creation, including V_{th} shift and G_m decrease. As the drain voltage (V_D) was applied at saturation region, there is no significant V_{th} shift during stress. This behavior was doubted to result from trapping-induced drain-induced-barrier-lowering (DIBL). To explain this phenomenon, the device with different channel length (L) was introduced to support our model in this work.

The HfO_2/TiN p-MOSFETs were studied in this paper based on the high-performance 28-nm CMOS technology. Both devices were fabricated using a conventional self-aligned transistor flow through the gate first process. For the gate first process devices, 10 Å and 30 Å of high quality thermal oxide were, respectively, grown on a (100) Si substrate as buffer oxide layers. After standard cleaning procedures, 30 Å of HfO_2 films were sequentially deposited by atomic layer deposition. Next, 10 nm of TiN films were deposited by radio frequency physical vapor deposition, followed by poly-Si deposition as a low resistance gate electrode. The source/drain and poly-Si gate activation were performed at 1025 °C. In this study, the dimensions of the selected devices were 10 μm and 1 μm in width and length, respectively. The device with buffer thickness of 10 Å was subjected to the maximum substrate current of CHCS conditions with −3.6 V drain voltage (V_D). The stress was briefly interrupted to measure the drain current-gate voltage (I_D-V_G) and substrate current-gate voltage (I_B-V_G) transfer characteristics. The gate induced drain leakage (GIDL) current was defined under the $V_G = 0.5$ V and $V_D = -2.4$ V. All experimental curves were measured using an Agilent B1500 semiconductor parameter analyzer.

Figure 1 shows the drain current (I_D) curve versus gate voltage (V_G) and corresponding transconductance (G_m) of HfO_2/TiN p-MOSFETs under CHCS. The stress condition V_G was selected at the maximum substrate current (I_{Bmax}) of CHCS conditions while $V_D = -3.6$ V. As the result, the degradations on device during CHCS show decrease and positive shift in transconductance (Gm) and threshold voltage

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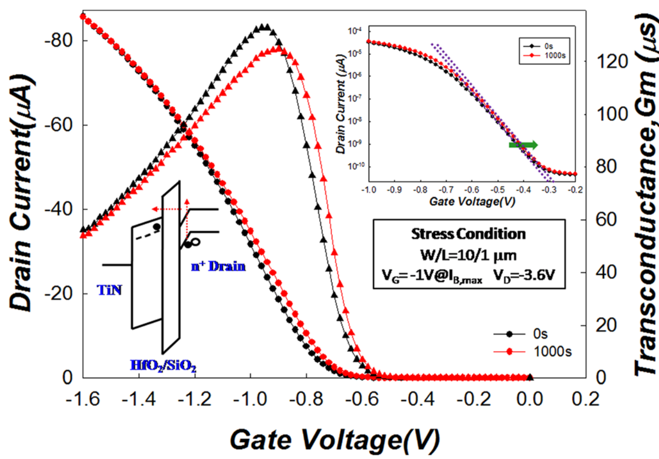

FIG. 1. I_D-V_G and corresponding G_m-V_G transfer characteristic curves of HfO_2/TiN p-MOSFETs before and after stress. The inset shows the comparison of subthreshold slope in log I_D-V_G under CHCS and the energy diagram of CHC-induced trapping.

(V_{th}), respectively. And I_D seems to be invariant at $V_G = -1.6$ V. Generally, the behavior of CHC effect on n-MOSFETs has a cruel degradation at drain side due to impact ionization, decreasing in I_D and G_m, but V_{th} shift is insignificant unless N_{it} generation due to higher lateral electric field during CHCS, respectively.[15] However, the V_{th} shift toward positive direction is obtained under CHCS for high-k/Metal gate p-MOSFETs as shown in Fig. 1. We suggest that V_{th} shift and decrease in G_m could result from electron trapping in high-k layer during stress. When electron-hole pairs are produced by impact ionization, the stressing potential difference between gate and drain (V_{GD}) makes electron tend to inject to gate side, resulting in V_{th} shift. Simultaneously, the field-effect mobility (G_m) is also influenced by charge trapping, enhancing the channel scattering.[16–18] However, V_{th} shift due to electron trapping should make I_D increasing, but the scattering reduces the channel-mobility and decreases I_D. Because those two causes are antagonistic in I_D then resulting an invariant in I_D. Additionally, the inset of Fig. 1 shows the I_D-V_G curve under semi-logarithmic scale before and after CHCS. It can be found that the degradation of subthreshold slope (SS) is insignificant, illustrating the N_{it} is less. Therefore, this result supports our assumption that the degradation of V_{th} is induced by electron trapping in high-k layer located at drain side, instead of CHC-induced N_{it}. In order to solid the claim, the effect of CHCS on the characteristics of I_B-V_G and I_D-V_G measured at $V_D = -2.4$ V are shown in Figure 2(a). It can be seen that the GIDL current and/or I_B current at $VG > 0.5$ V gradually increased during CHCS. This result implies that electrons are trapped in HfO_2 layer within drain side to bend the band upward, therefore elongating the path of band to band tunneling during CHCS. Consequently, it can decrease the GIDL current and/or I_B current at $V_G > 0.5$ V as I-V measurement. The corresponding energy diagram is shown in the inset of Fig. 2(a). Additionally, the C-V curve shows the occurrence of electron trapping near drain side as shown in Figure 2(b). It can be seen that the capacitance of gate terminal to drain terminal versus gate voltage (C_{GD}-V_G) curve shifts in positive direction after CHCS, which is consistent with the linear I_D-V_G result in Fig. 1.

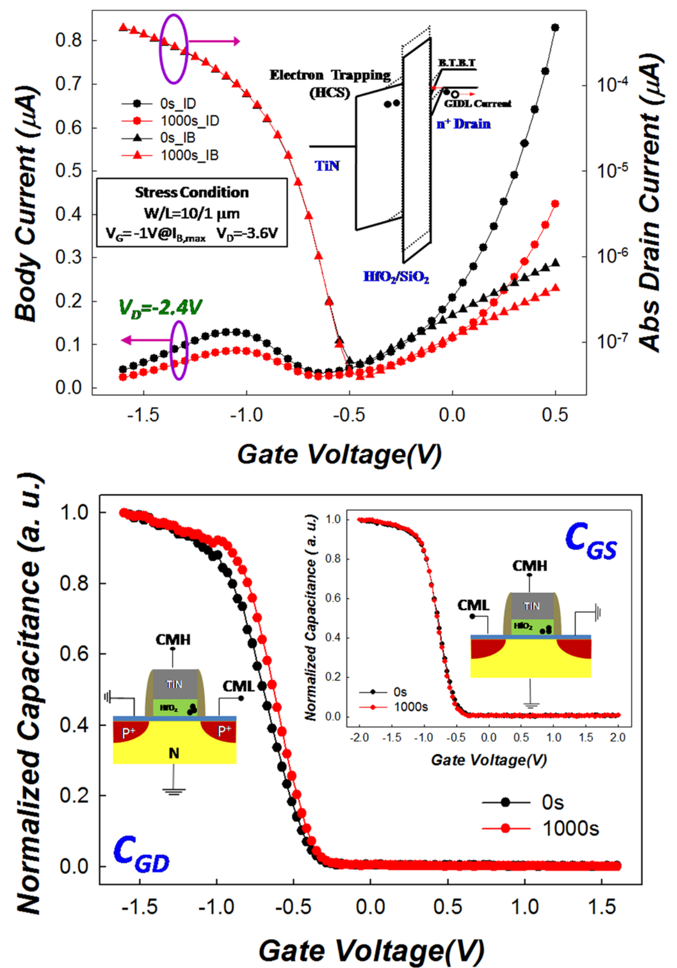

FIG. 2. (a) I_D-V_G and corresponding I_B-V_G transfer characteristic curves under $V_D = -2.4$ V as a function of stress time during CHCS for devices. The inset shows the energy diagram of GIDL behavior under CHCS. (b) Normalized C_{GD}-V_G curve before and after CHCS and its measurement method. The inset shows Normalized C_{GS}-V_G curve before and after CHCS and its measurement method.

However, the capacitance of gate terminal to source terminal versus gate voltage (C_{GS}-V_G) curve has on significant change before and after stress, demonstrating the degradation is located at drain side. As well as, those experimental data are consistent with the suggestion of degradation which is dominated by CHC-induced electron trapping within drain side we declared. However, the occurrence of electron trapping at drain side still has insufficient justification to vary V_{th} with insignificant N_{it} generation. In order to comprehend how comes the V_{th} shift under CHCS, we extract the degraded tendency of V_{th} versus stress time in linear and saturation region, which are defined Lin-V_{th} and Sat-V_{th}, respectively. Figure 3 shows the CHCS degradation of Lin-V_{th} and Sat-V_{th} versus stress time. The Lin-V_{th} was extracted from G_{mmax} and corresponding gate voltage at $I_D = 10^{-5}$ A is selected for Sat-V_{th}. It can be observed that an obvious shift on Lin-V_{th}, but Sat-V_{th} seem almost to be invariant under CHCS. As the result, the mechanism is deduced by trapping-induced DIBL. As electron-hole pairs are created by CHC impact ionization, CHC-induced electrons could be trapped into HfO_2 layer within drain side, which has been evidenced previously. As electron trapping occurs, it could bend channel potential upward to help the linear V_D (Lin-V_D) to

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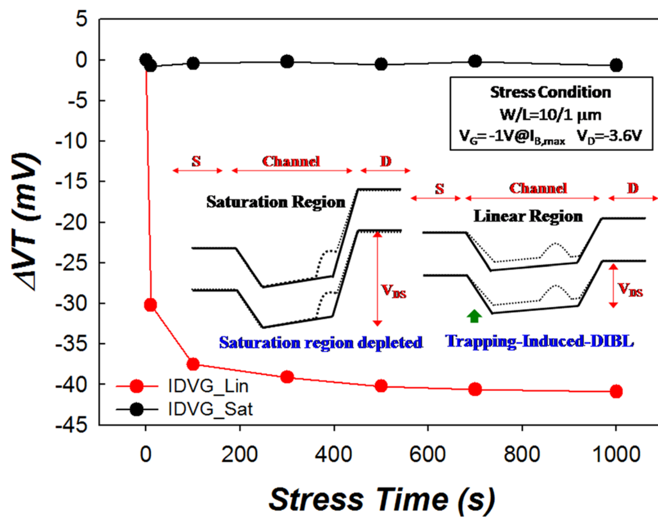

FIG. 3. The CHCS-induced Lin-V_{th} and Sat-Vth shift for HfO_2/TiN p-MOSFETs with $L = 1\,\mu m$. The inset shows the trapping-induced DIBL mechanism due to CHC-induced electron-trapping under linear and saturation region.

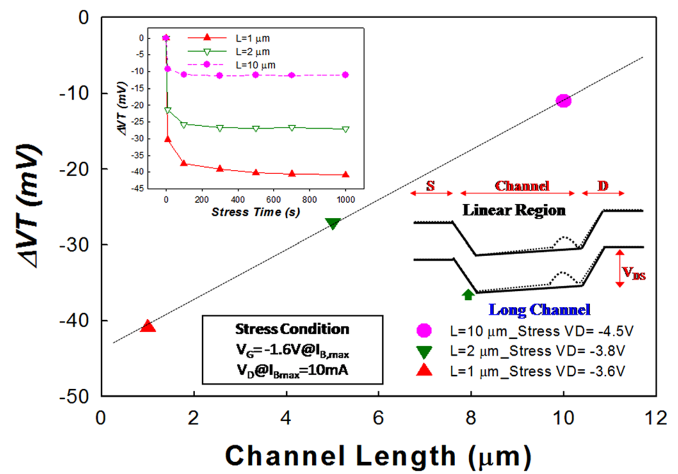

FIG. 4. The relation of Lin-V_{th} shift versus channel length for HfO_2/TiN p-MOSFETs under CHCS. The inset shows the Lin-V_{th} shift versus stress time for HfO_2/TiN p-MOSFETs with $L = 1\,\mu m$, $2\,\mu m$ and $10\,\mu m$ under CHCS and the illustration of trapping-induced DIBL behavior for long channel devices.

deplete channel, therefore lowering the source barrier as the illustration shown in the inset of Fig. 3. Nevertheless, under saturation region, higher V_D could deplete the trapping-induced potential variation to dominate the lateral electric field in channel, expressing an invariant in Sat-V_{th} as shown in the inset of Fig. 3. This is because the original I_D-V_G characteristic before stress has a conventional DIBL, resulting in a shift between Lin-V_{th} and Sat-V_{th} about 30 mV (not shown on here). If the Sat-V_{th} will be changed, the more significant trapping behavior which is greater than the influence of Sat-V_D should be required. According to our argument, the devices with long channel length were selected to prove the mechanism. Figure 4 shows the Lin-V_{th} shift versus stress time on HfO_2/TiN p-MOSFETs under CHCS with different L, including $1\,\mu m$ and $10\,\mu m$. In order to keep the equivalent probability of trapping, the close impact ionization rate is considered by choosing similar I_{Bmax} to control the same amount of electron-hole pairs. Due to the 10 mA I_{Bmax}, the long channel devices $L = 10$ and $2\,\mu m$ have a corresponding V_D are -4.5 V and -3.8 V, respectively. Figure 4 shows the Lin-V_{th} shift under CHCS for HfO_2/TiN p-MOSFETs with different channel length L. It can be found that the Lin-V_{th} has a positive shift on all the devices, regardless of different channel length. However, the Lin-V_{th} shift has a negative related to channel length L. The device with the longest channel corresponds to the most insignificant shift under CHCS, since the behavior of trapping-induced DIBL is suppressed by long channel device. This is because the potential variation due to electron trapping is growingly hard to extend to source side as channel length increases under Lin-V_D. Therefore, the Lin-V_{th} on long channel device has an insignificant degradation which is consistent with the model we supported. Consequently, the Lin-V_{th} shift on HfO_2/TiN p-channel MOSFETs under CHCS results from electron trapping has been generalized in this work.

This letter studies the CHCS behaviors on HfO_2/TiN p-channel MOSFETs. We found that the degradations result from electron trapping, leading G_m decrease and positive Lin-V_{th} shift, but Sat-V_{th} shows an insignificant degradation during stress. This dissimilar behavior of V_{th} is attributed to CHC-induced electron trapping induced DIBL. The devices with different channel length are introduced into evidence of trapping-induced DIBL behavior. As the result, the slightest Lin-Vth shift is corresponding to the HfO_2/TiN p-channe MOSFET with the longest channel length.

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