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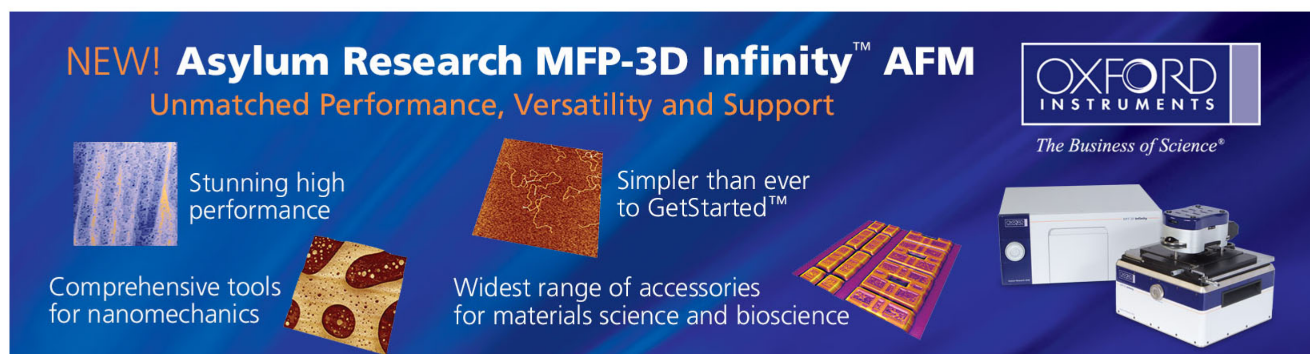

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Reliability improvement of InGaZnO thin film transistors encapsulated under nitrogen ambient

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The nitrogen ambient encapsulation (NAE) technique is introduced to improve the reliability issue for the amorphous InGaZnO (a-IGZO) thin-film transistors under positive gate bias stress (PGBS). For the NAE devices, the threshold voltage (V_{th}) shift is significantly decreased from 1.88 to 0.09 V and the reduction of saturation drain current is improved from 15.75 to 5.61 μA as compared to the bare a-IGZO counterparts after PGBS. These improvements are attributed to the suppression of negatively charged oxygen adsorption on the a-IGZO backsurface and thereby well maintain the channel potential of NAE devices, which in turn sustain the V_{th} during PGBS. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3702794]

Thin film transistors (TFTs) are widely used as pixel switch in the active-matrix liquid crystal display (AMLCD). The carrier mobility and device uniformity of TFTs are well known to strongly affect the properties of AMLCD. Due to the low carrier mobility of hydrogenated amorphous silicon (a-Si:H) TFTs, a larger dimensional device is required to obtain the higher drive current and makes the a-Si:H TFTs actualize high brightness and high aperture ratio in TFT array difficultly. To overcome this problem, various crystallization methods such as excimer laser annealing have been proposed to enhance the carrier mobility, i.e., polycrystalline silicon TFTs (poly-Si TFTs).[1] However, the uniformity of electrical characteristics in poly-Si TFTs is still a critical issue, which seriously restricted its applications. Recently, the amorphous InGaZnO TFTs (a-IGZO TFTs) have been considered as a good alternative for the AMLCD and active-matrix organic light-emitting diode (AMOLED) applications due to their higher carrier mobility than the traditional a-Si:H TFTs and superior device uniformity than the poly-Si TFTs.[2–4] Although the high-performance a-IGZO TFTs have been proposed,[2–4] the poor device reliability is one of the main limitations for the commercial product exploitation.

It is already known that the ambient effects such as oxygen molecules and light illumination play important roles in the electrical degradation of metal oxide transistors.[5–9] The study by Kang *et al*. reported that the threshold voltage (V_{th}) shift of a-IGZO TFTs was about 47 V as the oxygen pressure increased from 8.5×10^{-6} to 760 Torr.[10] Therefore, for practical application, it is necessary to fabricate the robust a-IGZO TFTs which can immunize against the unfavorable environment effects. In this work, we propose a simple method to construct a highly stable a-IGZO TFTs. In order to isolate the interference of environment atmosphere, the fabricated a-IGZO TFTs were finally encapsulated under nitrogen ambient. As compared with the bare TFT devices, the nitrogen ambient encapsulation (NAE) ones exhibit negligible V_{th} shift and minor saturation drain current (I_{Dsat}) reduction after DC positive gate bias stress (PGBS). The possible mechanism of the instability phenomenon is also investigated.

Bottom-gate inverted-staggered a-IGZO TFTs were fabricated on the glass substrate in this work. First, the Ti/Al/Ti (50/180/150 nm) trilayer metal film was deposited through dc-sputter system and the gate pattern was transferred by lithography process. Next, a 300-nm-thick SiN_x film was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 200 °C as the gate insulator. A 30-nm-thick a-IGZO active layer was then deposited by the dc-sputtering system at 300 W of plasma discharge power and 5 mTorr of process pressure in a gas mixture ratio of $O_2/Ar = 20\%$. Then, the thermal annealing process was carried out at 220 °C for 2 h in clean dry air ambient. After defining the active region, the 200-nm-thick SiO_x as etch stop layer was deposited by PECVD at 170 °C and patterned by dry etching to open the source/drain (S/D) contact hole, followed by the Ti/Al/Ti (50/180/150 nm) metal S/D formation. Some of these samples attached with driers, named as NAE TFTs, were then simultaneously encapsulated under the nitrogen ambient by using a covered glass. A thin adhesive layer of UV glue was applied to fix the covered glass for the protection of the devices from the outer ambience. Eventually, the adhesive layer was solidified by means of UV light exposure for 10 min in N_2 ambient. The photographic image of the NAE TFTs devices was shown in Fig. 1. For comparison, the conventional bare TFTs without encapsulation were also fabricated with the same process run.

The a-IGZO TFTs with $L = 4\ \mu m$ and $W = 30\ \mu m$ are employed in this work. The V_{th} is determined at normalized drain current ($I_{DS} \times L/W$) = 1 nA for $V_{DS} = 0.1$ V. The subthreshold swing (SS) is extracted from the inverse maximum slope of the semi-logarithmic I_{DS} versus V_{GS} curve at $V_{DS} = 0.1$ V. The initial V_{th}, SS, and field-effect mobility (μ_{FE}) are 0.44 V, 291 mV/decade, and 12.8 cm^2/Vs for the NAE a-IGZO TFTs, respectively, while those values are 0.81 V, 290 mV/decade, and 12.1 cm^2/Vs for the bare devices, as shown in Figs. 2(a) and 2(b). The corresponding

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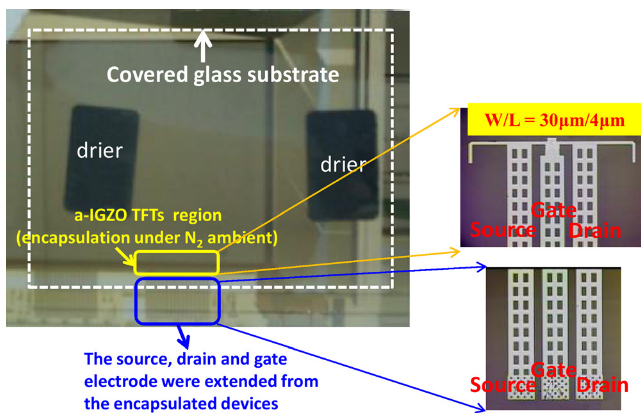

FIG. 1. The photograph of the NAE a-IGZO TFTs. The dotted lines indicate the covered glass substrate that was used to isolate the interference of environment atmosphere.

cross-sectional diagrams of the NAE and bare TFTs are also plotted in Figs. 2(a) and 2(b), accordingly. Although both devices appear the similar SS and μ_{FE}, however, the bare devices exhibit larger initial V_{th}. The oxygen adsorption on the a-IGZO surface is relatively easy for the bare TFTs, thus its initial V_{th} is significantly increased.[10] On the contrary, the lower V_{th} of NAE devices is attributed to the reduced negatively charged oxygen adsorption on the a-IGZO backsurface.

Prior to the PGBS experiment, all the samples were cured on a hot plate at 100 °C for 2 h to decrease the influence of ambient moisture. The electrical instabilities of NAE and bare devices are performed with the DC PGBS of $V_G = 30$ V and $V_{DS} = 0$ V for 1500 s at room temperature as shown in Figs. 2(a) and 2(b), respectively. The V_{th} shift as a function of bias stress duration is plotted in Fig. 2(c) and the inset shows the SS variation with the stress time. During PGBS, the parallel transfer characteristics shift to the positive direction with no significant degradation of SS for both devices are observed, which indicates that the interface state creations are negligible in a-IGZO TFTs after PGBS. However, a much greater V_{th} shift of 1.88 V is observed for the bare devices as compared to 0.09 V for the NAE ones under the same stress time. Previous investigations have reported that a combination of the charge trapping at the dielectric/channel layer and the oxygen adsorption at the a-IGZO backsurface is responsible for the electrical-stress degradation of a-IGZO TFTs.[11–13] Considering that both devices have an identical vertical electric field during PGBS test, the charge trapping at their dielectric/channel layers will be similar. Therefore, the remarkable V_{th} shift of the bare TFTs is mainly ascribed to the influence of the ambient environment. Although the SiO_x etch stop layer coated on the back channel region can be used as a passivation layer, the outer ambience such as oxygen molecules can still penetrate through the SiO_x layer due to the less dense thin film deposited by PECVD at relatively low temperature.[14,15] As mentioned in previous oxide-semiconductor device literatures,[11,16–18] adsorption oxygen molecules on their surface would cause a charge transfer phenomenon and the reaction could be expressed in the form of $O_2 + e^- \rightarrow O_2^-$. As the applied gate bias is raised beyond the V_{th} of a-IGZO TFTs, the conduction electrons $[e^-]$ in the a-IGZO thin film will be consid-

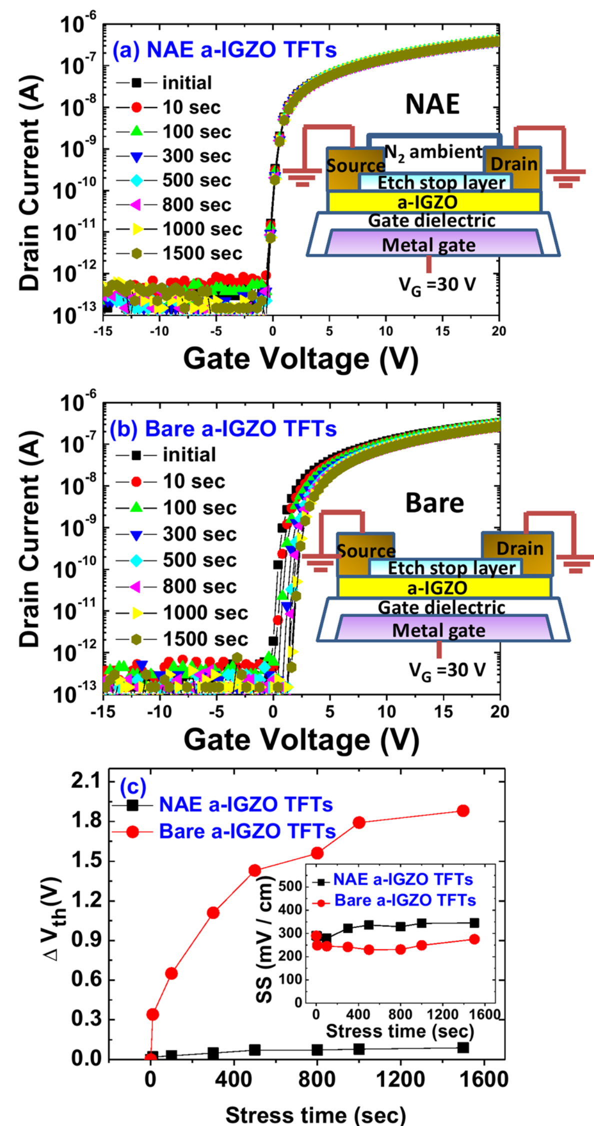

FIG. 2. The transfer characteristics of (a) NAE a-IGZO TFTs and (b) bare ones during PGBS of $V_G = 30$ V and $V_{DS} = 0$ V for 1500 s. The inset showed the corresponding cross-sectional diagrams. (c) Stress time dependence of V_{th} shift for the NAE TFTs and bare ones. The inset showed the SS variation with the stress time for both devices.

erably increased and then extracted by the surrounded oxygen molecules, resulting in a significant increase in negatively charged oxygen $[O_2^-]$ adsorption on the device backsurface. For the bare TFTs, the depletion layer formed underneath the a-IGZO backsurface will therefore be enlarged and simultaneously raise the channel potential, leading to the increase of V_{th} as the oxygen molecules are absorbed. The schematic plot and band diagram for the bare TFTs after PGBS are shown in Figs. 3(a) and 3(b) to explain the observed experimental results, respectively. In contrast, for the NAE devices, the undesirable oxygen molecules are obstructed outside the covered glass and effectively eliminate the oxygen penetration through the SiO_x etch stop layer, as shown in Fig. 3(c). The corresponding band diagram of NAE devices after PGBS is also shown in Fig. 3(d). Due to the suppression of the oxygen adsorption on the a-IGZO backsurface for the NAE devices, the channel potential will not be elevated, thereby sustaining the V_{th} during PGBS.

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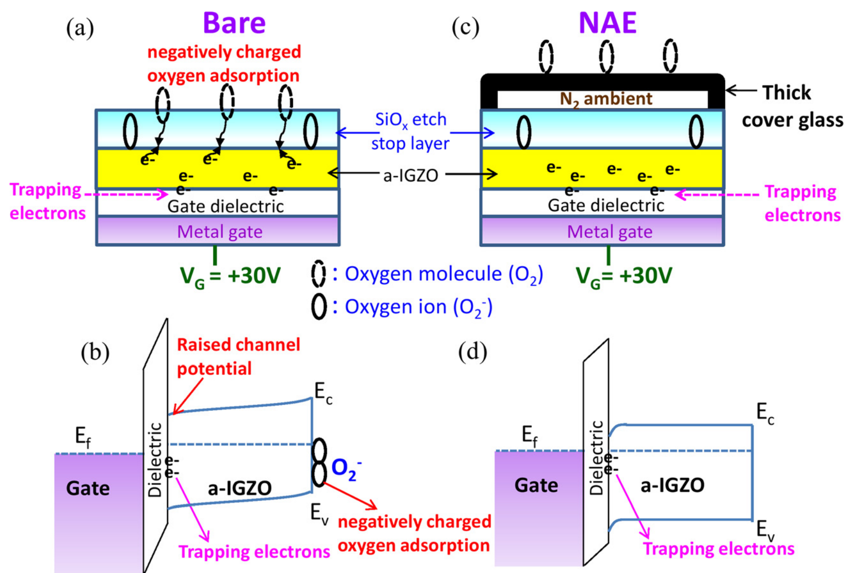

FIG. 3. (a) The schematic plot of bare a-IGZO TFTs during PGBS of $V_G = 30$ V and $V_{DS} = 0$ V. (b) The band diagram of bare a-IGZO TFTs after PGBS. (c) The schematic plot of NAE a-IGZO TFTs during PGBS of $V_G = 30$ V and $V_{DS} = 0$ V. (d) The band diagram of NAE a-IGZO TFTs after PGBS.

Figures 4(a) and 4(b) show the output characteristics of the NAE and bare devices after PGBS of $V_G = 30$ V and $V_{DS} = 0$ V for 1500 s, respectively. The I_{Dsat} reduction of the bare devices ($\Delta I_{Dsat} = 15.75\ \mu A$) after PGBS is more severe than the NAE ones ($\Delta I_{Dsat} = 5.61\ \mu A$) at $V_{DS} = 10$ V and $V_{GS} = 6$ V. Owing to the large amount of oxygen adsorption during PGBS for the bare devices, the V_{th} will be significantly increased to degrade the drain current. Nevertheless, the slight I_{Dsat} reduction is still observed in the NAE devices, which can be ascribed to the minor electron trapping at or near the dielectric/channel interface.

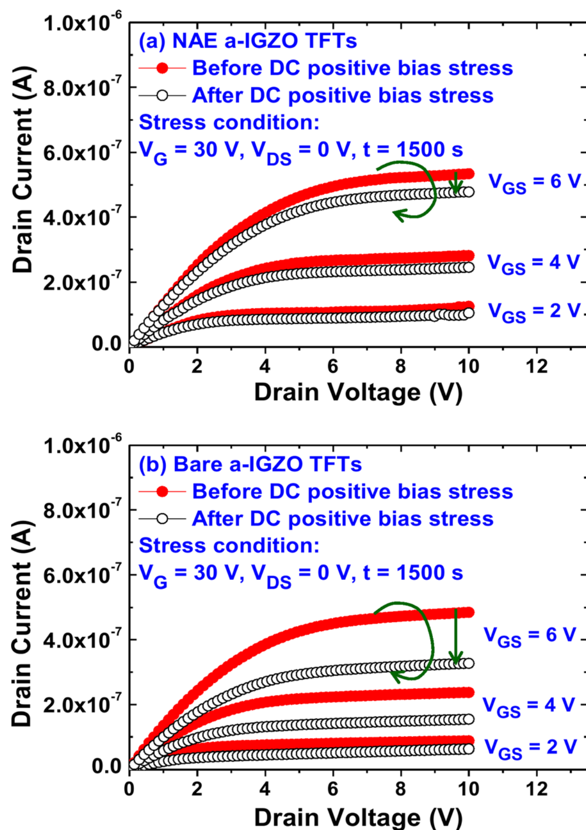

FIG. 4. The output characteristics of (a) NAE a-IGZO TFTs and (b) bare ones after PGBS of $V_G = 30$ V and $V_{DS} = 0$ V for 1500 s.

In summary, the effect of nitrogen encapsulation on the electrical instabilities of a-IGZO TFTs under the DC PGBS is investigated. The NAE devices exhibit superior V_{th} stability ($\Delta V_{th} = 0.09$ V) than the bare ones ($\Delta V_{th} = 1.88$ V) after PGBS at $V_G = 30$ V for 1500 s. Furthermore, a small I_{Dsat} reduction of 5.61 μA after PGBS test is also observed for the NAE TFTs as compared to 15.75 μA for the bare ones at $V_{DS} = 10$ V and $V_{GS} = 6$ V. The improvement can be attributed to the elimination of the negatively charged oxygen adsorption on the backsurface for the NAE devices. Practically, such simple method to construct a highly stable a-IGZO TFTs is promising for the applications in AMLCD and AMOLED.

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