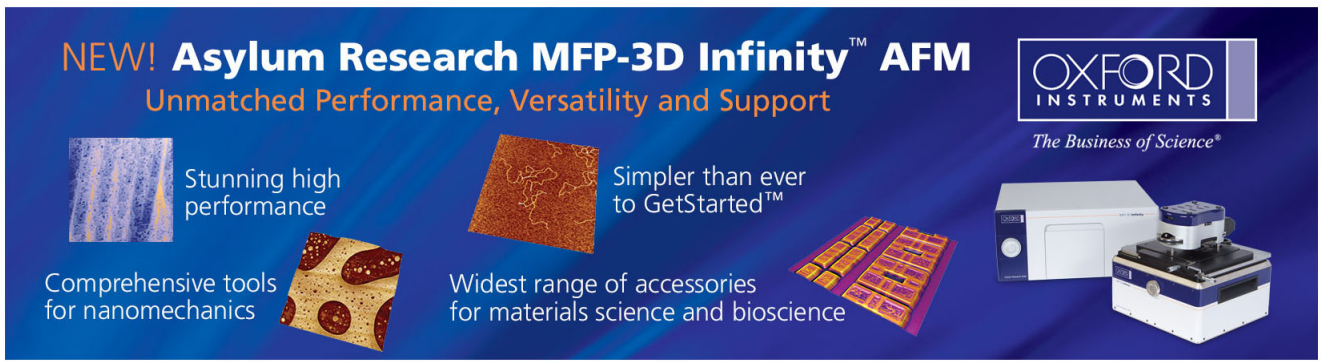
AIP Applied Physics Letters

Fast programming metal-gate Si quantum dot nonvolatile memory using green nanosecond laser spike annealing

Yu-Chung Lien, Jia-Min Shieh, Wen-Hsien Huang, Cheng-Hui Tu, Chieh Wang, Chang-Hong Shen, Bau-Tong Dai, Ci-Ling Pan, Chenming Hu, and Fu-Liang Yang

Citation: Applied Physics Letters **100**, 143501 (2012); doi: 10.1063/1.3700729
View online: http://dx.doi.org/10.1063/1.3700729
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/100/14?ver=pdfcov
Published by the AIP Publishing



Fast programming metal-gate Si quantum dot nonvolatile memory using green nanosecond laser spike annealing

Yu-Chung Lien,[1] Jia-Min Shieh,[1,2,a)] Wen-Hsien Huang,[1] Cheng-Hui Tu,[2] Chieh Wang,[2] Chang-Hong Shen,[1] Bau-Tong Dai,[1] Ci-Ling Pan,[3] Chenming Hu,[4] and Fu-Liang Yang[1]
[1]*National Nano Device Laboratories, No. 26, Prosperity Road 1, Hsinchu 30078, Taiwan*
[2]*Department of Photonics and Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan*
[3]*Department of Physics, National Tsing Hua University, Hsinchu 30013, Taiwan*
[4]*Department of Electrical Engineering and Computer Science, University of California, Berkeley, California 94720, USA*

(Received 20 January 2012; accepted 16 March 2012; published online 2 April 2012)

The ultrafast metal-gate silicon quantum-dot (Si-QD) nonvolatile memory (NVM) with program/erase speed of 1 μs under low operating voltages of $\pm$ 7 V is achieved by thin tunneling oxide, *in situ* Si-QD-embedded dielectrics, and metal gate. Selective source/drain activation by green nanosecond laser spike annealing, due to metal-gate as light-blocking layer, responds to low thermal damage on gate structures and, therefore, suppresses re-crystallization/deformation/diffusion of embedded Si-QDs. Accordingly, it greatly sustains efficient charge trapping/de-trapping in numerous deep charge-trapping sites in discrete Si-QDs. Such a gate nanostructure also ensures excellent endurance and retention in the microsecond-operation Si-QD NVM. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3700729]

Silicon quantum dot (Si-QD) nonvolatile memory (NVM), which is known for low-voltage and fast program/erase (P/E) operation, immunity to gate coupling effect, and good cycling endurance, has been viewed as a potential NAND memory alternative to the floating gate memory.[1–3] In order to further improve the speed of NVM, thin tunneling oxide and metal gate are necessary. Although the pursuit of thin tunneling oxide enhance the tunneling probability of electrons,[4] it inevitably degrades the reliability of NVMs.[5,6] Therefore, the bandgap engineered tunneling dielectric such as thin Si_3N_4 (<2 nm) or small Si-QD (1.1 nm) in ultra-thin SiO_2 were proposed to improve the reliability.[7,8] On the other hand, metal gate significantly improves the erase characteristic by additional work-function control[9,10] and eliminates the depletion and dopant diffusion of polycrystalline silicon (poly-Si).[11,12] However, classical rapid thermal annealing (RTA) and flash lamp annealing (FLA) are not compatible to self-align process due to their high thermal budget and non-selective activation on the nanostructured gate dielectrics.[12] Laser spike annealing (LSA) has become a candidate of junction technology because of the low doping activation at ion-implanted source-drain and the poor high-κ/Ge interface by RTA.[13,14] Furthermore, Heo *et al*. have reported the reduction of leakage current density and charge loss rate of metal-Al_2O_3-nitride-oxide-semicoductor type flash memory devices by LSA rather than RTA.[15] Green nanosecond laser, with high repetition rate and long wavelength, is particularly suitable for non-melt LSA because of its sub-millisecond scanning, low-photo-energy light producing less damage on metal-gate, gate dielectric, or even more delicate nanostructured gate stacks.[16–18]

In this study, we take advantages of thin tunneling oxide, *in situ* Si-QD-embedded nitride layer, and selective source/drain (S/D) activation by green nanosecond laser spike annealing (GN-LSA) that is enabled by metal-gate as a light-blocking layer. The laser activated Si-QD NVM shows microsecond P/E speed under low operating voltage and reveals high performance in reliability of retention and endurance in comparison with conventional metal-SiO_2-Si_3N_4-SiO_2-poly-Si (MONOS) NVM without Si-QDs.

Devices were fabricated on 6 in. silicon wafer with a 1000-nm-thick thermal dioxide. A layer of 100-nm-thick amorphous silicon (α-Si) was deposited by low pressure chemical vapor deposition (LPCVD) at 550 °C and then followed with laser crystallization at room temperature to be a poly-Si with grain size about 1 μm. The laser source is HIPPO 532QW Nd:YAG laser with wavelength, pulse width, scanning speed, and beam size of 532 nm, 13 ns, 25 cm/s, and 2.7 mm $\times$ 60 μm, respectively, which achieves the operation of sub-millisecond scanning of GN-LSA. The power for laser crystallization is 6.2 W. The tunneling oxide ($\sim$2 nm), Si-QDs-embedded nitride ($\sim$7 nm), and blocking oxide ($\sim$5 nm) were grown and deposited by LPCVD.[3] Si-QDs-embedded nitride layer formed from Si-rich nitride nanocomposite was sequentially synthesized by the method reported.[3] The Si-QDs prepared by *in situ* successive deposition enhances the bonding between the Si-QDs and the surrounding nitride. The transmission electron microscopy (TEM) of the NVM from gate view is shown in Fig. 1(a), and the inset shows the extended cross section of gate stacks. The 200-nm-thick Al-Si-Cu alloy was deposited as a gate electrode. Afterwards, the gate patterning, S/D implantation, and activation by GN-LSA with power of 3.5 W were performed. The measured reflectance of Al-Si-Cu alloy and poly-Si at wavelength of 532 nm are 0.9 and 0.3, respectively, indicates that the former is suitable for preventing pattern damage and gate dielectric from high power density of GN-LSA. Finally, the NVMs were completed by the standard passivation and metallization. A

a)E-mail: jmshieh@ndl.narl.org.tw and jmshieh@faculty.nctu.edu.tw.

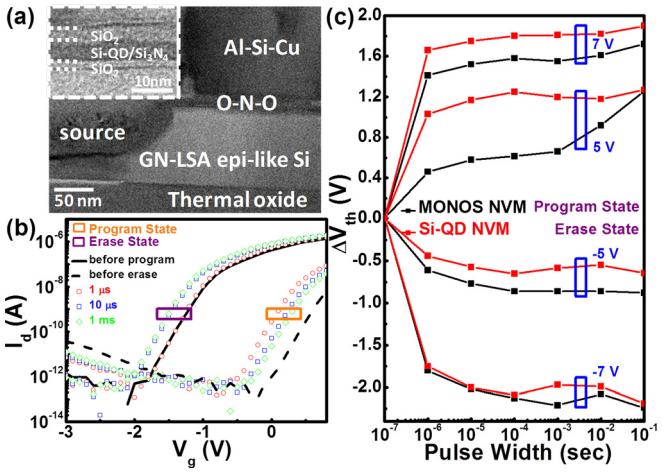


FIG. 1. (a) TEM of Si-QD NVM gate view. Inset: extended cross-section of gate stacks. (b) Transfer characteristic of Si-QD NVM before and after programming and erasing conditions. (c) Program and erase speed characteristics of MONOS and Si-QD NVMs at gate voltages of ± 5 and ± 7 V.

MONOS NVM with nitride of 7 nm was also fabricated as a controlled sample to investigate the effect of Si-QDs.

The transfer characteristics of Si-QD NVMs are shown in Fig. 1(b). The Si-QD NVMs show good electrical properties with high ON/OFF current ratio ($>10^7$) and low subthreshold swing (<0.19 V/decade). Low subthreshold swing characteristic facilitates the memory-state diagnosis of program and erase states. In addition, the output characteristic shows fairly lower parasitic resistance (R_p) of 3.07 kΩ-μm from GN-LSA than 12.14 kΩ-μm from RTA. After programming and erasing at 7 and −7 V with 1 μs pulse, the threshold voltage (V_{th}) shifts 1.67 and 1.8 V, respectively, which is large enough for a typical sense amplifier to detect memory window of 0.5 V.[19] The program and erase speed characteristics of MONOS and Si-QD NVMs were programmed and erased at different voltages of ±5 and ± 7 V by Fowler-Nordheim (F-N) injection for NAND-architecture application as shown in Fig. 1(c). During the program state, the Si-QD NVMs demonstrate broader memory window under each applied voltages because of the narrow bandgap and deep conduction band of Si-QDs.[2] It has been reported that the Si-QDs in SiO_2 function as a tunneling path from the Si substrate to the gate terminal which leads to the enhancement of the tunneling current;[20] moreover, the decrement of turn-on voltage and the enhancement of F-N tunneling performance result from abatement of effective barrier height which is more dominant for Si-rich SiO_2 than for pure SiO_2.[21] Similarly, the *in situ* prepared Si-QDs in nitride have modulated the $SiO_2/Si_3N_4/SiO_2$ gate stacks and lead to the improvement of the program efficiency. Although the erase speed of Si-QD NVMs is inferior to the MONOS NVMs due to the deep charge-trapping level, they seem to be comparable with sufficiently large erase voltage of −7 V.

Figure 2 depicts the band diagram of MONOS and Si-QD NVMs under program and erase states. The reasons for the fast P/E speed are as follows. The NVMs with Si-QDs exhibit more electron charging nodes between the interface of silicon nitride and Si-QDs or the trapping site in Si-QDs.[2,5] On the other hand, direct tunneling and F-N tunneling mechanisms occur simultaneously when the thickness of tunneling oxide shrinkages to <5 nm.[4] On the part of erase operation, the unwanted electron tunneling current through a blocking oxide is greatly suppressed through higher work function of Al-Si-Cu alloy than n^+ poly-Si gate. Hence, the higher electron barrier height by metal gate results in fewer recombinations of electron-hole pairs and thus leads to efficacious erasure. Chiang *et al*. have previously demonstrated high P/E speed (10/100 μs) SONOS NVM with *in situ* prepared Si-QDs.[3] The reasons of further improvement of this work are achieved by thinner blocking oxide, which is barely impacted by re-crystallization/deformation/diffusion of embedded Si-QDs due to low thermal budget on nanostructured gate dielectrics and selective S/D activation by GN-LSA enabled by metal-gate as a light-blocking layer. The suppression of the re-crystallization/deformation of embedded Si-QDs was confirmed by TEM plots (no shown herein) showing unchanged diameter (~3.9 nm) and d-spacing ($Si_{\langle 111 \rangle}$)

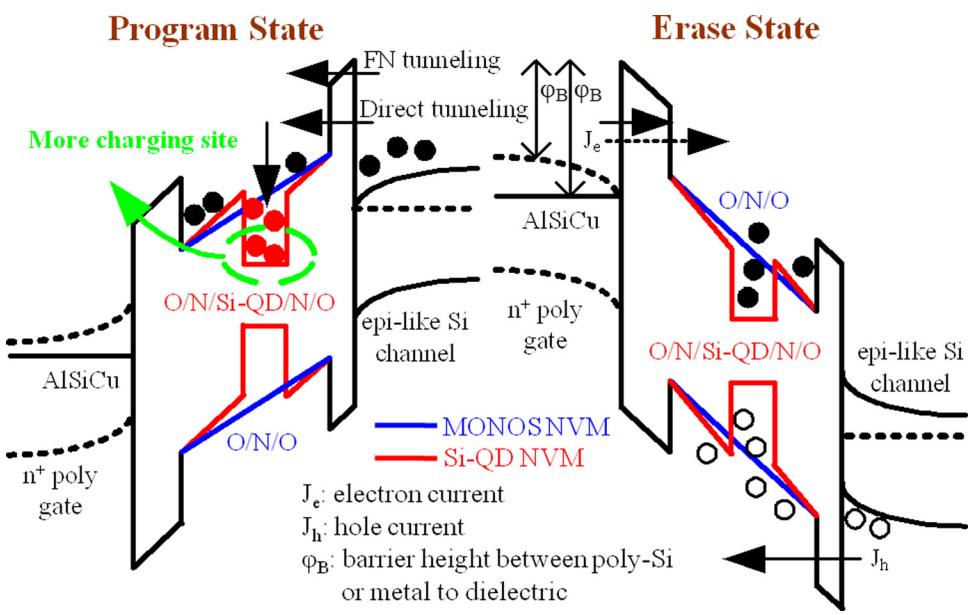


FIG. 2. The band diagram of MONOS and Si-QD NVM under program and erase states.

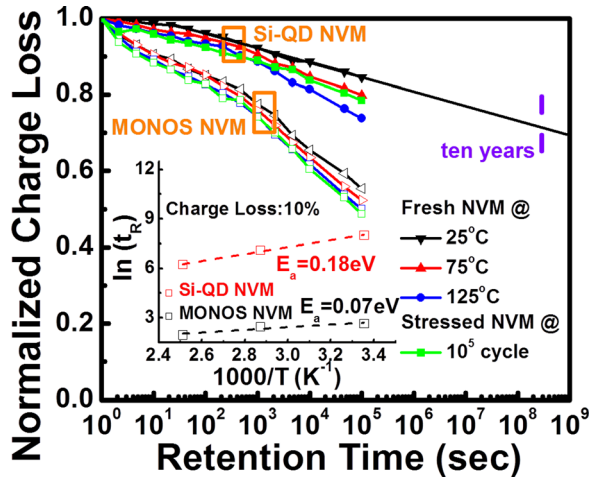


FIG. 3. Normalized charge loss ($\Delta V_{th}(t)/\Delta V_{th0}$) as a function of retention time of MONOS and Si-QD NVMs at temperatures of 25, 75, and 125 °C and after 10^5 P/E cycles. Inset: Arrhenius plots of retention time characteristics for charge loss of 10%.

(3.07 A) of Si-QDs embedded in nitride after GN-LSA. Moreover, during sub-millisecond scanning of GN-LSA, certainly low laser-power penetrating through metal gate into gate dielectrics provides only transient and little heat to gate dielectrics and thus is unable to cause the diffusion of Si element which takes place in a long-term duration.[22]

The normalized charge loss defined as $\Delta V_{th}(t)/\Delta V_{th0}$, where $\Delta V_{th}(t)$ and ΔV_{th0} stand for the transient memory window and initial memory window, as a function of retention time of MONOS and Si-QD NVMs are shown in Fig. 3. The ΔV_{th0} of MONOS and Si-QD NVMs are 1.67 and 1.41 V, respectively. Their retention characteristics are performed under temperatures of 25, 75, and 125 °C and after 10^5 P/E cycles. The Si-QD NVMs show superior data retention at room temperature with the charge loss rate of 28.4% ($\Delta V_{th} \sim 1.2$ V) to MONOS NVMs with charge loss rate of 81.7% ($\Delta V_{th} \sim 0.25$ V) by extrapolation at ten years. This is attributed to a suppression of the charge loss by electrostatic repulsion among the charged Si-QDs.[23] The improvement on data storage capability by Si-QDs still prevail under higher temperature. In order to clarify the charge loss mechanism between NVMs with and without Si-QDs, the effective activation energy (E_a) from the Arrhenius plots of retention time was extracted in the inset of Fig. 3. Among the NVM with shallow charging sites, the electrons wash away easily, which results in large charge loss inherently. Therefore, thermal heat, as a driving force to charge loss of the NVM system, has little impacts on the charge loss of NVMs with shallow charging sites, which acquires small E_a and vice versa. In more details, the larger value of E_a stands for the larger energy for charge loss and thus the preferable for data retention. Here, the retention time was defined as the time that the ΔV_{th} decreased by a factor of 10% compared with ΔV_{th0}. The extracted E_a of the MONOS and Si-QD NVMs are 0.07 and 0.18 eV, elucidating the prolonged data retention by the deep charge-trapping level formed at Si-QDs/nitride interface.[3] Furthermore, the E_a is closely related to the charge loss rate, which corresponds to the result of NVMs with multi-layered SiC nanocrystals.[24] The E_a of Si-QD NVMs with charge loss rate of 10, 20, and 30% are about 0.18, 0.45, and 0.72 eV, respectively. The explanation is attributed to the discrete quantum-confined energy states of Si-QDs; the electrons trapped in shallower energy states are more prone to cause leakage which results in smaller E_a and vice versa. Regardless of the charge loss from the shallower energy states of Si-QDs, the Si-QD NVMs still show improved retention characteristic to the MONOS NVMs with their E_a about 0.07-0.1 eV. Comparing the E_a of the *in situ* Si-QD NVM with charge loss rate of 20% to the E_a of the SiGe QD capacitor and SiC QD NVM with charge loss rate of 20 and 25%, the former exhibits higher E_a of 0.45 eV than the latter of 0.37 and 0.03 eV, respectively.[24,25]

Figure 4(a) shows the endurance of MONOS and Si-QD NVMs. The programming conditions are all 7 V under 1 μs pulse, but the Si-QD NVMs are erased at −7 V with different pulse durations from 1 to 100 μs. After 10^5 P/E cycles, the memory window of Si-QD NVMs remain larger than that of MONOS NVMs. The slightly larger V_{th} shift upward for Si-QD NVMs are due to the electron trapping in the deep charge-trapping level of Si-QDs or tunneling oxide.[3,5,26] The incomplete removal of the trapped electrons during the erasure operation could also be found from the erase speed characteristic in Fig. 1(c) and leads to the upward shift of V_{th} after increasing P/E cycles. Therefore, the lengthening of the erase period comes to the smaller variation of ΔV_{th} in Fig. 4(a). In addition, the Si-QD NVMs also show better data retention after 10^5 P/E cycles in Fig. 3. Last but not least, we compare our works with some representative groups about important characteristics such as erase speed, data retention with extrapolation at 10 years, and variation of memory window defined as extrapolation at 10^6 P/E cycles in Fig. 4(b). This *in situ* Si-QD NVMs with thin tunneling oxide have demonstrated fast erase speed and comparable data retention. Small variation of memory window of 13%-22% after 10^6 P/E

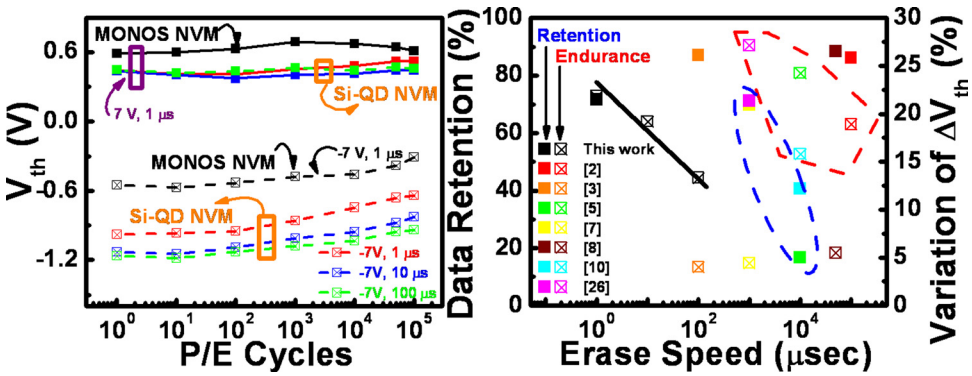


FIG. 4. (a) Endurance characteristics of MONOS and Si-QD NVMs under different programming and erasing conditions. (b) Comparison of the data retention after extrapolation at ten years and variation of memory window after extrapolation at 10^6 P/E cycles.

cycles using erase electrical pulse of $1-100\,\mu s$ and program electrical pulse of $1\,\mu s$ further manifests the reliability of the microsecond-operation Si-QD NVMs.[2,3,5,7,8,10,26]

We have developed a selective S/D activated metal-gate *in situ* Si-QD NVM by GN-LSA. Light-blocking by metal-gate during GN-LSA has benefit on enabling ultra-low thermal budget on sophisticated nanostructured gate dielectric such as *in situ* Si-QDs and thin tunneling oxide. Accordingly, the ultrafast characteristic of program and erase speed of $1\,\mu s$ and certainly fair reliability of endurance and retention are achieved simultaneously. Those results have shed a bright light on the realm of NVM industry.

The authors would like to thank the National Science Council of the Republic of China, Taiwan, for partially supporting this research.

[1]S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe, and K. Chan, Appl. Phys. Lett. **68**, 1377 (1996).
[2]M. F. Hung, Y. C. Wu, and Z. Y. Tang, Appl. Phys. Lett. **98**, 162108 (2011).
[3]T. Y. Chiang, T. S. Chao, Y. H. Wu, and W. L. Yang, IEEE Electron Device Lett. **29**, 1148 (2008).
[4]P. Punchaipetch, K. Ichikawa, Y. Uraoka, T. Fuyuki, E. Takahashi, T. Hayashi, and K. Ogata, Jpn. J. Appl. Phys. **45**, 3997 (2006).
[5]M. She, H. Takeuchi, and T. J. King, IEEE Electron Device Lett. **24**, 309 (2003).
[6]M. She and T. J. King, IEEE Trans. Electron Devices **50**, 1934 (2003).
[7]R. Ohba, Y. Mitani, N. Sugiyama, and S. Fujita, IEDM-Tech. Dig. **2008**, 1.
[8]H. T. Lue, S. Y. Wang, E. K. Lai, Y. H. Shih, S. C. Lai, L. W. Yang, K. C. Chen, J. Ku, K. Y. Hsieh, R. Liu, and C. Y. Lu, IEDM-Tech. Dig. **2005**, 547.
[9]K. C. Chiang, Albert Chin, C. H. Lai, W. J. Chen, C. F. Cheng, B. F. Hung, and C. C. Liao, Symp. VLSI-Tech. Dig. **2005**, 62.
[10]C. H. Lee, K. I. Choi, M. K. Cho, Y. H. Song, K. C. Park, and K. Kim, IEDM Tech. Dig. **2003**, 613.
[11]H. Tseng, D. L. O'Meara, P. J. Tobin, V. S. Wang, G. Xin, R. Hegde, I. Y. Yang, P. Gilbert, R. Cotton, and L. Hebert, IEDM-Tech. Dig. **1998**, 793.
[12]A. Shima, Y. Wang, S. Talwar, and A. Hiraiwa, Symp. VLSI-Tech. Dig. **2004**, 174.
[13]Q. Zhang, J. Huang, N. Wu, G. Chen, M. Hong, L. K. Bera, and C. Zhu, IEEE Electron Device Lett. **27**, 728 (2006).
[14]W. B. Chen, B. S. Shie, and A. Chin, IEEE Electron Device Lett. **32**, 449 (2011).
[15]S. Heo, M. Chang, Y. Ju, S. Jung, and H. Hwang, Appl. Phys. Lett. **93**, 172115 (2008).
[16]J. M. Shieh, C. Chen, Y. T. Lin, and C. L. Pan, Appl. Phys. Lett. **92**, 063503 (2008).
[17]J. Y. Huang, J. M. Shieh, H. C. Kuo, and C. L. Pan, Adv. Funct. Mater. **19**, 2089 (2009).
[18]J. M. Shieh, J. Y. Huang, W. C. Yu, J. D. Huang, Y. C. Wang, C. W. Chen, C. K. Wang, W. H. Huang, A. T. Cho, H. C. Kuo, B. T. Dai, F. L. Yang, and P. C. Lin, Appl. Phys. Lett. **95**, 143501 (2009).
[19]M. H. White, D. A. Adams, and J. Bu, IEEE Circuits Devices Mag. **16**, 22 (2000).
[20]G. Chakraborty, S. Chattopadhyay, and C. K. Sarkar, J. Appl. Phys. **101**, 024315 (2007).
[21]G. R. Lin, C. J. Lin, and H. C. Kuo, Appl. Phys. Lett. **91**, 093122 (2007).
[22]D. Yu, S. Lee, and G. S. Hwang, J. Appl. Phys. **102**, 084309 (2007).
[23]N. M. Park, S. H. Jeon, H. D. Yang, H. Hwang, and S. J. Park, Appl. Phys. Lett. **83**, 1014 (2003).
[24]D. U. Lee, T. H. Lee, E. K. Kim, J. W. Shin, and W. J. Cho, Appl. Phys. Lett. **95**, 063501 (2009).
[25]Y. Liu, S. Tang, and S. K. Banerjee, Appl. Phys. Lett. **88**, 213504 (2006).
[26]C. Y. Ng, T. P. Chen, L. Ding, and S. Fung, IEEE Electron Device Lett. **27**, 231 (2006).