Temperature-Oriented Mobility Measurement and Simulation to Assess Surface Roughness in Ultrathin-Gate-Oxide ($\sim$1 nm) nMOSFETs and Its TEM Evidence

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Abstract—On a 1.27-nm gate-oxide nMOSFET, we make a comprehensive study of SiO_2/Si interface roughness by combining temperature-dependent electron mobility measurement, sophisticated mobility simulation, and high-resolution transmission electron microscopy (TEM) measurement. Mobility measurement and simulation adequately extract the correlation length λ and roughness rms height Δ of the sample, taking into account the Coulomb-drag-limited mobilities in the literature. The TEM measurement yields the apparent correlation length λ_m and roughness rms height Δ_m. It is found that the following hold: 1) $\lambda \approx \lambda_m$ for both the Gaussian and exponential models, validating the temperature-oriented extraction process; 2) the extracted Δ ($\sim$1.3 Å for the Gaussian model and 1.0 Å for the exponential one) is close to that ($\sim$1.2 Å) of Δ_m, all far less than the conventional values ($\sim$3 Å) in thick-gate-oxide case; and 3) the TEM 2-D projection correction coefficient Δ_m/Δ is approximately 1.0, which cannot be elucidated with the current thick-gate-oxide-based knowledge.

Index Terms—Coulomb drag, gate oxide, interface plasmons, mobility, metal–oxide–semiconductor field-effect transistors (MOSFETs), scattering, surface roughness, transmission electron microscopy (TEM), universal mobility.

I. INTRODUCTION

RANDOM roughness at the SiO_2/Si interface can critically affect the carrier transport in the inversion layers of MOSFETs. Thus, attempts to characterize the surface roughness parameters are essential. To facilitate the description of the surface roughness picture, two fundamentally distinct models were proposed [1]: Gaussian and exponential. Both models contain two elements, i.e., correlation length λ and roughness rms height Δ. To assess the underlying λ and Δ, numerical

simulations were applied with the inversion-layer mobility data as inputs [1]–[4]. However, for MOSFETs having ultrathin gate oxides, such a scheme encountered difficulties due to the increasing importance of remote scatterers [5], [6]. Indeed, how to correctly distinguish between the surface roughness and remote scatterers has been a challenging issue [7]. To overcome the issue, we recently proposed a temperature-dependent extraction method [8]. As has been demonstrated [8] on 1.65-nm-gate-oxide nMOSFETs through the use of the Gaussian model, the merits of the method are summarized: 1) it can effectively distinguish the surface-roughness-limited mobility from the remote-scatterer-limited mobility; 2) it can accurately determine the surface roughness parameters; and 3) it can easily be conducted in a certain range around room temperature.

Alternatively, TEM measurements can be performed to provide the apparent correlation length λ_m and the apparent rms height Δ_m. To address the 2-D projection effect in the TEM measurement, a link to the aforementioned Δ was established in terms of correction coefficient Δ_m/Δ [1]. Furthermore, a mathematical transformation from digitized TEM surface roughness data, without directly accounting for λ and Δ, to mobility values was developed, thus producing a quantity associated with the projection correction [9]. However, these works [1], [9] were devoted to the thick-gate-oxide samples only.

To make a comprehensive surface roughness study and to advance the studies [1]–[9], in this paper, we integrate the aforementioned means, i.e., temperature-dependent mobility measurement, sophisticated mobility simulation accounting for both the Gaussian and exponential models, and TEM measurement. In addition, a thinner gate-oxide sample (1.27 nm), which enables fair citation of the simulated Coulomb-drag-limited mobilities (on 1-nm gate oxide) [5], is presented. The results are novel and might substantially improve current understanding of the surface roughness, particularly for the case of ultrathin gate oxides.

II. SAMPLE AND ELECTRICAL CHARACTERIZATION

The device under study was fabricated in a conventional manufacturing process. In this process, SiO_2 film was thermally grown on the (001) surface, followed by NO annealing. Corresponding process parameters can essentially be obtained by
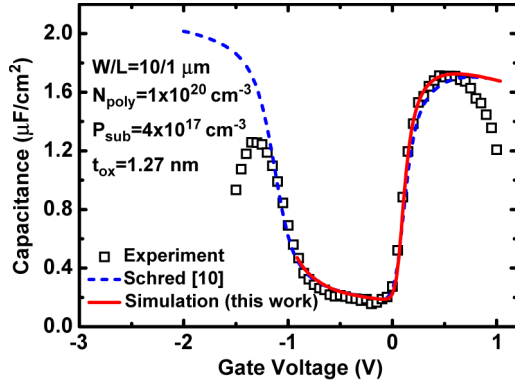
Fig. 1. Comparison of the measured (symbol) and simulated (lines) gate capacitance versus gate voltage. The lines came from the self-consistent Schrödinger and Poisson's equations solvers [10], [11].
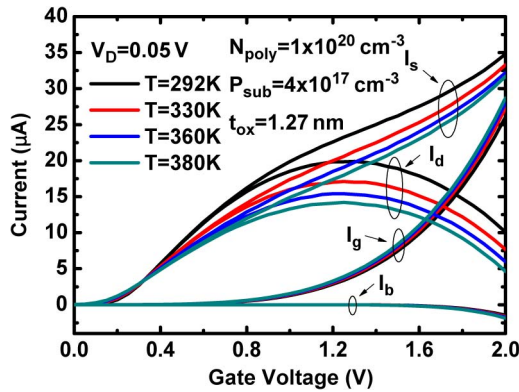

Fig. 2. Measured terminal currents at a drain voltage of 0.05 V versus gate voltage for four different temperatures.
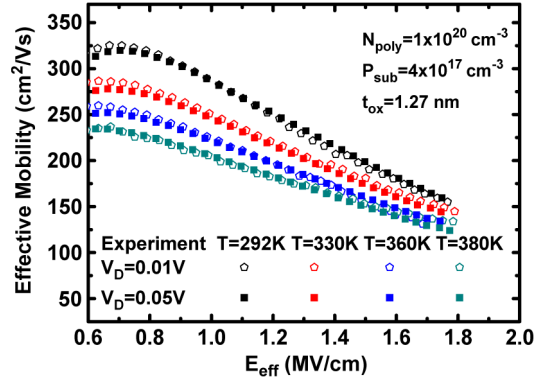

Fig. 3. Measured electron effective mobility at two drain voltages of 0.01 and 0.05 V versus vertical effective field for four temperatures.
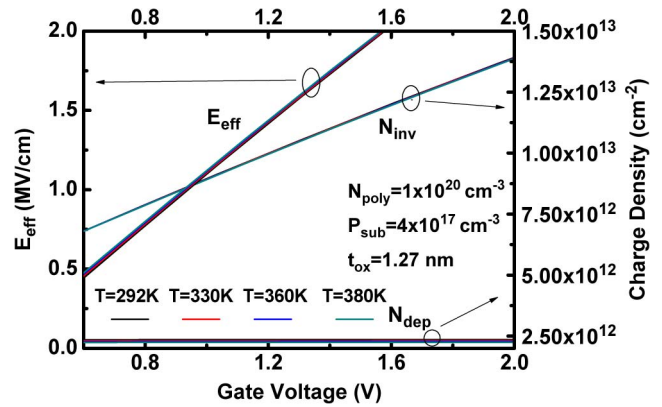

Fig. 4. Simulated vertical effective field, inversion-layer charge density, and substrate depletion charge density versus gate voltage with the temperature as a parameter.

fitting the measured gate capacitance versus the gate voltage (C_g–V_g), as shown in Fig. 1. This was realized with the use of a self-consistent Schrödinger and Poisson's equations solver. Two such solvers were cited: one named Schred [10] and the other in the previous work [11]. Obviously, the two sources [10] and [11] are consistent of each other in the data fitting. Although Cg-Cg data at high gate voltages were seriously distorted due to the prepared ultrathin gate oxide, where the direct tunneling current is profoundly large, the fitting was successfully done in the remaining regions, leading to n+ polysilicon doping concentration $= 1 \times 10^{20}$ cm^{-3}, gate oxide (SiO$_2$) physical thickness $= 1.27$ nm, and p-type substrate doping concentration $= 4 \times 10^{17}$ cm^{-3}. As will be explained in detail later, the NO annealing used may have an impact on the SiO$_2$/Si interface formation but not the SiO$_2$ bulk one.

The ratio of channel width W to length L of the device is 1/1 μm. The channel length direction is along the $\langle 110 \rangle$ direction. We conducted I–V measurements at four temperatures (292, 330, 360, and 380 K). Measured I–V curves across different positions on wafer were found to be comparable with each other. This ensures the integrity of the presented sample. Fig. 2 shows the measured drain current I_d, source current I_s, gate current I_g, and bulk current I_b at drain voltage $V_D =$ 50 mV, plotted versus gate voltage with the temperature as a parameter. The effect of the huge gate tunneling current on the source and drain currents is evidently clear. Similar behaviors

were also observed elsewhere [12]. In this situation, the correct mobility assessment should be formulated as [12]

$$\mu(V_g) = \frac{L}{W} \frac{(I_s(V_g) + I_d(V_g))}{2V_d} \frac{1}{qN_{\text{inv}}(V_g)}. \quad (1)$$

Resulting temperature-dependent mobilities are given in Fig. 3 and plotted versus vertical effective field E_{eff}. Here, E_{eff} followed the well-known expression

$$E_{\text{eff}} = \frac{q(0.5N_{\text{inv}} + N_{\text{dep}})}{\varepsilon_{\text{si}}} \quad (2)$$

where N_{inv} is the inversion-layer charge density, N_{dep} is the substrate depletion charge density, and ε_{si} is the silicon permittivity. With the aforementioned process parameters as inputs, the self-consistent Schrödinger and Poisson's equations solver [11] was executed to furnish N_{inv} and N_{dep}. Corresponding N_{inv}, N_{dep}, and E_{eff} are plotted in Fig. 4 versus gate voltage, with the temperature as a parameter. Moreover, we repeated the case of $V_D = 10$ mV and found that the change is little, as shown in Fig. 3. This ensures the quality of the presented mobility data, particularly for their temperature dependencies.

III. SIMULATION AND EXTRACTION

In the mobility simulation, we employed the self-consistent Schrödinger and Poisson's equations solver [11] to deliver

subbands and wavefunctions while computing the total mobility μ_{total}. Here, μ_{total} was limited to the high-E_{eff} region, where the microscopic scattering by acoustic and optical phonons in the channel region and by the SiO_2/Si surface roughness dominates. Two literature sources were quoted concerning the scattering rate formalisms: one for the phonon scattering rate [2] and the other for both the Gaussian and exponential surface roughness ones [13]. The material parameters used in the phonon scattering rate calculation were the same as in previous work [8]. These two surface roughness scattering rate formalisms are given as follows [13]:

$$\frac{1}{\tau_{\text{SR}}^i(E)} = \frac{m_{\text{dos}}^i e^2 E_{\text{eff}}^2 \Delta^2 \lambda^2}{2\hbar^3} \int_0^{2\pi} \exp\left(-\frac{q^2\lambda^2}{4}\right)(1-\cos\theta)\,d\theta \tag{3}$$

for the Gaussian model and

$$\frac{1}{\tau_{\text{SR}}^i(E)} = \frac{m_{\text{dos}}^i e^2 E_{\text{eff}}^2 \Delta^2 \lambda^2}{2\hbar^3} \int_0^{2\pi} \frac{1}{[1+(\lambda^2 q^2/2)]}(1-\cos\theta)\,d\theta \tag{4}$$

for the exponential model. In (3) and (4), τ_{SR}^i is the scattering rate of subband i, m_{dos}^i is the density-of-states effective mass of subband i, θ is the scattering angle, and $q^2 = 2k^2(1-\cos\theta)$, with $k^2 = 2m_{\text{dos}}^i(E-E_i)/2\hbar^2$. Simulated total mobility with different Δ's and different λ's were used to reproduce universal mobility data [14], [15] in a temperature range comparable with the measurement one in this work, as shown in Figs. 5 and 6 for the Gaussian and exponential models, respectively. The best fitting produces the solutions of Δ and λ, as shown in Fig. 7 for both models. Other values of Δ and λ only led to a poor fitting of the temperature dependencies and had been ruled out. It can be seen from Fig. 7 that Δ is considerably constant and is higher for the Gaussian model, λ has a broad range and is smaller in magnitude for the exponential model, and there is no overlap between the two models. Thus, in the subsequently analysis, λ will be fixed at the middle value, i.e., 14.9 and 23.2 Å for the Gaussian and exponential models, respectively. Accordingly, the values of Δ are 3.1 and 2.7 Å, respectively, which are close to the published values in the thick-gate-oxide case [1]–[4]. This dictates the applicability of the proposed temperature-dependent extraction process.

However, we found that, with the aforementioned Δ and λ values, simulated results cannot match all observed temperature dependencies of mobilities in a 1.27-nm sample. As shown in Figs. 8 and 9 for both models, simulated mobilities at 292, 330, and 360 K fall below data points, despite the apparent coincidence for the remaining temperature (380 K). Since this is physically unreasonable, the value of Δ must be reduced. The case of reducing Δ to lower values is depicted in these two figures.

The required reduction in Δ indicates the existence of the remote scatterers. In this sense, the additional mobility μ_{add} due to the remote scatterers, ionized substrate impurity atoms,
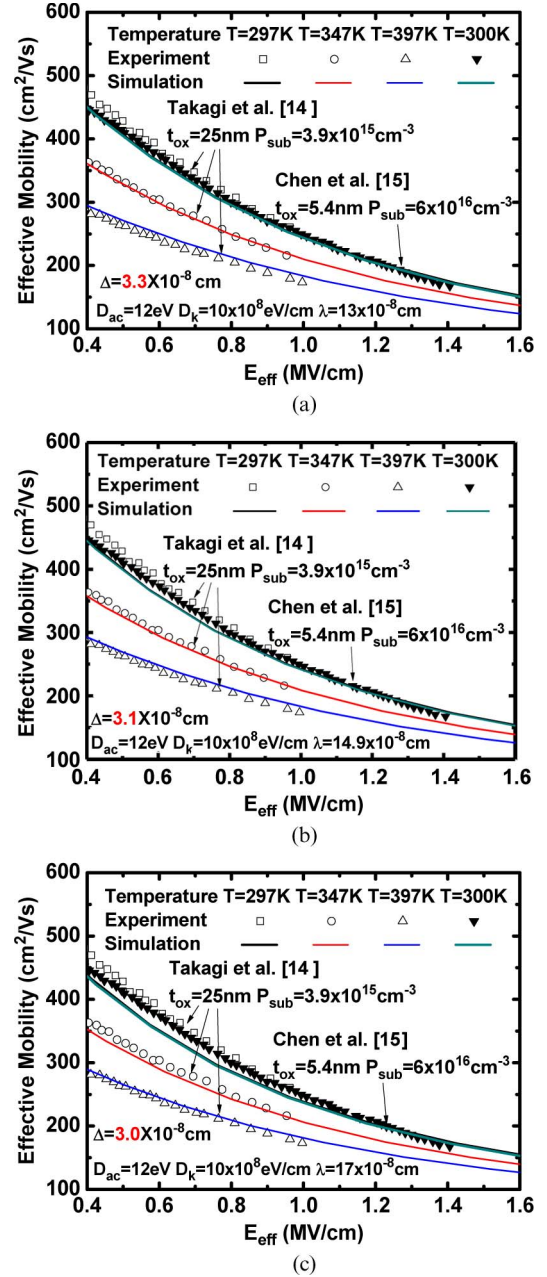

Fig. 5. Comparison of the experimental electron universal mobility curves for (open symbols) three temperatures [14] and (filled symbols) one temperature [15] with the (lines) simulated ones in this work for the Gaussian model. (a) $\Delta = 3.3$ Å, and $\lambda = 13$ Å. (b) $\Delta = 3.1$ Å, and $\lambda = 14.9$ Å. (c) $\Delta = 3.0$ Å, and $\lambda = 17$ Å. D_{ac} is the acoustic deformation potential. D_k is the deformation potential of the kth intervalley phonon.

and interface traps can be defined according to Matthiessen's rule, i.e.,

$$\frac{1}{\mu_{\text{eff}}} = \frac{1}{\mu_{\text{total}}} + \frac{1}{\mu_{\text{add}}} \tag{5}$$

where μ_{eff} is the measured mobility [i.e., (1)], and μ_{total} is the simulated total mobility that does not include the contributions by remote scatterers, substrate impurity atoms, or interface traps. Note that Matthiessen's rule can empirically apply as long as the undertaken E_{eff} or N_{inv} is high enough [16]. The effect of substrate impurity atoms or interface traps

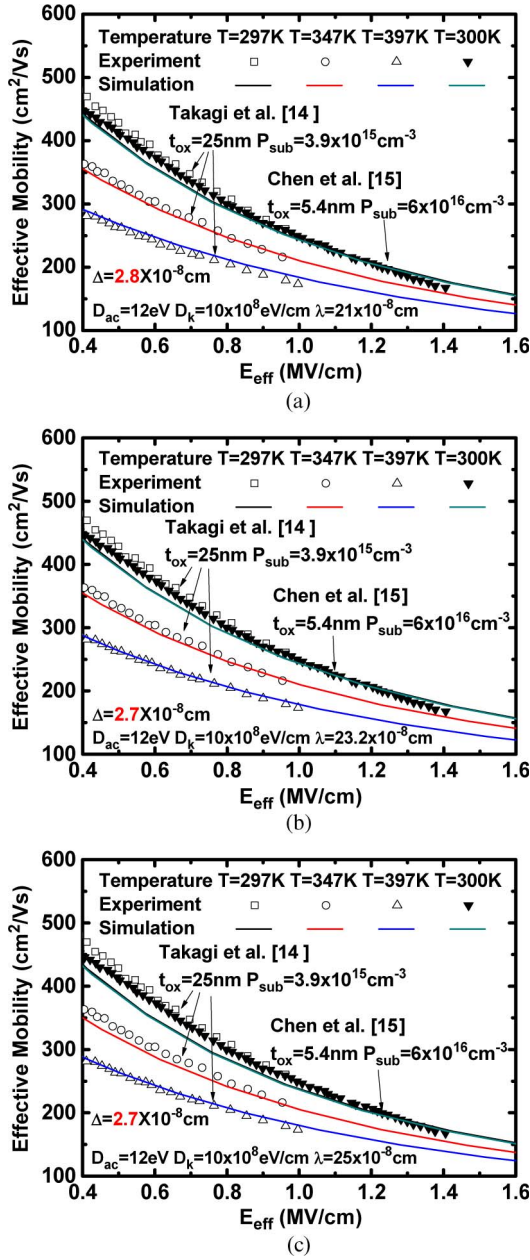Fig. 7. Best-fitting results of Δ versus λ for both the Gaussian and exponential models.

Fig. 6. Comparison of the experimental electron universal mobility curves for (open symbols) three temperatures [14] and (filled symbols) one temperature [15] with the (lines) simulated ones for the exponential model. (a) $\Delta = 2.8$ Å, and $\lambda = 21$ Å. (b) $\Delta = 2.7$ Å, and $\lambda = 23.2$ Å. (c) $\Delta = 2.7$ Å, and $\lambda = 25$ Å.

Fig. 8. Comparison of the (symbols) temperature-dependent electron effective mobility data with the simulated mobility curves using the Gaussian model for (a) Δ of (dashed line) 1.4 Å and (solid line) 3.1 Å, and (b) Δ of (dashed line) 1.2 Å and (solid line) 2.8 Å. $\lambda = 14.9$ Å.

IV. TEM MEASUREMENT AND ANALYSIS

In performing TEM measurements, the sample was 1000 nm long, and its cross-section thickness had a range of 20–60 nm. A TEM image was created, as shown in Fig. 11. In this picture, the labeled $\langle 110 \rangle$ direction is parallel to the SiO_2/Si interface, whereas the $\langle 001 \rangle$ direction is normal to the interface. Underlying λ_m and Δ_m were determined by following the work of Goodnick *et al.* [1]. First, digitalization of surface roughness was done by directly counting lattice points on the TEM photographs. The same sampling interval (1.92 Å) [1] was used. This led to the autocovariance function

can also be suppressed in the high-E_{eff} region. In Fig. 10, we show the extracted μ_{add} at N_{inv} of 1×10^{13} cm^{-2}, with Δ as a parameter, along with the two separate curves for the simulated Coulomb-drag-limited mobilities [5]. These two Coulomb-drag-limited mobility curves represent two limiting conditions of the Landau-damping wave vector: one for "zero-temperature Landau damping wave vector" and the other for "damping at Thomas Fermi screening wave vector" [5]. According to Fischetti [5], the realistic Coulomb-drag-limited mobility is likely to be situated between the two limits. In this sense, the actual Δ of the presented sample should be approximately 1.3 and 1.0 Å for the Gaussian and exponential models, respectively.
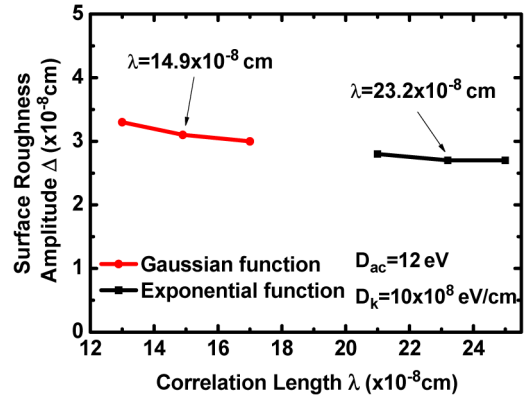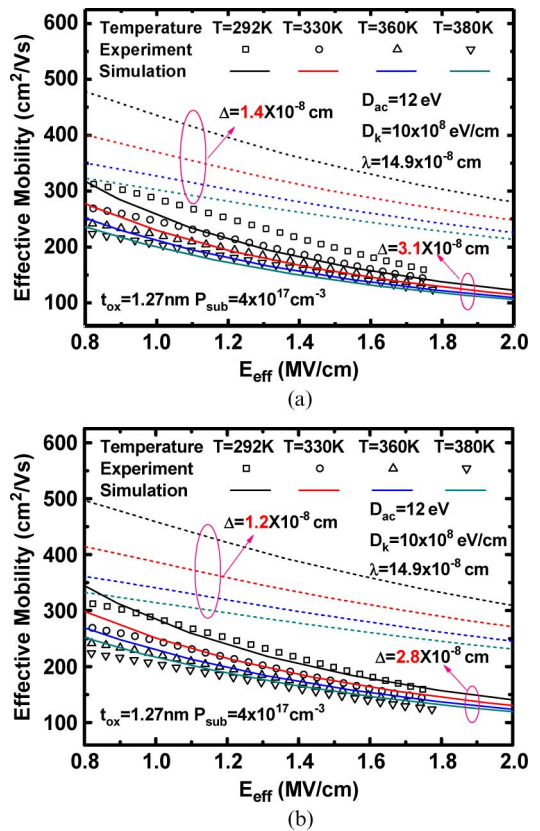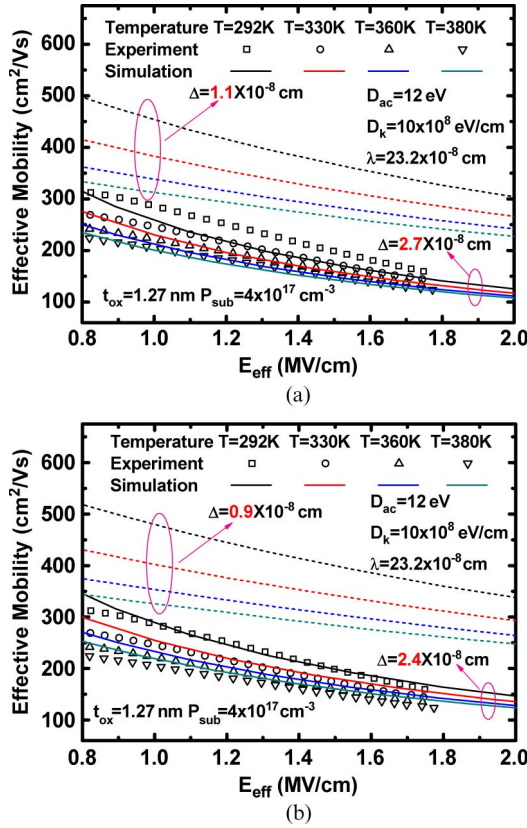
(a)

(b)

Fig. 9. Comparison of the (symbols) temperature-dependent electron effective mobility data with the simulated mobility curves using the exponential model for (a) Δ of (dashed line) 1.1 Å and (solid line) 2.7 Å and (b) Δ of (dashed line) 0.9 Å and (solid line) 2.4 Å. λ = 23.2 Å.
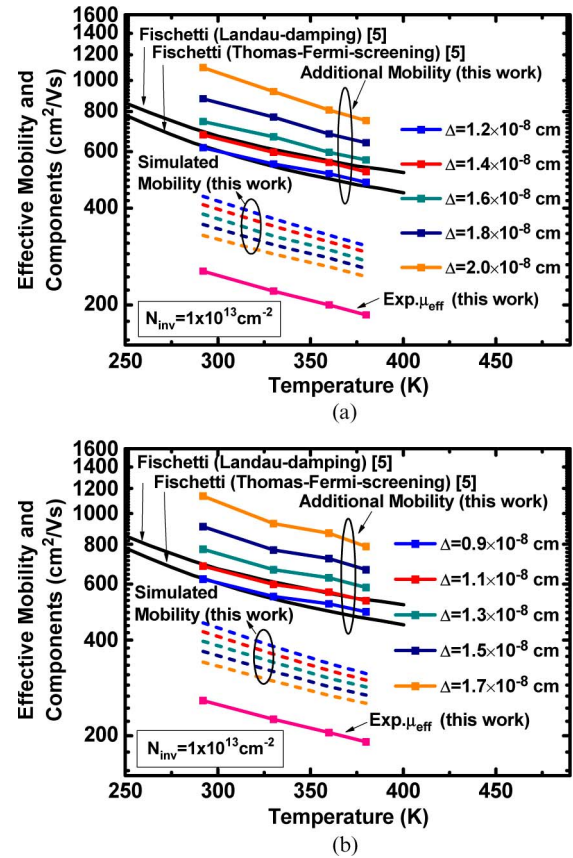

(a)

(b)

Fig. 10. Temperature dependence of the measured effective mobility, simulated mobility, and extracted additional mobility, all made at a fixed inversion-layer density of 1×10^{13} cm^{-2} to make a fair comparison with simulated interface-plasmons-limited mobility [5]. Simulated mobility and additional mobility are presented as a function of Δ. (a) Gaussian model. (b) exponential model.

in Fig. 12 as a function of the distance. In the figure, the squared root of the autocovariance at zero distance yields Δ_m of around 1.2 Å. Data fitting was carried out, producing $\lambda_m =$ 15.6 and 23.1 Å for the Gaussian and exponential models, respectively.

Straightforwardly, several key arguments can be drawn. First, the sample length effect [1] may be neglected due to a long sample used. Thus, the ratio of $\lambda_m/\lambda \approx 1.0$ is reached accordingly [1]. Strikingly, this is the fact because the extracted values of $\lambda_m =$ 15.6 and 23.1 Å in this work separately are close to those (14.9 and 23.2 Å) of λ. One of the arguments can thereby be inferred: the sample length effect as cited in [1] can act to be corroborating evidence for the temperature-dependent extraction method. Second, the TEM 2-D projection correction coefficient Δ_m/Δ is approximately 1.0, valid for both the Gaussian and exponential models. However, the current thick-gate-oxide-based knowledge [1] cannot reasonably explain this because, for the TEM sample cross-section thickness range of 20–60 nm as in our work, the theoretical calculation pointed out [1] that the upper limit of Δ_m/Δ decreases sharply from 0.7 (see [1]). Even the Δ_m/Δ in this work is much higher than the published experimental Δ_m/Δ values of 0.50–0.71 [8]. We attribute such significant deviations to the sole use of the ultrathin gate oxide (1.27 nm) in this work. It is therefore suggested that further theoretical investigation of the TEM sample cross-section thickness effect is needed, particularly for the ultrathin-gate-oxide situation.
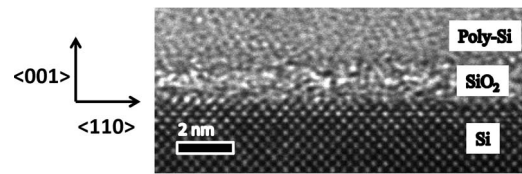

Fig. 11. TEM image of the sample.

Finally, we want to stress that the physical gate oxide thickness can be estimated from the TEM picture in Fig. 11, and it appears to be in proximity of 1.27 nm, which is the value of Cg-Vg fitting. The same gate oxide thickness had earlier been applied to p-type counterparts on the same wafer [17]. This strongly suggests that the presented SiO$_2$ bulk film was less nitrided during the NO annealing. Moreover, according to the literature [4], the use of the oxide nitridation process will produce a smoother Si/SiO$_2$ interface in terms of a reduced Δ. Extra traps may be created during the pure nitridation or mixed one (i.e., NO annealing process); however, their effect might be limited to the low-E_{eff} region, rather than the high-E_{eff} region where this work was focused on. Therefore, it is argued that the mixed NO annealing used may have an impact on the SiO$_2$/Si interface formation but not the SiO$_2$ bulk one.
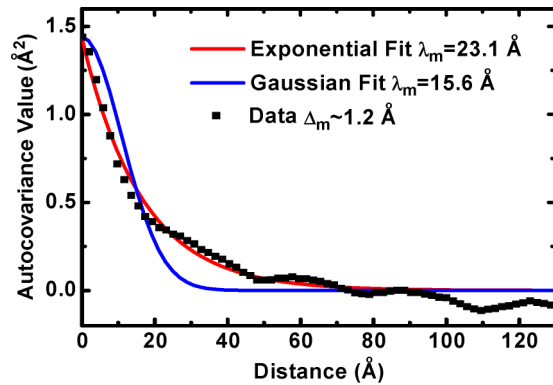
Fig. 12. Autocovariance function extracted from the TEM photograph as a function of distance. Both the Gaussian and exponential fits are shown.

V. CONCLUSION

Electron mobility of a 1.27-nm gate-oxide nMOSFET sample has been measured at various temperatures. Temperature-dependent numerical simulation has for the first time transformed existing universal mobility data into the solutions of surface roughness parameters and has been applied to the presented sample, taking into account the available Coulomb-drag-limited mobilities. The extracted surface roughness parameters have been correlated with the values from TEM measurements. As a consequence, novel results have been created and might substantially improve the current understanding of interface roughness, particularly for the case of ultrathin gate oxides.

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