A New AMOLED Pixel Circuit With Pulsed Drive and Reverse Bias to Alleviate OLED Degradation

Kuei-Yu Lee and Paul C.-P. Chao, *Member, IEEE*

***Abstract*—This paper proposes a new pixel circuit for an active matrix organic light-emitting diode (OLED) display, which consists of five thin-film transistors (TFTs) and one capacitor. This circuit develops techniques of pulsed drive and reverse bias to achieve desired emitted brightness levels and elongate OLED life times, respectively. A current mirror is also adopted in the circuit to minimize emission nonuniformity of the OLED panel. The required input data voltages for varied displayed gray levels are calculated based on analytically known TFT and OLED models and the designed circuit architecture. The designed pixel circuit is simulated with realistic TFT models for validating expected performance to realize 256 gray levels and minimizing nonuniformity. The designed circuit is implemented in a 2.4-in quarter video graphics array panel, which shows favorable performance for minimizing display nonuniformity and alleviating OLED degradation. In addition, a closeness is clearly observed among analytical predictions, simulations, and experimental measurements.**

***Index Terms*—Active matrix organic light-emitting diode (AMOLED), OLED degradation, pulsed drive, reverse bias, thin-film transistors (TFTs), threshold compensation.**

I. Introduction

ACTIVE matrix organic light-emitting diode (AMOLED) displays have drawn much attention recently due to various advantages, such as high brightness, good efficiency, wide viewing angles, fast responses (< 1 μs), and simple structures [1]. However, AMOLED displays face some serious drawbacks nowadays, like emission nonuniformity of an AMOLED panel and OLED degradation. The nonuniformity is generally considered to be due to threshold voltage ($V_{\rm th}$) shift among long-time-operated amorphous silicon thin-film transistors (a-si TFT) [2], called "dc stress degradation" [3], or $V_{\rm th}$ mismatch among low-temperature polycrystalline silicon thin-film transistor (LTPS-TFT), which results from diverse grain distribution in the process [4]. A number of past works on pixel circuit design were proposed to compensate the effects. The presented methods can be categorized into voltage-mode drives [5] and current modes [6]. The problems of the $V_{\rm th}$ mismatches are gradually improved with the advancements of thin-film transistor (TFT) fabrication processing and newly developed compensation methods. Another serious problem of the AMOLED display is the degradation in OLED emitted luminance and resulting shortened lifetime. This problem becomes detrimental as the OLED display is expected to replace large-sized and full high-definition liquid crystal display TVs in the future.

On the other hand, the lifetime degradation of the OLED component has been investigated by few past works [7]–[11], where the degradation was attributed to intrinsic and extrinsic causes. The extrinsic causes are, for example, particle contamination and inevitable humidification [7] in the fabrication process. As for the intrinsics, they are due to accumulative holes [8], the impurity of movable ions [9], [10], and the Indium diffusion [11] induced by high-density large currents under long-time driving. To tackle the OLED degradation due to long-time current drives, some compensation methods were developed in a few past works [12]. With the OLED degradation estimated via detecting its cross voltage in long-time driving, the compensations in [12] proposed current compensation approaches, where the current through an OLED component was intentionally adjusted larger to maintain the originally designed emitted luminance. However, it often aggravates OLED degradation due to larger currents. To solve the problem, this paper proposes a new pixel circuit that incorporates the techniques of pulsed drive and reverse bias to alleviate OLED degradation for longer lifetimes. The effects of pulsed drives on OLED emitted luminance were first discussed by Luo *et al.* [13]. This work used the current drives in different duty ratios to a single OLED component and then recorded the resulting OLED degradation curves. It was shown that even for different OLED materials the pulsed drives render positive influence on alleviating OLED degradation. As for reverse bias, Si *et al.* [14] imposed reverse biases on OLED in a nonemission period in each frame for a 3T1C pixel circuit. This work did not, however, offer experimental validation. Yahiro *et al.* [15] used a single OLED to experimentally show the capability of the reverse bias to alleviate OLED degradation.

Employing both aforementioned methods of pulsed drive and reverse bias, this paper proposes a new OLED pixel circuit that includes five TFTs and one capacitor (5T1C). The two methods are implemented together within a pixel circuit for the first time. The designed pulsed drive is a voltage-mode drive that is easy for realizing high-resolution gray levels up to 256 with current-drive periods, whereas the reverse bias is imposed on an OLED in the designed current-off periods. This special drive is proven effective in alleviating OLED degradation. In addition, the designed pixel circuit and timing offer the baseline merits of panel

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The authors are with the Department of Electrical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: pchao@mail.nctu.edu.tw).

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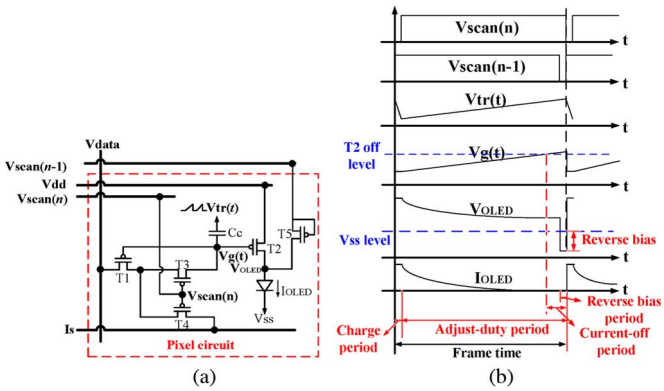

Fig. 1. (a) Proposed pixel circuit. (b) Associated timing diagram.

nonuniformity compensation via a current mirror. With design in hands, the circuit dynamics is simulated by HSPICE to show the expected performance, which is followed by the fabrication of a 2.4-in quarter video graphics array (QVGA) OLED panel with the designed circuit implemented. The measurements of the OLED-emitted luminance recorded in an extended period of time confirm that the proposed combined methods of pulsed drive and reverse bias are well capable of alleviating OLED degradation while realizing 8-bit gray levels.

This paper is organized as follows. Section II states the design and operation of the new pixel circuit and its accompanying timing diagram. It presents the capabilities of the designed pixel circuit for implementing pulsed drive, reverse bias, panel nonuniformity compensation, and displaying 8-bit gray levels. Section III presents simulated results. Section IV validates experimentally the performances of gray level realization by pulsed drive and OLED degradation alleviation by reverse bias.

II. Design of the New Pixel Circuit

A. Implementing Pulsed Drive and Reverse Bias

The proposed new drive pixel circuit is shown in Fig. 1(a), which is composed of five TFTs and one capacitor, whereas Fig. 1(b) illustrates the associated timing diagram. The entire frame time is designed to have both charge and adjust-duty periods other than reverse bias period at the end. The TFTs of T_1 and T_2 form a current mirror, whereas T_3 and T_4 perform as switches for the charge period, as shown in Fig. 1(a). T_5 is a switch for realizing the operation of reverse bias. C_c is a storage capacitor. $V_{\rm scan}(n)$ and $V_{\rm data}$ are those signals provided by the scan and data lines, respectively, in which $V_{\rm scan}(n)$ is responsible for addressing rows, whereas $V_{\rm data}$ provides signals to control the OLED current, then adjusting the luminance level. On the other hand, $V_{\rm scan}(n)$ represents the scan waveform for the nth row, controlling T_3 and T_4, whereas $V_{\rm scan}(n-1)$ does T_5. $V_{\rm tr}(t)$ is a predesigned triangular waveform with the aim to generate current-off periods for alleviating OLED degradation. $V_g(t)$ denotes the resulting gate voltage of T_2 that is determined by $V_{\rm data}$. $V_{\rm OLED}$ is the voltage at the OLED anode, whereas $I_{\rm OLED}$ represents the OLED drive current.

Fig. 2(a)–(d) illustrates four different operation stages of the proposed OLED pixel circuit: 1) the transient charge period; 2) the steady-state charge period; 3) the adjust-duty period; and 4) the reverse bias period. In the first stage, the transient charge period, as shown in Fig. 2(a), $V_{\rm scan}(n)$ is designed at the low voltage level such that T_3 and T_4 turn on. The storage capacitor C_c is then charged until it is full, whereas current I_c stays zero, as shown in Fig. 2(b). At this steady-state period, the drain current of T_1 is set to I_s since current I_c stays zero. $V_{\rm GS}$ of T_1 is fixed; thus, for T_1

$$I_s = K_{T1}\left(V_{{\rm GS},T1} + |V_{{\rm TH},T1}|\right)^2 \tag{1}$$

where

$$K_{T1} = \frac{1}{2} C_{\rm ox1} \mu_1 \frac{W_1}{L_1} \tag{1a}$$

which contains gate capacitance $C_{\rm ox1}$, mobility μ_1, and TFT aspect ratio of T_1, W_1/L_1. In addition, $V_{{\rm TH},T1}$ is the threshold voltage of T_1. Equation (1) can be rewritten as

$$I_s = K_{T1}\left(V_g(t) - V_{\rm data} + |V_{{\rm TH},T1}|\right)^2. \tag{2}$$

Rearrangement of (2) gives the gate voltage of T_2 as

$$V_g(t) = V_{\rm data} - |V_{{\rm TH},T1}| - \sqrt{I_s/K_{T1}}. \tag{3}$$

The foregoing equation reveals that a predesignated $V_{\rm data}$ affects linearly $V_g(t)$, the gate voltage of drive TFT T_2 for OLED. Thus, $V_{\rm data}$ effectively controls the OLED current $I_{\rm OLED}$ for desired luminance in the subsequent charge period. This way, the OLED current can easily be controlled by a voltage signal $V_{\rm data}$ instead of an external current source [6], which paves the way to an easy control on the gray level of OLED emission. In the next stage, the adjust-duty period, $V_{\rm scan}(n)$ provides high levels of voltage such that T_3 and T_4 are turned off, as shown in Fig. 2(c). In the mean time, $V_g(t)$ is increased by the triangular wave $V_{\rm tr}(t)$, as shown in Fig. 1(b), until T_2 is turned off. This happens when $V_g(t)$ is raised to the value, which makes $V_{\rm GS}$ of T_2 smaller than the threshold voltage of T_2, i.e.,

$$|V_g(t) - V_{\rm dd}| < |V_{{\rm TH},T2}|. \tag{4}$$

The turn-off of T_2 actually leads to a current-off period for $I_{\rm OLED}$, as shown in Fig. 1(b). Finally, the current-off period is extended and embeds a subperiod of reverse-bias period, where reverse bias is applied, as shown in Fig. 2(d). In this period, $V_{\rm scan}(n-1)$ is designed to be at a low level such that T_5 is turned on; thus, the anode voltage of the OLED is reversed biased. It is applied in each frame to alleviate OLED degradation.

The gray level of OLED emission is determined by the time integration of $I_{\rm OLED}$ in Fig. 1(b). The time integration on $I_{\rm OLED}$ is the integration over a pulse waveform since $I_{\rm OLED}$ keeps constant at charge periods, follows a parabolic-curve-like decline in the adjust-duty period, and finally stays at the zero level in the current-off period. The emitted luminances are seen by human eyes without flickering since the frame frequency is always larger than 60 Hz. By adjusting the predesigned triangular waveform $V_{\rm tr}(t)$, one is able to control durations of adjust-duty and current-off periods, thus tuning the emitted luminance of the OLED pixel. The ability of controlling the

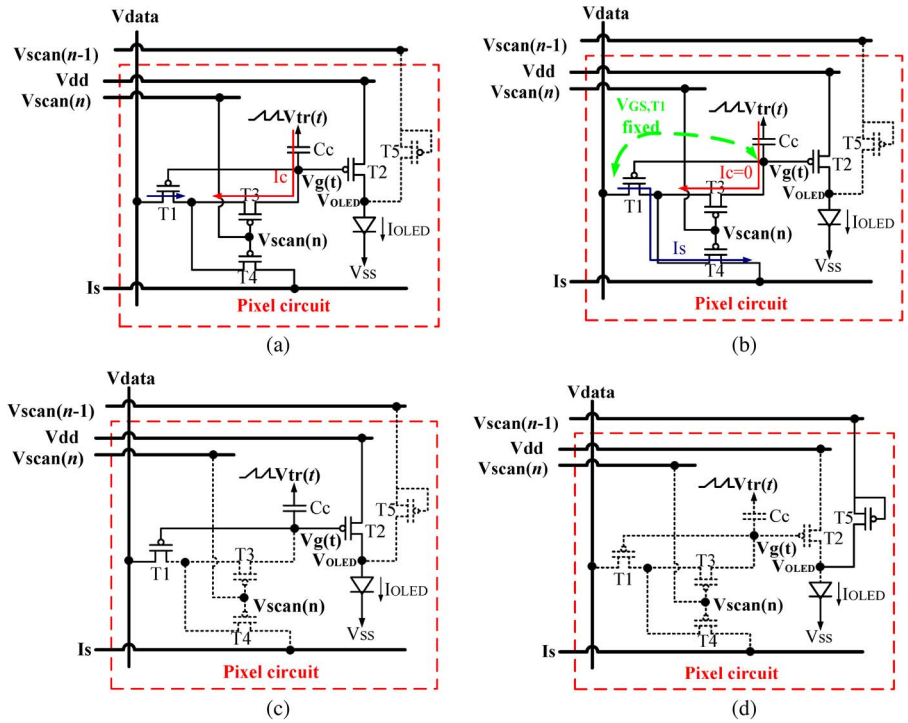

Fig. 2. Operations of the proposed circuit in (a) the transient charge period, (b) the steady-state charge period, (c) the adjust-duty period, and (d) the reverse bias period within the current-off period.

duty for nonzero OLED currents categorizes the present addressing scheme as a method of pulsed drive. Pixel designers would be able to choose appropriate levels of $V_{\rm data}$ and $V_{\rm tr}(t)$ to control the emitted OLED gray level for initiation of the current-off period, and $V_{\rm scan}(n-1)$ for a reverse bias period in the current-off period to alleviate the OLED degradation.

B. Minimizing Panel Nonuniformity

The new pixel circuit also offers the baseline merit of compensating panel nonuniformity, in addition to the aforementioned degradation alleviation. The compensation is made possible to compensate TFT $V_{\rm th}$ mismatches by the current mirror pair of T_1 and T_2, as shown in Fig. 1(a). T_1 and T_2 create a current mirror that is used to control the drain current through T_2, which is also the OLED drive current. Based on the basic operation principles of a TFT, the OLED current, i.e., the drain current of T_2, can be derived as

$$I_{\rm OLED} = I_{D,T2} = K_{T2}\Big(V_{\rm data} - |V_{\rm TH,T1}| - \sqrt{I_s/K_{T1}} - V_{\rm dd} + |V_{\rm TH,T2}|\Big)^2 \quad (5)$$

where K_{T2} is composed of mobility, gate capacitor $C_{\rm ox}$, and the aspect ratio of T_2. $V_{\rm TH,T2}$ is the threshold voltage of T_2. If the TFTs are fabricated from the same fabrication process, $V_{\rm TH,T1}$ and $V_{\rm TH,T2}$ are considered approximately cancellable by each other. The drain current equation of $I_{\rm OLED}$ is then

$$I_{\rm OLED} = K_{T2}\left(V_{\rm data} - V_{\rm dd} - \sqrt{I_s/K_{T1}}\right)^2 \quad (6)$$

which makes the design work easier to render the desired gray level of $I_{\rm OLED}$ with a given $V_{\rm data}$ since $V_{\rm TH,T1}$ and $V_{\rm TH,T2}$ are assumed identical and cancel each other. Note that this cancellation between $V_{\rm TH,T1}$ and $V_{\rm TH,T2}$ can also ease dc stress degradation, since the degradation effect can be modeled in some degree as $V_{\rm th}$ shifts in the square law of TFT current equation [3]. However, due to varied sizes (W/L) of T_1 and T_2 and different temperatures and processes, the difference between $V_{\rm TH,T1}$ and $V_{\rm TH,T2}$ does exist. Moreover, mobilities of T_1 and T_2 are also varied due to the same reasons, and different dc stress degradations on T_1 and T_2 lead to different $V_{\rm TH}$ shifts. These all lead to errors in designating OLED drive current $I_{\rm OLED}$. To suppress the negative effects from these variations, Monte Carlo simulations are conducted to estimate the variations in the resulting OLED drive [16] in the next section for confirming the tolerable emission nonuniformity of an OLED panel.

C. Realizing Gray Level

This paper is next focused on how to designate the range and resolution of $V_{\rm data}$ for targeted displayed gray levels of the OLEDs. As for the present pixel circuit design in voltage mode, shown in Fig. 1(a), the luminance at varied gray levels is proportional to the time integration of $I_{\rm OLED}$ over a frame time, as shown in Fig. 1(b). Since $I_{\rm OLED}$ changes in a frame over two stages, i.e., the charge and adjust-duty periods, before it reaches zero, the calculation of the gray level is carried out for two different stages. For the charge period, the integration on (6) for $I_{\rm OLED}$ gives

$$\bar{I}_{\rm OLED,ch} = \frac{T_f}{N}\left[K_{T2}\left(V_{\rm data} - V_{\rm dd} - \sqrt{I_s/K_{T1}}\right)^2\right] \quad (7)$$

where N is the row numbers of OLED panel, and T_f is the frame time. In the adjust-duty period, since $V_g(t)$ is increased

by the triangular waveform $V_{\rm tr}(t)$, the initiating timing for the current-off period is when $V_g(t)$ reaches $(V_{\rm dd}-|V_{{\rm TH},T2}|)$. The time evolution of the gate voltage of T_2 can be derived as

$$V_{g,\rm duty}=\left(V_{\rm data}-|V_{{\rm TH},T1}|-\sqrt{I_s/K_{T1}}\right)+\left(\frac{V_{\rm dd}-|V_{{\rm TH},T2}|-V_{\rm data}+|V_{{\rm TH},T1}|+\sqrt{I_s/K_{T1}}}{[(N-1)/N]\cdot T_f}\right)\cdot t \quad (8)$$

where $\{[(N-1)/N]T_f\}$ is the time span for the adjust-duty period in a frame time. Thus, the drain current of T_2, i.e., $I_{\rm OLED,ad}$, in the adjust-duty period can be calculated and shown as

$$I_{\rm OLED,ad}=K_{T2}\left(V_{\rm data}-|V_{{\rm TH},T1}|-\sqrt{I_s/K_{T1}}+\left(\frac{V_{\rm dd}-|V_{{\rm TH},T2}|-V_{\rm data}+|V_{{\rm TH},T1}|+\sqrt{I_s/K_{T1}}}{[(N-1)/N]\cdot T_f}\right)\cdot t-V_{\rm dd}+|V_{{\rm TH},T2}|\right)^2. \quad (9)$$

The foregoing equation is integrated over time in the adjust-duty period for estimating emitted OLED luminance, yielding

$$\bar{I}_{\rm OLED,ad}=\int_{\left(\frac{T_f}{N}\right)}^{T_f} K_{T2}\times\left[V_{\rm data}-|V_{{\rm TH},T1}|-\sqrt{I_s/K_{T1}}+\left(\frac{V_{\rm dd}-|V_{{\rm TH},T2}|-V_{\rm data}+|V_{{\rm TH},T1}|+\sqrt{I_s/K_{T1}}}{[(N-1)/N]\cdot T_f}\right)\cdot t-V_{\rm dd}+|V_{{\rm TH},T2}|\right]^2 dt. \quad (10)$$

The preceding OLED current is integrated to obtain the estimated average luminance sensed by human over time, i.e., the visualized OLED luminance. The emitted OLED luminance can be regarded in a linear relationship to the average OLED-driven current based on time integration over frame time. This way, the total emitted luminance per frame time L is approximately proportional to the integration of $I_{\rm OLED}$ over the entire frame, denoted by $\bar{I}_{\rm OLED,total}$, which pertains to two periods, as shown in Fig. 1(b), the charge and adjust-duty periods. Thus, $\bar{I}_{\rm OLED,total}$ is equal to the sum of calculated $\bar{I}_{\rm OLED,ch}$ and $\bar{I}_{\rm OLED,ad}$ by (7) and (10), respectively, yielding (11), shown at the bottom of the page, where α is the proportionality constant relating luminance to current integration. Note from (7) and (10) that $\bar{I}_{\rm OLED,ch}$ and $\bar{I}_{\rm OLED,ad}$ are both quadratic-like functions of $V_{\rm data}$, even with some terms in (7) and (10) being not related to $V_{\rm data}$. Their contributions to L are in fact small as compared with other terms. Henceforth, the OLED emitted luminance L can be approximated well in the sense of proportionality to $\bar{I}_{\rm OLED,\ total}$ in (11), which is in fact a quadratic-like function of $V_{\rm data}$. Note that the resulting quadratic-like relation between the input data voltage $V_{\rm data}$ and the resulting luminance L facilitates well the important task of gamma correction [17] in displaying varied gray levels. Calculations are conducted to depict this quadratic relation between L and $V_{\rm data}$, which is shown in Fig. 3 with a normalized luminance L for the ordinate. In this figure, a quadratic-like relation is clearly seen, which demonstrate well an easy implementation of gamma correction.

III. Simulations

A. Displaying Gray Levels With Designed Pulsed Drive

The software HSPICE is utilized herein to simulate the electronic dynamics of the newly-designed LTPS-TFT (LEVEL 62) pixel circuit for a QVGA OLED display. The frame frequency is assumed as 60 Hz, which corresponds to the flickering limit of human vision and a standard setting of a TV. The charge period is set as 70 μs based on the calculation for 240 rows. In addition, shown in Fig. 1(a) is the triangular wave $V_{\rm tr}(t)$ set from 5 to 15 V, whereas the scan line signal $V_{\rm scan}$ is from -10 to 15 V. Finally, $V_{\rm dd}$ is 5 V. $V_{\rm ss}$ is -7.5 V, and I_s is 0.1 μA, as in Table I. The aspect ratios (W/L) of switch TFTs, T_1, T_3, T_4, and T_5, in the pixel circuit, as shown in Fig. 1(a), are set

$$L=\alpha\left\{\frac{Tf}{N}\left[K_{T2}\left(V_{\rm data}-V_{\rm dd}-\sqrt{I_s/K_{T1}}\right)^2\right]+\int_{\left(\frac{Tf}{N}\right)}^{Tf} K_{T2}\left[V_{\rm data}-|V_{{\rm TH},T1}|-\sqrt{I_s/K_{T1}}+\left(\frac{V_{\rm dd}-|V_{{\rm TH},T2}|-V_{\rm data}+|V_{{\rm TH},T1}|+\sqrt{I_s/K_{T1}}}{[(N-1)/N]\cdot T_f}\right)\cdot t-V_{\rm dd}+|V_{{\rm TH},T2}|\right]^2 dt\right\} \quad (11)$$

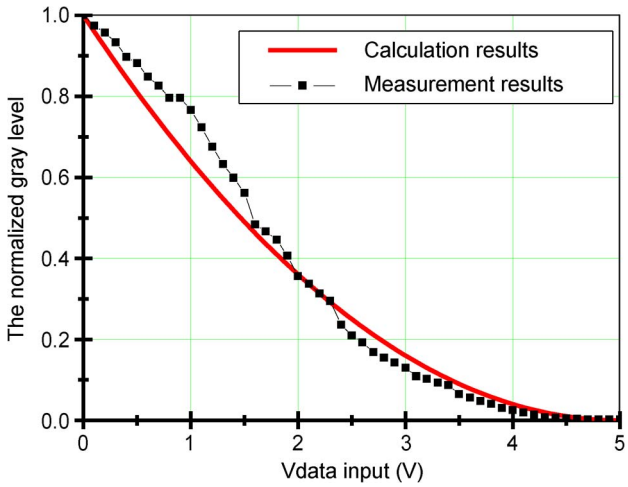

Fig. 3. Normalized gray level versus input data voltage.

TABLE I
PARAMETER VALUES FOR SIMULATIONS

Parameter	Magnitude
V_{dd}	5(V)
$V_{scan}(n)$ and $V_{scan}(n\text{-}1)$	-10~15(V)
V_{data}	0~5(V)
V_{ss}	-7.5(V)
I_s	0.1(uA)
$V_{tr}(t)$	5~15(V)
TFT aspect ratios (W/L)	6/6 for T_1, T_3, T_4, and T_5 4/20 for T_2

identically to be 6 μm/6 μm, whereas the driving TFT T_2 is set to be 4 μm/20 μm.

To show the capability of the proposed pixel circuit to display 256 gray levels, the following simulations are conducted. $V_{\rm data}$ is set from 0 to 5 V for 256 gray levels with 0.025 V for distinguishing a single gray level. Shown in Fig. 4 are the simulated curves representing different output currents driven by the designed pixel circuit in a frame time of 17 ms, with $V_{\rm data}$ ranging from 0 to 5 V. These curves are seen with different declining trends and levels within the displayed frame time, which contributes to displaying different gray levels from the highest to the lowest, proving that the new pixel circuit is able to display varied gray levels.

B. Application of Reverse Bias

Simulations are also conducted to observe the application of reverse bias in the current-off period. The simulated results are shown in Fig. 5, where it is seen that $V_{\rm ss}$ is set as -7.5 V, and the OLED anode voltage $V_{\rm OLED}$ is gradually decreased in the frame time to -6 V before the cutoff period, keeping the cross voltage of the OLED greater than 1.5 V for emission. At the end of the current-off period, there is a reverse bias period where

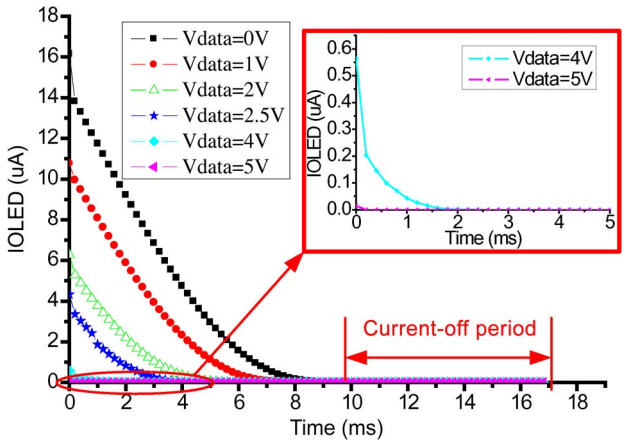

Fig. 4. Simulated $I_{\rm OLED}(t)$ with $V_{\rm data}$ ranging from 0 to 5 V.

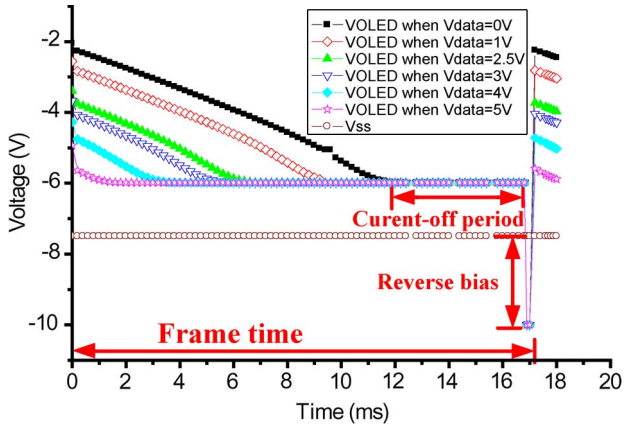

Fig. 5. Simulated $V_{\rm OLED}(t)$ with $V_{\rm data}$ ranging from 0 to 5 V.

TABLE II
TYPICAL VARIATIONS OF LTPS-TFT PARAMETERS

	V_{th}(V)	U_o(cm^2/V-S)	I_{err}(uA)
Average	-2	95	0.1
Standard deviation	1	3	0.005

the voltages of the OLED anodes $V_{\rm OLED}$ are seen intentionally pulled down by $V_{\rm scan}(n-1)$ to -10 V, successfully realizing reverse biasing on the OLED component.

C. Compensation Effects

Monte Carlo simulations on the HSPICE model of the proposed circuit are conducted to show tolerable panel emission nonuniformity considering the variation of three parameters: 1) threshold voltage $V_{\rm th}$; 2) mobility U_o; and 3) current source error $I_{\rm err}$. Gaussian distributions are assumed for the aforementioned three variations. They are listed in Table II with corresponding averages and standard deviations. Monte Carlo simulations on the conventional 2T1C and proposed 5T1C pixel circuits are next conducted 20 times, and the results are compared. As shown in Fig. 6(a) and (b), the average drive current offered by the proposed 5T1C circuit renders only the

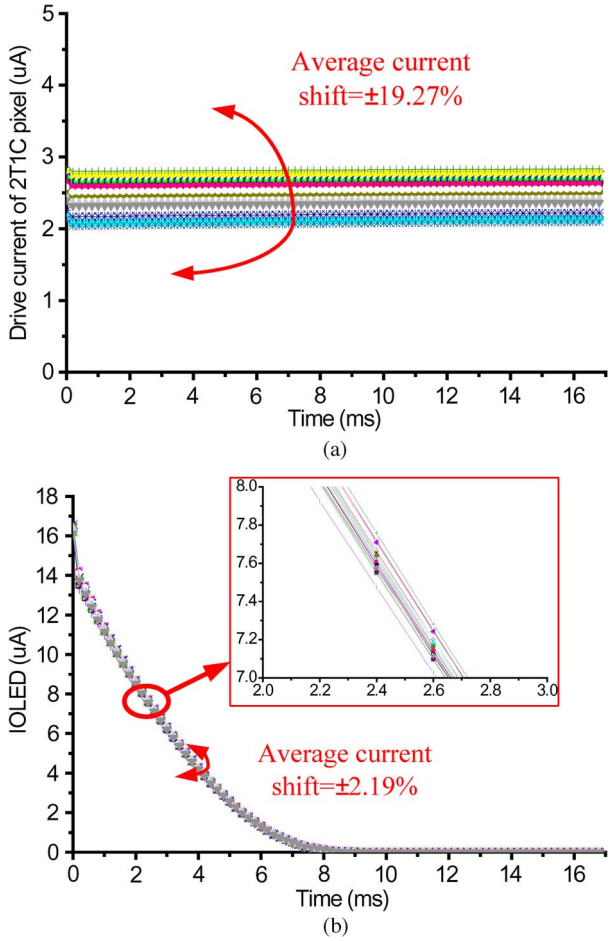

Fig. 6. Simulations of the average current with considering variations and Monte Carlo simulations for (a) conventional 2T1C and (b) new 5T1C pixel circuit.

variation of ±2.19%, whereas the conventional 2T1C leads to ±19.27%.

IV. Measurements

A. Fabrications

A 2.4-in QVGA OLED display panel is fabricated in the laboratory for performance testing. The panel is designed and implemented with top-emitting OLEDs, the pixel circuits proposed in this paper, and a triangular waveform generator realized by the gate-driver-on-array process. Fig. 7 shows the designed layouts of subpixels for red, green, and blue colors. The aspect ratios (W/L) of switch TFTs T_1, T_3, T_4 and T_5 in the pixel circuit, as shown in Fig. 1(a), are designed identically to be 6 μm/6 μm, whereas the driving TFT T_2 is designed to be 4 μm/17.5 μm, 4 μm/20 μm, and 4 μm/6.75 μm in the subpixels for red, green, and blue colors, respectively. Different sizings of T_2 for red, green, and blue are aimed to consider different emission efficiencies for RGB colors. Fig. 8(a) shows a microphotograph of the fabricated pixel layout for red color, where five TFTs and one capacitor are present. In addition, in the figure are the electrodes for scan line signals $V_{\rm scan}(n)$ and $V_{\rm scan}(n-1)$. Note that $V_{\rm scan}(n-1)$ is for the operation of reverse bias. Fig. 8(b) shows the overall practical experimental

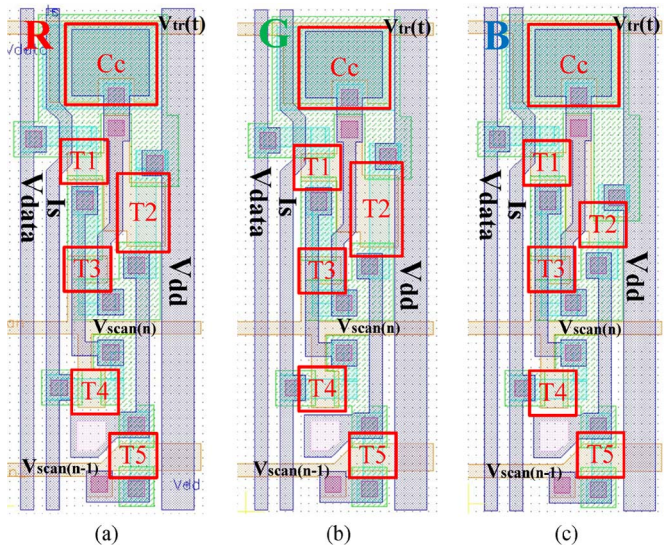

Fig. 7. Designed layouts of the subpixels for (a) red, (b) green, and (c) blue.

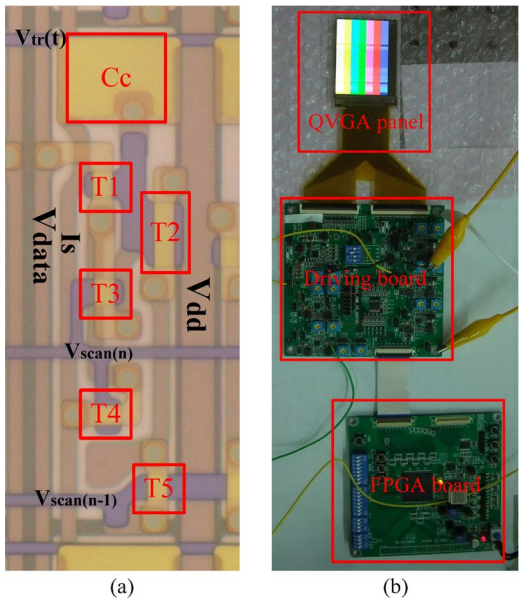

Fig. 8. (a) Microphotograph of the fabricated new pixel circuit in a QVGA panel for red color. (b) Experimental setup.

setup, where there are the QVGA OLED panel, a driving board, and a field-programmable gate array (FPGA) board. The FPGA board processes image data and signals for scanning. The driving board provides the power. This QVGA OLED panel is set up for displaying bars in different colors for testing. Table III summaries the specifications and properties of the QVGA panels.

B. Measurements of Emission Nonuniformity

The emission nonuniformity of the 2.4-in QVGA panel is experimentally investigated to validate the effectiveness of the proposed pixel circuit in $V_{\rm th}$ compensation. The standard of Video Electronics Standards Association (VESA) Flat Panel Display Measurement (FPDM) [18] is used herein for investigation. Fig. 9 shows the measurement results at five points specified by VESA FPDM. Point A is located at the center

TABLE III
SPECIFICATIONS OF THE NEW PIXEL CIRCUIT

Feature	Spec.
Diagonal	2.4-in. diagonal
Resolution	240 × RGB × 320
Pixel pitch	51um×153um×3 (166ppi)
Gray scale	8-bit 256 gray scale
Driving method	Current compensation
Non-uniformity	2.6%
Input V_{data} range	0~5V(Voltage input)

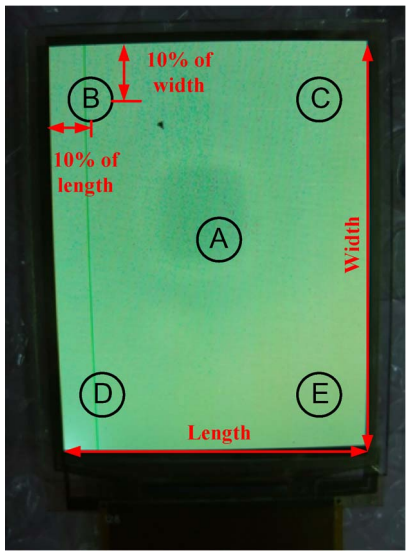

Fig. 9. Measurements for panel emission nonuniformity by VESA FPDM.

TABLE IV
MEASUREMENT RESULTS ON PANEL EMISSION NONUNIFORMITY

Point Position	Luminance(cd/m^2)
A	214.3
B	212.2
C	217.7
D	212.0
E	217.9

of panel. Points B–E are located at 10% of panel length and width from margin of the panel. The displayed nonuniformity can then be calculated by

$$\text{Nonuniformity} = [1 - (L_{\min}/L_{\max})] \times 100\% \qquad (12)$$

where $L_{\min}$ and $L_{\max}$ are minimum and maximum luminances, respectively. The highest gray level is set for determining nonuniformity. Table IV gives the measurement results, which show that point E has the maximum luminance, i.e., 217.9 cd/m^2, whereas point B does the minimum luminance, i.e., 212.2 cd/m^2. In the results, the emission nonuniformity

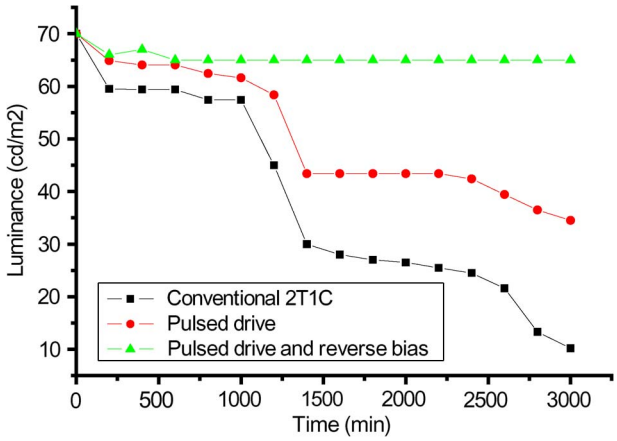

Fig. 10. Measurements of OLED-emitted luminance for three different operations.

of the new 2.4-in panel is as small as 2.6%, which is close to 2.19% of the simulated previously by Monte Carlo method. 2.6% or 2.19% in nonuniformity can generally be regarded as tolerable for a display.

C. Measurements of Gray Level

The emitted gray levels of this QVGA panel implemented with the newly-designed pixel circuits are measured by a colorimeter. The measurements of mixed white light are shown in Fig. 3, where those analytical counterparts calculated by current integration of the new pixel circuit abiding by (11) are also depicted for comparison. The closeness between two sets of data confirms the validity of the luminance prediction by (11). Based on (11), the pixel designer is able to easily find varied levels and range of V_{data} for implementing 256 gray levels from 0 to 5 V. In addition, present in the figure is a quadratic dependence of measured normalized gray levels on input data voltage, demonstrating well an easy implementation of gamma correction.

D. Measurements of Degradation Alleviation

Three different operation conditions for the OLED panel are next considered for investigating the performance of alleviating the AMOLED degradation by the proposed pulsed drive and reverse bias. First, the emitted luminance of a QVGA OLED panel with pixel circuits consisting of conventional two TFTs and one capacitor (2T1C) is measured for three days. Next, the newly designed 5T1C panel by the designed pulsed drive is measured with and without reverse biasing, also for three days. The initial luminances for three different conditions are all set to 70 cd/m^2 by a specific input data voltage, as shown in Fig. 10. The three sets of experimental data in this figure show measured luminances with respect to time for three days. It is obviously seen that the 2T1C pixel circuit leads to the lowest emitted OLED luminance—the worst case regarding OLED degradation. The new 5T1C pixel circuit with pulsed drive but no reverse bias offers a higher (better) luminance, validating the advantage offered by the pulsed drive. Finally, the emitted luminance with both pulsed drive and reverse bias implemented is almost unchanged of three days, resulting in the best (largest)

emitted luminance than the previous two drives. It validates the superiority of the proposed 5T1C pixel circuit in alleviating AMOLED degradation.

V. Summary

A new AMOLED pixel circuit implemented with drive techniques of pulsed drive and reverse bias has been proposed herein to alleviate OLED emission degradation. The designed circuit also reduces the emission nonuniformity of the AMOLED panel. Simulations are conducted by HSPICE, which demonstrates successfully tolerable panel emission nonuniformity using Monte Carlo methods. The design offers the capability of displaying 256 gray levels in the range of 0–5 V for input data voltage. For the experimental study, a 2.4-in AMOLED panel in QVGA resolution with the new pixel circuit implemented is fabricated for testing. The nonuniformity of this panel is measured at five points of the panel, which is only 2.6%. In addition, the gray levels recorded by experiments for this panel are confirmed in good agreement with the theoretical counterparts predicted by the proposed current integration. To test the circuit performance of OLED degradation alleviation, additional measurements on the emitted luminance are also recorded from other panels with basic 2T1C circuits and the proposed designed 5T1C circuits for an extensive period of time. The results show that the pulsed drive does moderately ease OLED gradation, whereas the reverse bias further renders superior degradation alleviation for OLEDs.

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Kuei-Yu Lee received the B.S. degree in electrical engineering in 2007 from the National Taiwan Ocean University, Keelung, Taiwan, and the M.S. degree in electrical control engineering in 2009 from the National Chiao Tung University, Hsinchu, Taiwan, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests focus on thin-film transistors and active-matrix organic light-emitting diode (OLED) display.

Paul C.-P. Chao (M'07) received the B.S. degree from the National Cheng-Kung University, Tainan, Taiwan, in 1989 and the M.S. and Ph.D. degrees from Michigan State University, East Lansing in 1993 and 1997, respectively.

He worked for the CAE Department, Chrysler Corp., Auburn Hill, Detroit, MI, for two years. He is currently a faculty member with the Electrical Engineering Department, National Chiao Tung University (NCTU), Hsinchu, Taiwan. In recent years, his research interests focus on interface analog circuit design for optical devices/systems; micromechatronics, control technology, microsensors, and actuators.

Dr. Chao was the recipient of the 1999 Arch T. Colwell Merit Best Paper Award from the Society of Automotive Engineering, Detroit, the 2002/2003/2004 CYCU Innovative Research Award; the 2004 Long-Wen Tsai Best Paper Award from the National Society of Machine Theory and Mechanism, Taiwan; the 2005 Best Paper Award from the National Society of Engineers, Taiwan; the 2006 AUO Award; the 2007 Acer Long-Term 2nd-prize Award; the 2007/2008/2009 NCTU EEC Outstanding Research Award; the 2009 Best Paper Award from the Symposium on Nano-Device Technology; and the 2010 Best Paper Award from the 20th Annual IEEE/ASME Conference on Information Storage and Processing Systems (ISPS). He was the Associate Provost of NCTU, the Secretary of IEEE Taipei Section, 2009-2010, and currently the founding chair of the local chapter for the IEEE Sensor Council and an AdCom member of the IEEE Sensors Council. He is also the Associate Editor of three well-known SCI-index journals, IEEE Sensors Journal, *ASME Journal of Vibration and Acoustics*, and *Journal of Circuit, System and Computer*.