Evidence for a Very Small Tunneling Effective Mass ($0.03m_0$) in MOSFET High-k (HfSiON) Gate Dielectrics

Ming-Jer Chen, *Senior Member, IEEE*, and Chih-Yu Hsu, *Student Member, IEEE*

***Abstract*—We have recently conducted experimental and modeling tasks on TaC/HfSiON/SiON n-type MOSFETs, leading to an effective mass of $0.03m_0$ for 2-D electrons tunneling in high-k HfSiON dielectrics. In this letter, we present extra evidence obtained from complementary MOSFETs undergoing the same TaC/HfSiON/SiON processing, which shows that such a very small tunneling effective mass is existent not only for 3-D electrons but also for 2-D holes. This new finding is very important because it can substantially enhance the current understanding of gate tunneling leakage suppression in metal-gate high-k MOSFETs.**

***Index Terms*—Effective mass, effective oxide thickness (EOT), HfO_2, HfSiON, high-k, metal gate, MOSFETs, tunneling.**

I. INTRODUCTION

HIGH-k GATE dielectrics are currently largely employed in advanced MOSFET manufacturing. Thus, understanding the fundamental properties of high-k dielectrics is crucial. Relative to conventional SiO_2 and SiON counterparts, high-k dielectrics feature two fundamentally distinct properties: a narrower energy bandgap and a lower optical phonon energy [1]. Concerning electrons or holes tunneling in high-k dielectrics, their tunneling effective masses should, in principle, differ fundamentally from those of gate oxide. More recently, we have conducted experimental and modeling tasks on TaC/HfSiON/SiON n-MOSFETs and found that 2-D electrons in a HfSiON dielectric have a tunneling effective mass of around $0.03m_0$ [2]. This value is quite unusual because it is far below that of gate oxide and is the smallest of high-k dielectrics to date. On the other hand, a countertrend with increasing effective oxide thickness (EOT) was experimentally observed [3]–[5]: HfO_2 gate tunneling leakage with respect to the SiO_2 one does not decrease as intuitively expected. To elucidate this, an intermixing action between a high-k dielectric and an interfacial layer was proposed [3], [4]; however, tunneling effective masses as responsible origins were not mentioned there.

The aim of this letter is to provide extra evidence to confirm the existence of a very small tunneling effective mass and make it one of the fundamental properties of the high-k HfSiON dielectric. In a sense, the current understanding of the observed gate tunneling leakage suppression [3]–[5] is able to be significantly enhanced.

II. EXPERIMENT

TaC/HfSiON/SiON n- and p-MOSFETs were fabricated in a manufacturing process detailed elsewhere [6]. A TEM picture of the underlying TaC/HfSiON/SiON/Si system is shown in Fig. 1. The corresponding energy band diagram is together plotted for a p-MOSFET in flatband condition. All relevant material and process parameters are labeled in Fig. 1, along with the corresponding values. By performing a quantum mechanical numerical fitting of gate capacitance C_g–V_g measured from the p-MOS device in inversion, we obtained TaC work function = 4.48 eV, EOT = 1.5 nm, and n-type substrate doping concentration $= 1 \times 10^{17}$ cm^{-3}. Evidently, the p-MOS gate stack is slightly larger than the n-MOS one (1.4 nm) [2]. We attributed this to the different nitrogen concentrations encountered. To meet the same EOT (1.5 nm), $\varepsilon_{\mathrm{IL}}$ in the interface layer (IL) was changed to $6.2\varepsilon_0$. The corresponding φ_{ILC} and φ_{ILV} were 2.54 and 3.06 eV, respectively [7].

The carrier separation method in inversion condition was employed. The measured terminal currents are shown in Figs. 2 and 3 for n- and p-MOSFETs, respectively. Fig. 2 reveals the following: 1) The source/drain current $I_{S/D}$ dominates the gate current I_g due to 2-D electron tunneling, and 2) owing to 3-D valence-band electron tunneling to the gate, separated holes flow down the substrate and constitute the substrate current I_b. In the inset of the figure, the carrier separation measurement setup is shown. In Fig. 3, one can see that I_g comprises two distinct components: 1) $I_{S/D}$ due to hole tunneling from the inversion layer and 2) I_b due to 3-D electron tunneling from the metal side. In Fig. 3, we inserted experimental C_g–V_g for p-MOSFET in inversion, along with the aforementioned curve fitting. The corresponding energy band diagrams and tunneling paths are shown in Fig. 4.

III. CALCULATION AND FITTING

A quantum gate tunneling simulator [2], [8] was used. Given the known material and process parameters ($m_k^* = 0.03m_0$,

---

Manuscript received October 26, 2011; accepted December 28, 2011. Date of publication January 31, 2012; date of current version March 23, 2012. This work was supported by the National Science Council of Taiwan under Contract NSC 98-2221-E-009-164-MY3. The review of this letter was arranged by Editor J. Cai.

The authors are with the Department of Electronics Engineering and the Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: chenmj@faculty.nctu.edu.tw; cyhsu.ee94g@g2.nctu.edu.tw).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2011.2182599

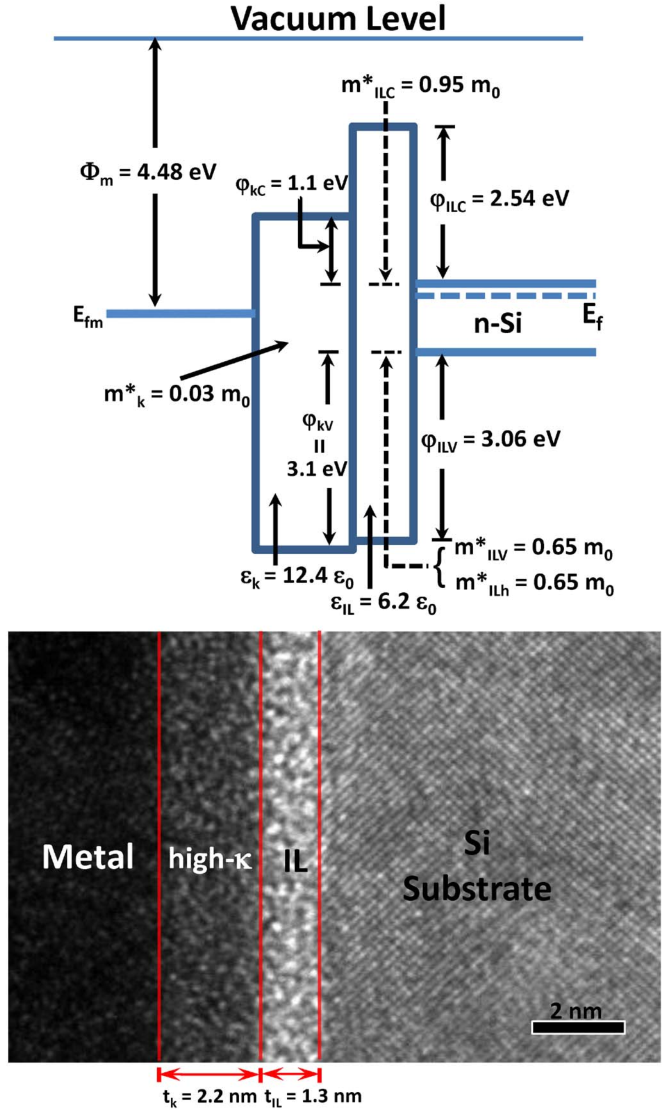

Fig. 1. Schematic of the energy band diagram in a metal-gate/high-k/IL/Si system for a p-MOSFET in flatband condition, along with a high-resolution TEM picture. The relevant material and process parameters are as follows: 1) the TaC metal work function Φ_m; 2) for the HfSiON high-k part, its physical thickness t_k, permittivity ε_k, tunneling effective mass m^*_k, conduction-band offset φ_{kC}, and valence-band offset φ_{kV}; and 3) for the SiON IL part, its physical thickness t_{IL}, permittivity $\varepsilon_{\mathrm{IL}}$, conduction-band electron tunneling effective mass m^*_{ILC}, valence-band electron tunneling effective mass m^*_{ILV}, hole tunneling effective mass m^*_{ILh}, conduction-band offset φ_{ILC}, and valence-band offset φ_{ILV}.

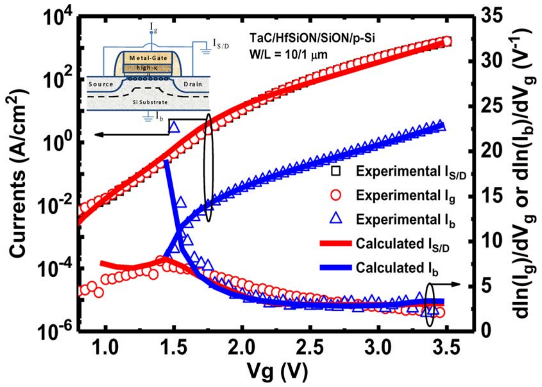

Fig. 2. (Symbols) Experimental I_g, $I_{S/D}$, and I_b, as well as the corresponding $d\ln(I_g)/dV_g$ and $d\ln(I_b)/dV_g$, plotted versus V_g for n-MOSFET in inversion. The (lines) calculated results are given. For $I_{S/D}$ calculation, $\varphi_{\mathrm{kC}} = 1.1$ eV, $\varphi_{\mathrm{ILC}} = 2.36$ eV, $m^*_k = 0.03m_0$, $m^*_{\mathrm{ILC}} = 0.95m_0$, and $\varepsilon_{\mathrm{IL}} = 7\varepsilon_0$. For I_b calculation, $m^*_k = 0.03m_0$, and $m^*_{\mathrm{ILV}} = 0.65m_0$. The inset schematically shows the current separation measurement.

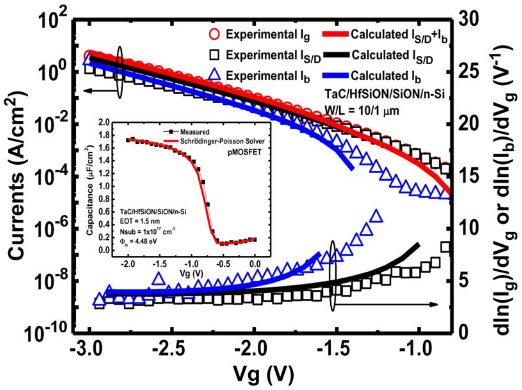

Fig. 3. (Symbols) Experimental I_g, $I_{S/D}$, and I_b, as well as the corresponding $d\ln(I_{S/D})/dV_g$ and $d\ln(I_b)/dV_g$, plotted versus V_g for p-MOSFET in inversion. The (lines) calculated results are given. For I_b calculation, $\varphi_{\mathrm{kC}} = 1.1$ eV, $\varphi_{\mathrm{ILC}} = 2.54$ eV, $m^*_k = 0.03m_0$, and $m^*_{\mathrm{ILC}} = 0.95m_0$. For $I_{S/D}$ calculation, $\varphi_{\mathrm{kV}} = 3.1$ eV, $\varphi_{\mathrm{ILV}} = 3.06$ eV, $m^*_k = 0.03m_0$, and $m^*_{\mathrm{ILh}} = 0.65m_0$. The inset shows a comparison of the (symbol) experimental and (line) simulated C_g versus V_g for TaC/HfSiON/SiON-gate-stack p-MOSFET in inversion.

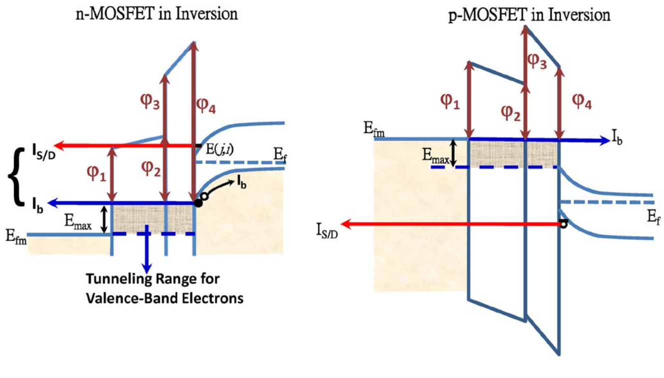

Fig. 4. Schematics of the energy band diagrams and tunneling paths for n- and p-MOSFETs.

$\varphi_{\mathrm{kC}} = 1.1$ eV, $\varepsilon_k = 12.4\varepsilon_0$, $m^*_{\mathrm{ILC}} = 0.95m_0$, $\varepsilon_{\mathrm{IL}} = 7\varepsilon_0$, and $\varphi_{\mathrm{ILC}} = 2.36$ eV) [2], the calculated $I_{S/D}$ of the n-MOSFET and, hence, its $d\ln(I_g)/dV_g$ are shown in Fig. 2. The opposite tunneling case, namely the I_b of the p-MOSFET in inversion, should encounter the same tunneling parameters. To testify to this, we quoted an existing formula [9], and thereby, the underlying I_b can be written as

$$I_b = \frac{4\pi q m^*_M}{h_3} \int_{0}^{E_{\max}} E T_{\mathrm{WKB}}(E)\, dE \tag{1}$$

where m^*_M $(= 1.0m_0)$ is the metal electron mass; E is the allowed electron energy, as shown in Fig. 4 for the p-MOSFET, for tunneling between metal Fermi level and conduction-band energy at the Si/IL interface; and $E_{\max}$ is the corresponding energy difference. The WKB transmission probability T_{WKB} in (1) can make use of existing analytic expressions (i.e., [2, eq. (2)]) as long as the tunneling criteria (i.e., φ_1, φ_2, φ_3, and

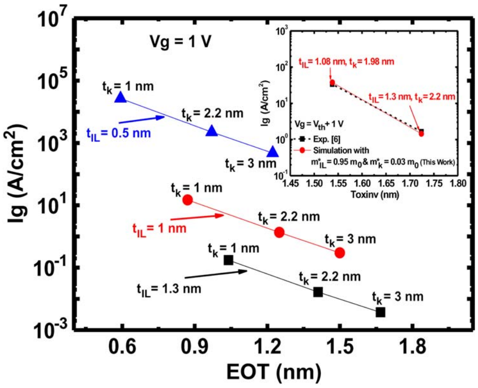

Fig. 5. Simulated I_g due to electron tunneling from the inversion layer versus EOT with t_{IL} as a parameter. The corresponding t_k values are labeled. The material parameters used in the simulation are the same as those in Fig. 2. The inset shows a comparison of the simulated I_g with experimental values [6] in the same TaC/HfSiON/SiON process, plotted versus electrical gate oxide thickness in inversion. V_{th} is the threshold voltage.

φ_4 therein) are modified according to the energy band diagram in Fig. 4. Strikingly, the resulting I_b appears to match the experimental data well, as shown in Fig. 3. This was achieved without changing any parameters.

Next, the values of $m_k^* = 0.03m_0$ and $m_{\mathrm{ILV}}^* = 0.65m_0$ were drawn from a fitting of the experimental I_b of the n-MOSFET in inversion. This was done by using (1) but with the following changes: m_M^* was replaced by a valence-band electron effective mass of $0.65m_0$ [9], $E_{\max}$ was redefined as the difference between metal Fermi level and silicon valence-band edge, and the corresponding criteria (φ_1, φ_2, φ_3, and φ_4) for T_{WKB} were altered, in accordance with the energy band diagram in Fig. 4. The fitting quality is fairly good, as shown in Fig. 2.

Physically speaking, m_{ILh}^* in IL should be equal or close to m_{ILV}^*. In this work, we made $m_{\mathrm{ILh}}^* = 0.65m_0$. To calculate the hole tunneling component $I_{S/D}$ of the p-MOSFET, a hole tunneling simulator [8] was utilized. T_{WKB} can be easily modified accordingly. Then, a comparison of the calculated $I_{S/D}$ with the experimental one led to $\varphi_{\mathrm{kV}} = 3.1$ eV. As shown in Fig. 3, good fitting holds again.

IV. DISCUSSION

To see the individual effects of varying t_k and t_{IL}, we show in Fig. 5 the simulated I_g due to electron tunneling from the inversion layer, plotted versus EOT for three t_{IL} values. The simulation points are also labeled with corresponding t_k. In addition, the simulated I_g was found to match existing data in the same manufacturing process [6], as shown in the inset of the figure for two different combinations of t_k and t_{IL}.

From Fig. 5, we can see the following: 1) the gate leakage increases with decreasing EOT, in agreement with [3]–[5], and 2) an increase in t_{IL} can suppress I_g more significantly than t_k. We also show in Fig. 5 that reducing t_{IL} will seriously increase I_g until it is intolerably high. This seems to be inconsistent with recent experiments [5]: I_g through HfO$_2$ is tolerable even for the case of t_{IL} approaching zero. However, one of the fundamental differences should be kept in mind: HfO$_2$ permittivity is higher than that of HfSiON, and as a consequence of maintaining the same EOT, the HfO$_2$ dielectric is much thicker. Indeed, this is the fact since a fair comparison of experimental I_g between HfSiON and HfO$_2$ has been published in the literature [6].

As corroborated earlier, a fundamental very small tunneling effective mass is existent. In this sense, a tunneling effective mass point of view is able to enhance current understanding of the observed I_g suppression [3], [4]. First, the HfO$_2$ dielectric is featured by a very small m_k^* while the interfacial layer can have a much higher m_{IL}^*. Next, as stated in [3] and [4], extra annealing treatments increase t_{IL} while simultaneously making more hafnium atoms appear in the regrown interfacial layer. Thus, the corresponding m_{IL}^* is likely to be lowered according to this work. Consequently, the gate leakage suppression ability relative to the SiO$_2$ gate oxide is degraded, as experimentally observed [3], [4].

V. CONCLUSION

Characterization and modeling of gate tunneling components of TaC/HfSiON/SiON complementary MOSFETs in inversion have been carried out. A fundamental tunneling effective mass featuring a very small value has been corroborated in the HfSiON dielectric. Current understanding of gate leakage suppression has been substantially enhanced.

REFERENCES

[1] M. V. Fischetti, T. P. O'Regan, S. Narayanan, C. Sachs, S. Jin, J. Kim, and Y. Zhang, "Theoretical study of some physical aspects of electronic transport in nMOSFETs at the 10-nm gate-length," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2116–2136, Sep. 2007.

[2] C. Y. Hsu, H. G. Chang, and M. J. Chen, "A method of extracting metal-gate high-k material parameters featuring electron gate tunneling current transition," *IEEE Trans. Electron Devices*, vol. 58, no. 4, pp. 953–959, Apr. 2011.

[3] A. Callegari, P. Jamison, E. Cartier, S. Zafar, E. Gusev, V. Narayanan, C. D'Emic, D. Lacey, F. M. Feely, R. Jammy, M. Gribelyuk, J. Shepard, W. Andreoni, A. Curioni, and C. Pignedoli, "Interface engineering for enhanced electron mobilities in W/HfO$_2$ gate stacks," in *IEDM Tech. Dig.*, Dec. 2004, pp. 825–828.

[4] A. Callegari, P. Jamison, D. Neumayer, F. M. Feely, J. Shepard, W. Andreoni, A. Curioni, and C. Pignedoli, "Electron mobility dependence on annealing temperature of W/HfO$_2$ gate stacks: The role of the interfacial layer," *J. Appl. Phys.*, vol. 99, no. 2, pp. 023709-1–023709-5, Jan. 2006.

[5] T. Ando, M. M. Frank, K. Choi, C. Choi, J. Bruley, M. Hopstaken, M. Copel, E. Cartier, A. Kerber, A. Callegari, D. Lacey, S. Brown, Q. Yang, and V. Narayanan, "Understanding mobility mechanisms in extremely scaled HfO$_2$ (EOT 0.42 nm) using remote interfacial layer scavenging technique and Vt-tuning dipoles with gate-first process," in *IEDM Tech. Dig.*, Dec. 2009, pp. 423–426.

[6] Y. T. Hou, F. Y. Yen, P. F. Hsu, V. S. Chang, P. S. Lim, C. L. Hung, L. G. Yao, J. C. Jiang, H. J. Lin, Y. Jin, S. M. Jang, H. J. Tao, S. C. Chen, and M. S. Liang, "High performance tantalum carbide metal gate stack for nMOSFET application," in *IEDM Tech. Dig.*, Dec. 2005, pp. 31–34.

[7] X. Guo and T. P. Ma, "Tunneling leakage current in oxynitride: Dependence on oxygen/nitrogen content," *IEEE Electron Device Lett.*, vol. 19, no. 6, pp. 207–209, Jun. 1998.

[8] C. Y. Hsu, C. C. Lee, Y. T. Lin, C. Y. Hsieh, and M. J. Chen, "Enhanced hole gate direct tunneling current in process-induced uniaxial compressive stress p-MOSFETs," *IEEE Trans. Electron Devices*, vol. 56, no. 8, pp. 1667–1673, Aug. 2009.

[9] J. W. Yang, J. G. Fossum, G. O. Workman, and C. L. Huang, "A physical model for gate-to-body tunneling current and its effects on floating-body PD/SOI CMOS devices and circuits," *Solid-State Electron.*, vol. 48, no. 2, pp. 259–270, Feb. 2004.