LDMOS Transistor High-Frequency Performance Enhancements by Strain

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***Abstract*—The effects of mechanical stress on the dc and high-frequency performances of laterally diffused MOS (LDMOS) transistors with different layout structures were investigated by using the wafer bending method. A 3.1% peak cutoff frequency (f_T) enhancement is achieved for the multifinger device under 0.051% biaxial tensile strain. For LDMOS with annular layout, the f_T enhancement is increased to 3.7% due to the various channel directions. Our results suggest the strain technology can be adopted in LDMOS for RF applications. The transconductance and gate capacitance were also extracted to clearly demonstrate the f_T variations.**

***Index Terms*—Annular layout, biaxial tensile strain, cutoff frequency, laterally diffused MOS (LDMOS), mechanical stress.**

I. Introduction

THE RAPID growth of wireless communication product markets has created a huge demand for low-cost, high-efficiency, and good-linearity radio-frequency (RF) power amplifiers. Among power devices, laterally diffused MOS (LDMOS) transistors are the most attractive in cost and potential improvements in performance and integration. LDMOS transistors have been widely used in RF power amplifier modules for a high-frequency range up to 3.8 GHz [1]–[3]. Recently, CMOS device improvements with mechanical strain have produced large IC performance gains [4]–[7]. The strain on the Si channel can be induced by using process technology (e.g., silicon nitride cap, SiGe source/drain, and SiGe buffer layer) and/or by bending the Si wafer directly.

In the case of LDMOS transistors, the strained Si channel upon a relaxed SiGe buffer layer was presented by Kondo [8]. Better RF power performances were demonstrated as compared to the conventional LDMOS. However, a comprehensive analysis of device performance enhancements under strain was not accomplished. Owing to the existence of a drift region in LDMOS, the strain effects on the LDMOS performance might be different from those on the CMOS device performance. Therefore, it is interesting to investigate the electrical characteristics of LDMOS under strain. In this letter, we study the effects of mechanical stress on the dc and high-frequency characteristics of LDMOS by using wafer bending method. The external mechanical stress can provide biaxial tensile strain on the devices without changing the process flow parameters. It is helpful for studying the strain effect alone. The strain-induced performance enhancements in different layout structures were also compared. The strain-induced high-frequency performance enhancements were observed and were understood by analyzing the changes in transconductance and gate capacitance.

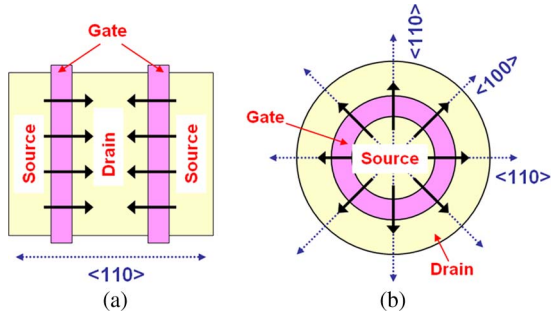

Fig. 1. Layout structures of LDMOS cell. (a) Multifinger. (b) Annular ring. The black arrow indicates the electron current direction.

II. Experiments

The n-channel LDMOS transistors were fabricated by a 0.5 μm CMOS-DMOS process with a gate oxide thickness of 135 Å. The substrate is (100) silicon wafer. The effective channel length and drift length are 1.1 and 2.4 μm, respectively. Detailed description of the device structure can be found in [9]. Two device layouts are studied in this work (see Fig. 1). Since the drift region of the annular structure is located on the outside, it is less susceptible to quasi-saturation at high current [10]. More significantly, it has higher cutoff frequency, which cannot be improved by increasing the width of the multifinger structure.

A wafer bending apparatus is used to apply external biaxial tensile stress [4], [5]. The strain on the silicon substrate was estimated by the ANSYS simulation. The dc and high-

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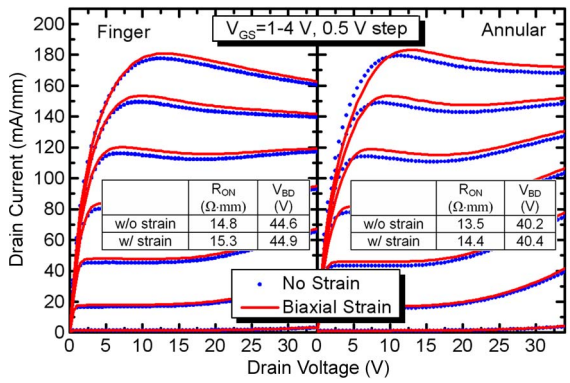

Fig. 2. Output characteristics of the multifinger (left) and annular (right) LDMOS transistors with and without 0.051% mechanical strain. The on-resistances shown in this figure were extracted at $V_{\rm GS} = 4$ V.

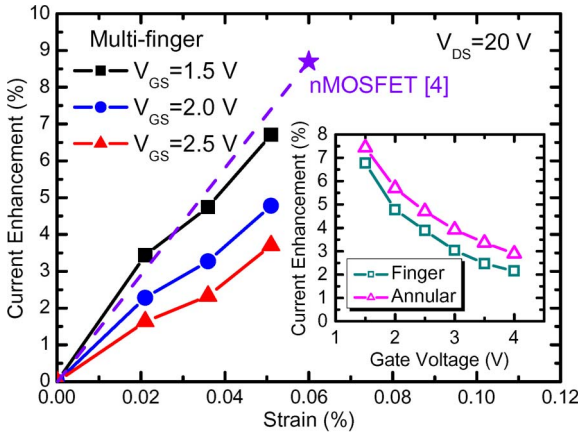

Fig. 3. I_D enhancements of a multifinger device with different biaxial strains. At $V_{\rm GS} = 1.5$ V, the current enhancements are similar as the nMOSFET in low-voltage CMOS technology [4]. The inset shows the I_D enhancement under 0.051% strain as a function of gate voltage.

frequency characteristics of the test devices were measured on chip using an Agilent 4142B modular source/monitor and an Agilent 8510C network analyzer from 100 MHz to 20 GHz.

III. Results and Discussion

The dc characteristics of LDMOS under strain are shown in Fig. 2. The drain currents (I_D) in both multifinger and annular LDMOS devices are enhanced by applying the biaxial stress, owing to the strain-induced mobility enhancement [11]. Since the change in silicon energy bandgap is small under the low strain (0.051%), the breakdown voltages are nearly unchanged ($< 1\%$). By plotting the current enhancements with different strains, we found that the current enhancements are nearly proportional to the strain (see Fig. 3). At low gate voltages $(V_{\rm GS})$, the I_D improvements are similar as today production low-voltage CMOS transistor for the same biaxial strain [4] suggesting that improvement as large as 30% maybe obtainable, as in CMOS transistor if large biaxial strain is applied with stressor as in strained CMOS technology. However, unlike strained CMOS transistors, LDMOS current enhancement is significantly lower at high $V_{\rm GS}$ than at low $V_{\rm GS}$. With 0.051% biaxial strain, the enhancement of I_D decreases from 6.7% to 3.7% when $V_{\rm GS}$ increases from 1.5 V to 2.5 V for multifinger device.

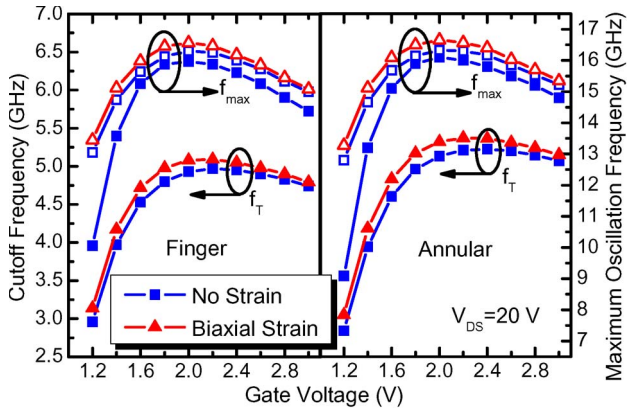

Fig. 4. Cutoff frequency and maximum oscillation frequency of the LDMOS transistors with and without 0.051% mechanical strain. Solid symbols are the measured data, and open symbols are the calculated data.

For LDMOS transistors, the drain current is dominated by the channel current at low $V_{\rm GS}$, while it is dominated by the drift region resistance at high $V_{\rm GS}$. Therefore, the smaller enhancement at higher $V_{\rm GS}$ indicates that the drift resistance cannot be changed as much as the channel current by the tensile stress. When the electrons emit from channel to drift region, the applied stress is not parallel to the current direction. In addition, the electron velocity in the drift region is closer to saturation than in the channel. These differences may degrade the enhancement and even increase the resistivity in the drift region. The increase of the drift resistivity can be confirmed by the increase of on-resistance $(R_{\rm ON})$, as shown in Fig. 2.

The inset of Fig. 3 compares the strain-induced current enhancements between multifinger and annular devices. The annular device has better improvement than the multifinger one at all gate biases. For multifinger device, the current flows in the $\langle 110 \rangle$ direction, while for annular device, the current flows through all directions in the (100) plane (see Fig. 1). Since the piezoresistance coefficients increase from $\langle 110 \rangle$ to $\langle 100 \rangle$ [12], the current in annular device could have larger increase than that in multifinger counterpart. Present production techniques produce uniaxial strains, $\langle 100 \rangle$ current flow would be advantageous. Owing to a higher drain current and strain sensitivity, the annular layout would be a better choice for power-amplifier applications.

To study the high-frequency behavior under strain, the ac current gain (H_{21}) and unilateral power gain (U) were calculated from S-parameters to extract the cutoff frequency (f_T) and maximum oscillation frequency $(f_{\rm max})$, respectively. Fig. 4 shows the strain effects on the measured f_T for the two layouts. Similar to the dc performance, the strain-induced improvement of cutoff frequency is better in annular device. 3.7% peak f_T improvements are observed versus 3.1% for the multifinger device. Moreover, the strain-induced f_T enhancement closes to the I_D enhancement at the same bias condition, indicating that the applied stress can also have large influence on the RF performance. Since the f_T is related to the small-signal transconductance (g_m) and gate capacitance $(C_{\rm gg})$, we are interested to analyze their variations after applying stress.

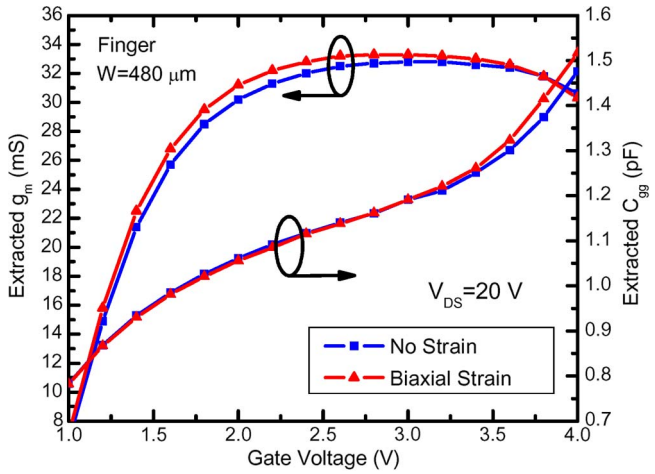

Fig. 5. Extracted g_m and $C_{\rm gg}$ of a multifinger LDMOS with and without 0.051% mechanical strain.

When ignoring the parasitics, g_m and $C_{\rm gg}$ can be extracted from Y parameters at low frequencies directly [13]. The extracted results of a multifinger LDMOS are shown in Fig. 5. Similar results are also obtained for annular devices. We observed that the g_m increases with increasing tensile strain, while $C_{\rm gg}$ is nearly unchanged at $V_{\rm GS} < 3.5$ V. Hence, the strain-induced increase in f_T is mainly attributed to the increase in g_m. At $V_{\rm GS}$ near the peak f_T, the enhancements of g_m and f_T are 3.3% and 3.1%, respectively. The strain-induced enhancement of f_T is slightly lower than that of g_m. It is probably due to the influence of drain resistance [9]. At $V_{\rm GS} > 3.5$ V, the $C_{\rm gg}$ begins increasing with strain. In pre-quasi-saturation region, the inversion charges may be injected from the intrinsic MOSFET to the depleted area of the drift, so the $C_{\rm gg}$ increases rapidly with increasing gate voltages [14]. Therefore, the strain-induced $C_{\rm gg}$ variation at high gate voltages suggests the quasi-saturation effect may become more serious under strain. Fortunately, for RF applications, the gate biases of LDMOS are below the pre-quasi-saturation region.

Because the measurement uncertainty of $f_{\rm max}$ could be higher than 3% owing to the influence of gate resistance (R_g), we compared the $f_{\rm max}$ variation under strain using the calculated data based on [15]

$$f_{max} \approx \frac{f_T}{2\sqrt{g_{ds}R_g + 2\pi f_T C_{gd}(R_g + \alpha R_d)}} \qquad (1)$$

where $g_{\rm ds}$ is the channel conductance, $C_{\rm gd}$ is the gate-to-drain capacitance, R_d is the drain resistance, and α is the ratio of drain capacitance to $C_{\rm gg}$. Since the terms $g_{\rm ds}R_g$ and $2\pi f_T C_{\rm gd}\alpha R_d$ in (1) are much lower than the $2\pi f_T C_{\rm gd}R_g$ in our devices, the strain-induced variations of $g_{\rm ds}$ and R_d can been ignored. In addition, R_g could not be changed by the strain. Therefore, all parameters except f_T in (1) were derived from the measured S-parameters without strain, while the measured f_T with and without strain were substituted into (1) to obtain the $f_{\rm max}$ with and without strain, respectively. The calculated $f_{\rm max}$ without strain quite approaches to the measured $f_{\rm max}$ (see Fig. 4). The strain-induced enhancements of peak $f_{\rm max}$ for multifinger and annular devices are 1.6% and 2.0%, respectively.

IV. Conclusion

The enhancements of high-frequency performances of LDMOS transistors by mechanical tensile stress have been observed in this study. By analyzing the g_m and $C_{\rm gg}$ variations with strain, we know the strain-induced f_T enhancement is mainly related to the g_m enhancement. In addition, owing to the different channel directions, the annular devices have more improvement than the multifinger ones. Our results suggest that applying a tensile stress to LDMOS is an effective and attractive method to improve its performance for RF applications.

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