High-Reliability Trigate Poly-Si Channel Flash Memory Cell With Si-Nanocrystal Embedded Charge-Trapping Layer

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***Abstract*—This letter introduces a polycrystalline-silicon nanowire (NW) thin-film nonvolatile memory (NVM) with a self-assembled silicon-nanocrystal (Si-NC) embedded charge-trapping (CT) layer. This process is simple and compatible with conventional CMOS processes. Experimental results indicate that this NW NVM exhibits high reliability due to a deep-quantum-well structure and immunity of enhanced electric field underneath a disk-shaped Si-NC. After 10 000 P/E cycles, the memory window loss of the NVM with a Si-NC embedded CT layer is less than 12% until 10^4 s at 150 °C. Accordingly, a poly-Si thin-film transistor with a Si-NC embedded CT layer is highly promising for NVM applications.**

***Index Terms*—Nanocrystal (NC), nonvolatile memory (NVM), thin-film transistor (TFT).**

I. Introduction

FLASH memory is a type of nonvolatile memory (NVM) which does not require a power supply to sustain information storage; it is also the essential component of portable electronics. Significant advances in mobile equipment have markedly increased the demand for information storage. Accordingly, Flash memory has been continuing to scale to satisfy market demand. However, it is becoming increasingly difficult to sustain Moore's law because of process and device limitations. Hence, 3-D multilayer-stack memory based on polycrystalline-Si (poly-Si) thin-film transistors (TFTs) has been proposed to solve these problems [1]–[4].

Silicon–oxide–nitride–oxide–silicon (SONOS) structure is a promising candidate of NVM, due to the localized charge storage/loss and immunity to floating-gate coupling [5]. Recently, NVM devices with silicon nanocrystals (Si-NCs) have also been investigated. Several self-assembled Si-NC fabrication structures have been studied, such as SiO_2/Si-NC/SiO_2 and Si_3N_4/Si-NC/Si_3N_4 [6]–[8]. However, the SiO_2/Si-NC/SiO_2 structure needs high crystallization temperature and would damage the tunneling oxide. Furthermore, Si-NCs on Si_3N_4 are of interest because of their higher density of states, as compared to those on SiO_2 [9]. Compared with SONOS Flash memory, these Si-NC memories could further improve retention characteristics due to high-density deep-level traps on the Si-NC surface and spatial isolation of stored charges [10]–[12]. However, a local increase of the electric field under the spherical-shaped Si-NC improves P/E speed, yet possibly degrades reliability [13]. Hence, in this letter, a disklike shape of Si-NC was preformed to sustain the reliability of NVM.

In CMOS and TFT technology, a trigate structure has gate control over the channel superior to that of a conventional single-gate MOSFET [14], [15]. The nanowire (NW) structure is suitable for nonvolatile applications. In particular, the program/erase (P/E) efficiency of poly-Si NW NVM is outstanding [16]. However, this high P/E speed degrades the gate dielectric. Therefore, in this letter, a Si_3N_4/Si-NC/Si_3N_4 charge-trapping (CT) layer was introduced into poly-Si NW NVM to enhance reliability characteristics.

II. Device Structure and Fabrication

The trigate poly-Si TFT NVM with a Si-NC embedded CT layer was fabricated by initially growing a 400-nm-thick silicon dioxide layer. A 50-nm-thick undoped amorphous-Si (a-Si) layer was deposited by low-pressure chemical-vapor deposition (LPCVD) at 550 °C and solid-phase crystallized at 600 °C for 24 h in nitrogen ambient. The patterns of the active layer were defined as ten strips of multiple 68-nm NWs. An 11-nm-thick tetraethyl orthosilicate (TEOS) SiO_2 layer was grown as the tunneling oxide. Above the tunneling oxide, first, a 3-nm-thick Si_3N_4 layer was deposited by LPCVD. Second, a 2-nm-thick a-Si film was deposited at controlled deposition condition and deposition time by LPCVD. Third, a 3-nm-thick Si_3N_4 layer was deposited by LPCVD with 1050 °C annealing for 30 min in a horizontal furnace. For comparison, a pure Si_3N_4 CT layer with 3-nm thickness was deposited by LPCVD. Then, a 19-nm-thick TEOS oxide layer was deposited as the blocking oxide. Subsequently, a 100-nm-thick poly-Si layer was deposited as the gate electrode. The self-aligned source, drain, and gate regions were implanted with 23-keV phosphorous ions at a dose of 5×10^{15} cm^{-2} and activated by rapid thermal annealing at 1050 °C in nitrogen ambient. A SiO_2 passivation layer was deposited. Finally, 300-nm-thick Al–Si–Cu metallization was performed and sintered.

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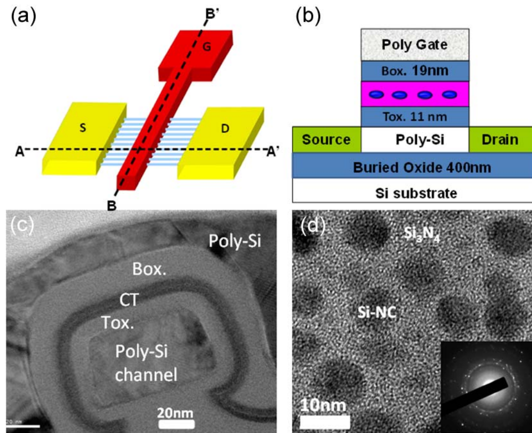

Fig. 1. (a) Top view of trigate TFT NVMs. (b) Cross-sectional view corresponding to (a) in the AA′ direction. (c) Cross-sectional TEM image of the trigate structure with NWs = 68 nm, and SiO_2 = 11 nm/Si_3N_4 = 3 nm/Si-NC = 2 nm/Si_3N_4 = 3 nm/SiO_2 = 19 nm stacked gate dielectric. (d) Top view of Si-NCs with disk shape on the control wafer. The inset of (d) shows the diffraction pattern of the Si-NC trap layer.

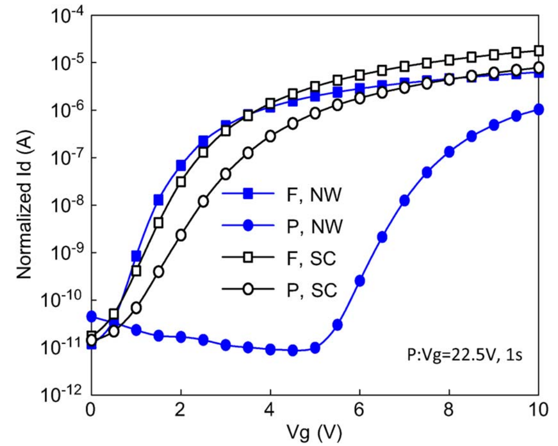

Fig. 2. I_d–V_g transfer characteristics of fresh and programmed states of NW trigate and conventional single-gate (SC) devices with Si-NC embedded CT layer. Both devices are programmed at $V_g = 22.5$ V for 1 s from the fresh state.

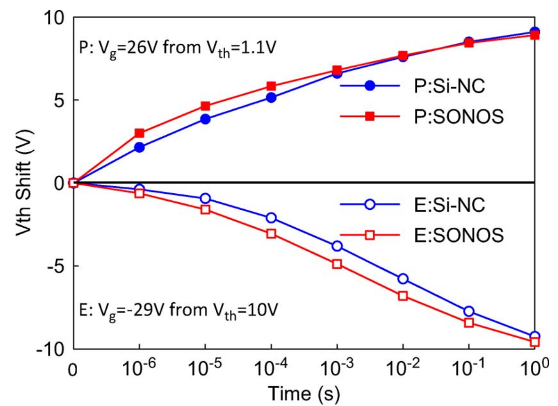

Fig. 3. P/E characteristics of Si-NC and SONOS devices under F-N bias conditions.

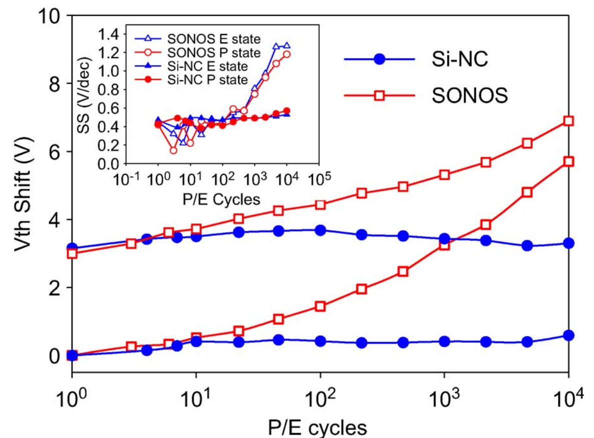

Fig. 4. Endurance characteristics of Si-NC and SONOS devices. Both devices have the same applied voltage but different physical thickness of stacked gate dielectric. Therefore, the SONOS device has the higher electric field in tunnel oxide, resulting in worse endurance than that of the Si-NC one. The inset shows SS during 10^4 P/E cycles.

III. Results and Discussion

Fig. 1(a) shows the top view of the pi-gate TFT NVM with a hybrid (Si_3N_4/Si-NCs/Si_3N_4) CT layer, and Fig. 1(b) exhibits the cross-sectional view of trigate NVMs in the AA′ direction. Ten strips of NW are made, and the space is 300 nm between each NW. Fig. 1(c) shows the cross-sectional transmission electron microscopy (TEM) photograph of one NW of trigate NVM with a hybrid (Si_3N_4/Si-NCs/Si_3N_4) CT layer, and the poly-Si active layer of the trigate device is surrounded by the stacked gate dielectric. The physical width of each NW is 68 nm, and the gate length is 10 μm. Fig. 1(d) shows the top view of Si-NCs surrounded by Si_3N_4, which is deposited and annealed on the control wafer. During the high-temperature thermal annealing, the ultrathin a-Si film (2 nm) self-assembles to form the Si-NCs with a diameter of around 7–10 nm with a disklike shape [7], [8], in which the density of Si-NCs is around 10^{12} cm^{-2}. The inset of Fig. 1(d) illustrates the diffraction pattern taken from the Si-NC trap layer. It is clearly found that the Si thin-film is amorphous as-deposited and then turns out to be polycrystalline after 1050 °C furnace annealing.

Fig. 2 plots the normalized drain current ($I_d \times L/W$) versus gate voltage for NW and single-channel (SC, gate width = 1 μm) devices in the fresh and programmed states. The devices are programmed at $V_{gs} = 22.5$ V for 1 s from the fresh state. The NW device exhibits a much higher programming speed and a better subthreshold slope than the SC device due to the corner effect and excellent gate control of the trigate structure, which is consistent with previous studies [3].

Fig. 3 plots the P/E characteristics of the trigate device with a Si-NC embedded CT layer (Si-NC device) and the trigate device with a single Si_3N_4 CT layer of 3 nm (SONOS device). For the $V_g = 26$ V program condition of Si-NC and SONOS memory devices, the electric field of the tunnel oxide is 8.23 MV/cm in the Si-NC device and 8.47 MV/cm in the SONOS memory device. Although the electric field of the Si-NC device is smaller than that of the SONOS device, the Si-NC device shows the same threshold shift with the SONOS device for the P/E characteristics due to the local increase of the electric field under the oval-shaped Si-NC [13].

Fig. 4 shows the endurance characteristics of Si-NC and SONOS devices. The subthreshold swing (SS) during 10^4 P/E cycling tests is shown in the inset of Fig. 4. Although Si-NC and SONOS devices both guarantee 10 000 P/E operations, the P/E efficiency of the SONOS device decreases with an increasing number of P/E cycles. For the SONOS device, the upward

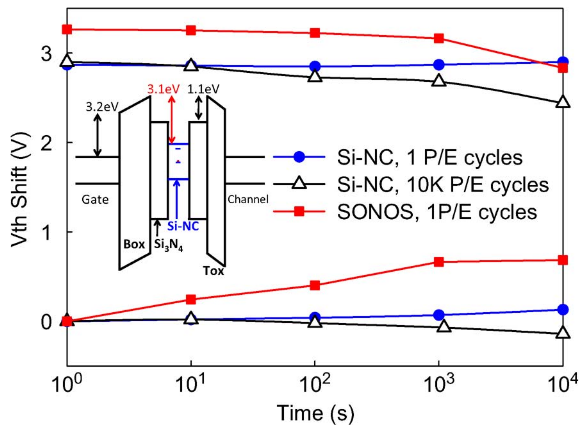

Fig. 5. Retention characteristics of Si-NC and SONOS devices at 150 °C. The inset is the band diagram of poly-Si/SiO_2/Si_3N_4/Si-NC/Si_3N_4/SiO_2/poly-Si stacked film.

threshold-voltage shift ($\Delta V_{\rm th}$) is due to the low-injected hole into the CT layer, higher electric field across the tunneling oxide, generation of Si$-$$SiO_2$ interface traps, and electron trapping in the deep states [10], [17]–[19]. The interface traps lead to SS degradation (inset of Fig. 4) and reduce the P/E speed. Hence, the Si-NC device exhibits excellent endurance of around 86% of the initial memory window after 10^4 P/E cycles.

Fig. 5 plots the data retention of Si-NC and SONOS devices at 150 °C. The memory windows of Si-NC and SONOS devices sustain 95% and 65%, respectively, for 10^4 s at 150 °C. After 10 000 P/E cycles, the memory window of the Si-NC device remains 88% for 10^4 s at 150 °C. The inset of Fig. 5 is a band structure of the Si-NC device. As the Si-NC embedded CT layer sustains a large amount of charges for data storage, the deep quantum well of Si-NC effectively suppresses direct tunneling from the CT layer into the channel [20], [21]. Moreover, the stored charges in the trap sites of the Si_3N_4 layer have tended to tunnel back into the Si-NC quantum well rather than out of the CT layer due to a markedly shorter tunneling width. These characteristics result in an excellent retention of the Si-NC device even with 10 000 P/E cycles, i.e., oxide-defect-induced charge leakage is also reduced extensively.

IV. Conclusion

A poly-Si thin-film Flash NVM with a Si-NC embedded CT layer through self-assembly processes has been presented. Experimental results indicate that memories with a Si-NC CT layer exhibits high retention and endurance characteristics. After 10 000 P/E cycles, the data retention is remarkable for NVM applications due to the deep quantum well of Si-NC encapsulated in the Si_3N_4 layer and immunity to the enhanced electric field underneath the disk-shaped Si-NCs. In addition, reducing the thickness of the tunnel oxide can further lower the P/E voltage. This investigation examines the feasibility of the poly-Si thin-film NVM with a Si-NC embedded CT layer on 3-D layer-to-layer stacked high-density NAND memory applications.

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