Abnormal Subthreshold Leakage Current at High Temperature in InGaZnO Thin-Film Transistors

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***Abstract*—Abnormal subthreshold leakage current is observed at high temperature in amorphous InGaZnO thin-film transistors. The transfer curve exhibits an apparent subthreshold current stretch-out phenomenon that becomes more serious with increasing temperatures. The negative bias temperature instability experiment has been used to prove high-temperature-induced hole generation. Furthermore, the transfer characteristics with different drain voltages have been also used to confirm the status of hole accumulation. These pieces of evidence clearly defined the stretch-out phenomenon, which is caused by thermal-induced hole generation and accumulation at the source region that leads to source-side barrier lowering.**

***Index Terms*—Indium–gallium–zinc–oxide (IGZO), temperature, thermal-induced hole, thin-film transistors (TFTs).**

I. Introduction

TRANSPARENT amorphous oxide semiconductors such as amorphous In–Ga–Zn–O (a-IGZO) are widely accepted as channel layers of thin-film transistors (TFTs) in the next-generation flat-panel displays because their TFTs have better characteristics than the traditional hydrogenated amorphous silicon (a-Si:H) TFTs. For example, a-IGZO TFTs exhibit faster field-effect mobility ($\sim 10\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{sec}$) [1], larger on/off current ratio ($> 10^8$) [2], and better stability against electrical stress [3]–[5]. Furthermore, their low process temperature and low cost are desirable for large flat-panel display applications [6]–[8]. Therefore, several applications such as active-matrix liquid-crystal displays, active-matrix organic light-emitting-diode displays, and electronic paper (e-paper) have been demonstrated using a-IGZO TFTs as driving/switching TFT arrays [9]. These mobile displays are often used in harsh environments such as on hot dashboards in cars. Therefore, it is important to explore the extent of the operating temperature for a-IGZO TFTs with good performance and reliability. In this letter, we investigate the abnormal subthreshold leakage current with temperature dependence of the a-IGZO TFT and explain the effects using energy band diagrams. Moreover, the device was given negative bias stress tests at different temperatures and under different drain biases to confirm the proposed mechanism.

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II. Experimental Setup

Bottom-gate coplanar a-IGZO TFTs were produced on a glass substrate in this letter. Plasma-enhanced chemical vapor deposition (PECVD)-derived SiO_X (300 nm) film as the gate insulator was grown at 370 °C over the patterned Ti/Al/Ti tri-layer gate electrodes. The Ti/Al/Ti source/drain electrodes were formed by sputtering and then patterned into the dimensions of channel width W from 5 to 30 μm with channel length L of 10 μm. A 30-nm-thick a-IGZO film was deposited by a dc magnetron sputtering system at room temperature using a target of In:Ga:Zn = 1:1:1 in atomic ratio, a plasma discharge power value of 300 W, and under a pressure of 5-mtorr ambiance of O_2/Ar gas mixture at the ratio of 6.7%. After defining the active region, the devices were capped with a 200-nm SiO_X layer by PECVD at 170 °C and sequentially annealed in an oven at 330 °C for 2 h. The electrical properties of a-IGZO TFTs were analyzed by using Agilent B1500A semiconductor device analyzer under no ambient light.

III. Results and Discussion

The transfer characteristics of a-IGZO TFTs at different temperatures are shown in Fig. 1. As shown in this figure, the I–V curves shift to the left and drain current I_D raises with increasing temperatures. Threshold voltage V_T is determined when normalized drain current ($\mathrm{NI}_D = I_D \times L/W$) reaches 10^{-10} A, and delta threshold voltage is determined such that the V_T at the higher temperature minus that at 300 K. Below 400 K, V_T proportionally decreases with increasing temperatures, as shown the inset in Fig. 1. It is well known for oxide semiconductors that the free electrons in the materials are mainly due to the generation of oxygen vacancies [10], [11]. Thermally excited oxygen atoms that leave their original sites move into the interstitial sites and cause vacancies with the remaining free electrons at the corresponding sites. The lower V_T observed at the higher temperature can be attributed to these free electrons generated along with the oxygen vacancies [12], [13]. Therefore, the threshold voltage shifts toward the negative direction

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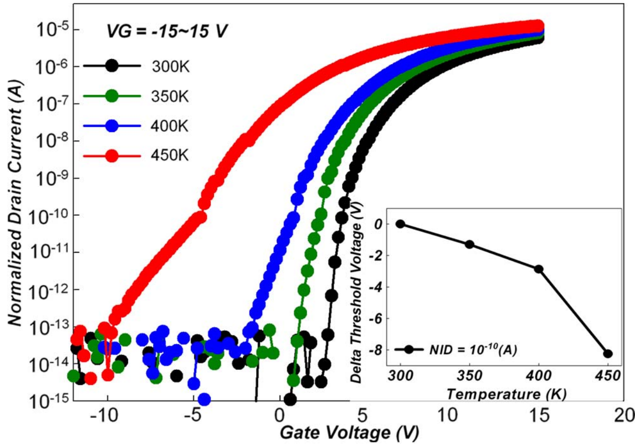

Fig. 1. I_D–V_G curves of a-IGZO TFTs at different temperatures. (Inset) Corresponding threshold voltage shift with different temperatures.

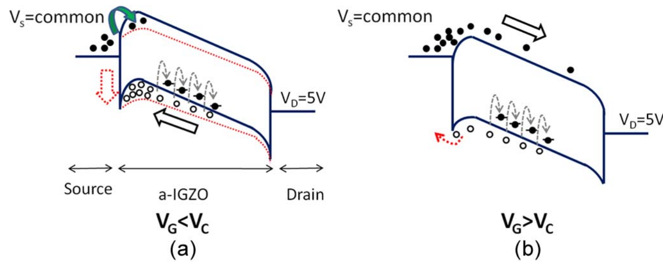

Fig. 2. Energy band diagram of proposed mechanisms for these two distinct regions. (a) Gate voltage is below V_C. (b) Gate voltage is above V_C.

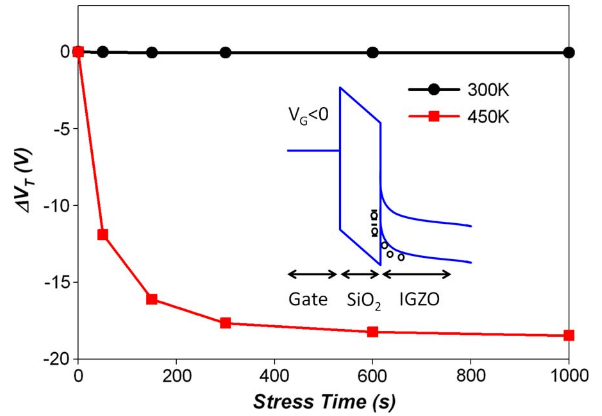

Fig. 3. Threshold voltage shift under negative gate bias at 300 K and 450 K. (Inset) Energy band diagram under negative gate bias.

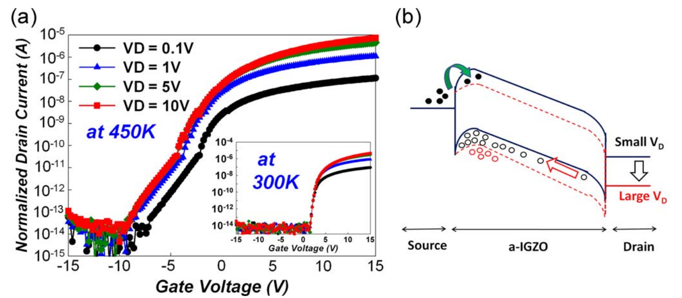

Fig. 4. (a) Normalized current–voltage characteristics at different drain voltages. (b) Energy band diagram with different drain voltages.

with increasing temperatures. Moreover, at temperature above 400 K, the transfer curves stretch out in the subthreshold region. The stretch-out phenomenon becomes more serious with increasing temperatures. It should be noted that the transfer characteristic at room temperature (300 K) restores after high temperature measurements, which means that this temperature effect is reversible.

Next, we discuss the unique behavior of the subthreshold leakage current for a-IGZO TFTs at high temperature. The transfer characteristics can be separated into stretch-out and normal regions by a critical voltage V_C. The mechanisms for these two distinct regions are proposed in Fig. 2. As shown in Fig. 2(a), when the gate voltage is below V_C, thermal-induced holes move to the source side due to the transverse electric field. Then, the holes accumulate at the source region that leads to source-side barrier lowering. Source-side barrier lowering enhances electron injection from the source and causes an apparent subthreshold leakage current. As for the normal region where $V_G > V_C$, the transfer characteristics are dominated by the barrier between the a-IGZO and the source. The barrier height becomes much lower with increasing gate voltage. The low barrier height cannot hold holes to accumulate them at the source, as shown in Fig. 2(b). Therefore, the transfer curve separates into two regions at high temperature.

High-temperature-induced hole generation and accumulation at the source have been used to prove the proposed mechanism. The negative bias temperature instability (NBTI) [14] experiment is conducted with Vg $= -30$ V at 300 K and 450 K. V_T was measured before and after NBTI. The V_T shift (ΔV_T) is plotted against stress time in Fig. 3. At 300 K, ΔV_T hardly shifts under negative gate bias stress, which is consistent with previous reports [15]–[17]. On the other hand, V_T significantly shifts in the NBTI experiment at 450 K. At high temperature, the thermal-induced hole generation and the holes are accumulated by the negative gate voltage and get trapped in the gate dielectric or at the dielectric/channel interface, as shown the inset in Fig. 3. The trapped holes then induce more electrons to shift V_T negatively with stress time.

The status of hole accumulation is further examined by measuring the normalized current–voltage $(V_G - I_D)$ characteristics at different drain voltages, as shown in Fig. 4(a). At 300 K, the subthreshold current has no significant change with the increased drain bias. On the other hand, at 450 K, the subthreshold leakage current significantly increases with a higher drain bias. Furthermore, the stretch-out phenomenon is more noticeable when the drain bias becomes larger, and the subthreshold leakage current saturates for drain voltages above 5 V. When the drain bias increases, the large transverse electrical field causes more holes drift to the source region, as shown in Fig. 4(b). The more holes made, source barrier lowering became more serious. Thus, the subthreshold leakage current raises with increasing drain bias. On the other hand, when the drain bias is above 5 V, the total holes drift to the source region; thus, source barrier lowering would saturate no matter how the drain bias increases. Therefore, the stretch-out phenomenon saturates when the drain bias is above 5 V.

IV. Conclusion

The transfer characteristics of a-IGZO TFTs exhibit an apparent subthreshold current stretch-out phenomenon at high temperature, which becomes more serious with increasing temperatures. The experiment of NBTI has been used to prove high-temperature-induced hole generation. Furthermore, the transfer characteristics with different drain voltages have been also used to confirm the status of hole accumulation. These pieces of evidence clearly defined the stretch-out phenomenon, which is caused by thermal-induced hole generation and accumulation at the source region that leads to source-side barrier lowering.

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