A Novel SONOS Memory With Recessed-Channel Poly-Si TFT via Excimer Laser Crystallization

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***Abstract*—A silicon–oxide–nitride–oxide–silicon memory with recessed-channel (RC) polycrystalline-silicon (poly-Si) thin-film transistors (TFTs) via excimer-laser crystallization (ELC) has been demonstrated to achieve a high mobility of $\sim$ 400 $cm^2/V \cdot s$ and a large ON/OFF current ratio of $\sim 10^8$. Such a high performance is because the RC poly-Si TFTs possess only one perpendicular grain boundary (GB) in the channel and the corresponding protrusion at this GB. In addition, the proposed devices also exhibited the largest memory window of 2.63 V in 10 ms with respect to 2.37 and 1.31 V for the conventional-ELC and solid-phase-crystallized ones, respectively. Since the silicon grain growth could be artificially controlled, the device-to-device uniformity could be significantly improved. Therefore, such a simple scheme is promising for applications of low-temperature poly-Si TFTs in 3-D ICs and system on panel.**

***Index Terms*—Excimer-laser crystallization (ELC), lateral grain growth, nonvolatile memory, recessed-channel (RC), thin-film transistor (TFT).**

I. Introduction

Low-temperature polycrystalline-silicon thin-film transistors (TFTs) played an important role in active-matrix (AM) liquid-crystal displays (LCDs) and AM organic light-emitting diodes owing to the integration of driver circuities on a panel [1], [2]. Thus, a device having high-performance transistor characteristics is required for the system-on-panel application [3].

For TFT-LCD portable products, however, power consumption should be overcome [4]. Some research works have reported that the backlight system and ac power supply should be the major factors of power consumption [5]. Therefore, the memory-in-pixel technology was proposed to achieve low power consumption [6], [7]. As a result, a device with TFT and memory characteristics, which is so-called bifunctional, is becoming more and more important for future applications.

From the viewpoint of TFT performance, the excimer-laser-crystallized (ELC) poly-Si TFTs always display better driving ability than the solid-phase-crystallized (SPC) ones. However, the uniformity issue and narrow process window were found in the ELC ones. Despite some of grain-enlargement methods to solve these problems, they might impose some complexity on device fabrication [8], [9]. In the perspective of memory characteristics, the electric-enhanced structures, such as nanostructures [10], [11] or Si protrusions [12], could improve the program/erase behavior. Nevertheless, some reports mentioned that the Si protrusions fabricated by sequential lateral solidification might also have a uniformity problem [11]. Bandgap engineering [13], nanocrystal trapping layer [14], and dual-gate structure [15] were proposed to improve memory characteristics. However, the poor quality of the SPC poly-Si channel comprising many dangling bonds along the grain boundaries (GBs) suffered from the reliability issue [16].

Based on our previous study [3], the poly-Si TFTs with a recessed-channel (RC) structure could provide high-performance transistor characteristics. Thus, in this letter, the ELC silicon–oxide–nitride–oxide–silicon (SONOS) memory with RC poly-Si TFT structures is proposed to obtain superior transistor performance and high program/erase efficiency. Since the grain growth and the corresponding protrusion at the GB could be artificially controlled, the memory characteristics and device uniformity could therefore be improved.

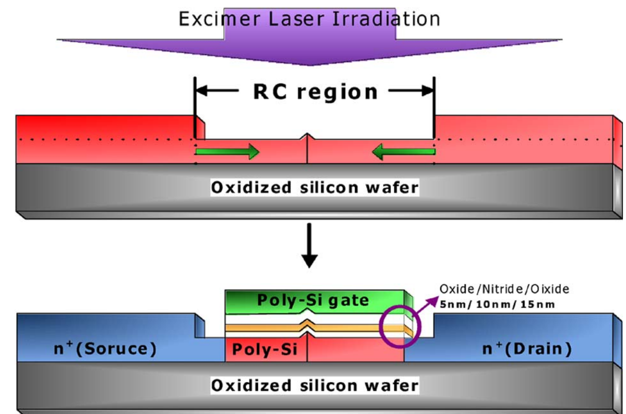

Fig. 1. Schematic diagrams of the key-process procedures of the proposed RC-ELC SONOS poly-Si TFTs.

II. Device Fabrication

Fig. 1 shows the key fabrication steps for the proposed RC SONOS TFTs crystallized with ELC. First, a 100-nm-thick amorphous-silicon (a-Si) layer was deposited by low-pressure

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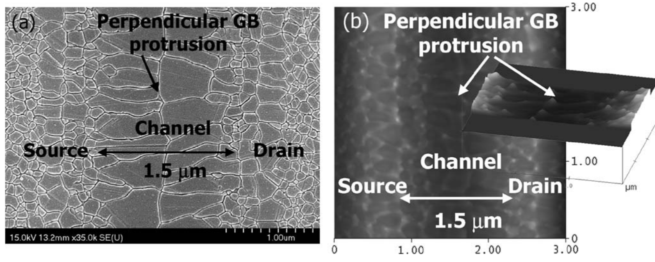

Fig. 2. (a) SEM image and (b) AFM photograph of the ELC poly-Si thin film with RC structure. The grain size can be achieved to about 0.75 μm. The height of protrusion is about 8 nm at the perpendicular GB.

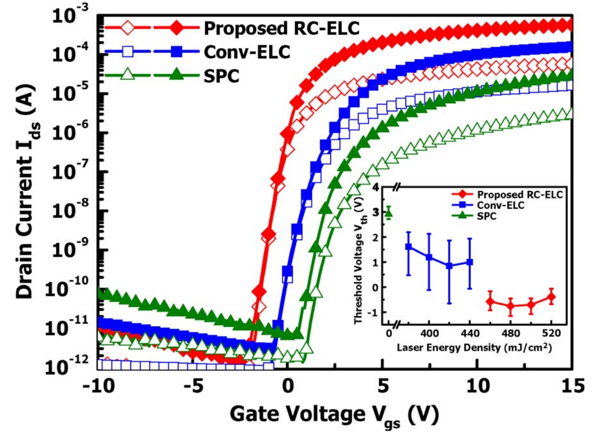

Fig. 3. Typical transfer characteristics of the RC-ELC, conv-ELC, and SPC SONOS TFTs. The inset is the dependence of threshold voltage on applied laser energy density for the RC-ELC, conv-ELC, and SPC SONOS TFTs.

chemical vapor deposition (LPCVD) at 550 °C on oxidized silicon wafers. Next, the a-Si layer located in the channel region was etched off. Then, a 100-nm-thick a-Si layer was subsequently deposited to form an RC structure. Afterward, the a-Si films were irradiated by a KrF excimer laser ($\lambda = 248$ nm) at room temperature. The excimer-laser energy density was selected to attain only one perpendicular GB in the RC structure [3]. After the definition of the active regions, sequential deposition of an ONO stacked gate dielectric (5 nm/10 nm/15 nm) and a 100-nm-thick *in situ* phosphorus-doped polysilicon layer were formed by LPCVD. After the definition of the gate electrodes, a self-aligned phosphorous implantation with a dose of 5×10^{15} cm^{-2} was carried out to form the source and drain regions. Then, a TEOS passivation oxide layer was deposited, and source/drain-implanted dopant activation was performed by the furnace anneal at 600 °C for 8 h. Finally, contact hole opening, metallization, and a 30-min sintering process were conducted to complete the fabrication of the RC-ELC SONOS devices. For comparison, the conventional-ELC (conv-ELC) and solid-phase-crystallized (SPC) SONOS ones were also fabricated. The devices had channel widths and lengths of 1 μm.

III. Results and Discussion

Fig. 2(a) shows the scanning electron microscope (SEM) image of the RC-ELC poly-Si lm. As the laser irradiation energy density was properly selected to be 460–520 mJ/cm^2, a spatially controlled silicon grain with a length of 0.75 μm and one perpendicular GB were successfully formed in the channel region. It was attributed to the fact that the silicon grain growth was controlled starting from the thicker a-Si, both sides toward the middle channel region, and then impinging in the center of the channel. Meanwhile, a perpendicular GB along with a silicon protrusion could therefore be formed in the center of the channel. The atomic force microscopy (AFM) image of the RC-ELC poly-Si surface morphology, as shown in Fig. 2(b), indicated the protrusion with about 8 nm in height at the perpendicular GBs.

Fig. 3 shows that the subthreshold swing and field-effect mobility were 0.304 V/dec and 403 cm^2/V $\cdot$ s for the RC-ELC devices, 0.491 V/dec and 125 cm^2/V $\cdot$ s for the conv-ELC ones, and 0.705 V/dec and 29.9 cm^2/V $\cdot$ s for the SPC devices, respectively. The inset of Fig. 3 presents the dependence of threshold voltage (V_{th}) on applied laser energy density for the RC-ELC SONOS TFT, conv-ELC, and SPC ones. As compared

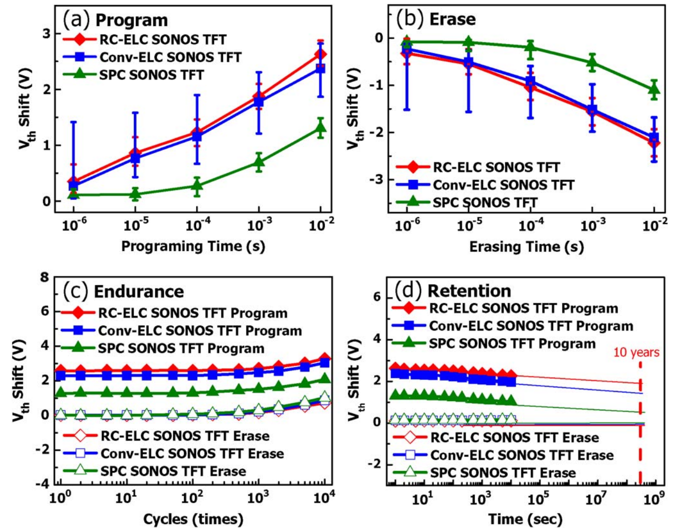

Fig. 4. (a) Threshold-voltage (V_{th}) shift comparison of RC-ELC, conv-ELC, and SPC devices at a program bias of 20 V. (b) Threshold-voltage (V_{th}) shift comparison of RC-ELC, conv-ELC, and SPC devices at an erase bias of −20 V. (c) Endurance and (d) retention characteristics of RC-ELC, conv-ELC, and SPC devices.

with the conv-ELC SONOS TFTs, the RC-ELC ones demonstrated smaller threshold voltage and electrical variation. On the other hand, the SPC ones possessed a high threshold voltage in spite of the small device deviation.

In the perspective of memory operation, Fig. 4(a) shows the V_{th} shift comparison of the SONOS TFTs with a Fowler–Nordheim tunneling mechanism at an applied gate voltage of 20 V. The proposed RC-ELC ones demonstrated the largest V_{th} shift of 2.63 V in 10 ms with respect to 2.37 and 1.31 V for the conv-ELC and SPC ones, accordingly. Furthermore, Fig. 4(b) shows the same trend that the RC-ELC device had the fastest erase speed as compared to the other two counterparts. It indicated that the P/E efficiencies could be markedly enhanced by the introduction of the GB protrusion [12]. Meanwhile, the larger V_{th} shift variation was also found in the conv-ELC devices than the proposed RC-ELC ones due to the random distribution of the GBs, as shown in Fig. 4(a) and (b). The endurance characteristics of the devices are shown

in Fig. 4(c). Although the rate of memory-window narrowing increased upon increasing P/E cycles, the proposed RC-ELC devices revealed good endurance that the memory window was well maintained at about 2.55 V with a small reduction after 10 000 P/E cycles, while the conv-ELC and SPC ones displayed 2.17 and 1.05 V, accordingly. The retention times of the RC-ELC devices could be extrapolated up to ten years for a 1.8-V memory window at room temperature, as shown in Fig. 4(d), while the conv-ELC and SPC ones showed 1.5 and 0.6 V memory windows, correspondingly.

In order to examine the electric-field enhancement by GB protrusion, the electric-field distributions from the gate to the channel were simulated. Indeed, the maximum electric field was increased from 3.94×10^7 to 6.58×10^7 V/cm at the same gate bias of 20 V while the protrusion was introduced. Consequently, the proposed RC-ELC device could acquire a better charge-trapping efficiency in the nitride layer, which is consistent with the experimental results. Therefore, the bifunctional RC-ELC devices could obtain both higher transistor performance and better memory characteristics. Moreover, the uniformity could also be improved.

IV. Conclusion

RC-ELC poly-Si TFTs have been utilized to demonstrate the SONOS memory with excellent electric characteristics. The proposed RC-ELC TFTs exhibited a high field-effect mobility of 403 $cm^2/V \cdot s$ and a steep subthreshold slope of 0.314 V/dec as compared with the conv-ELC and SPC ones, correspondingly. It is because the silicon grain growth was artificially controlled under proper laser irradiation energy density, and meanwhile, a perpendicular GB accompanying with a silicon protrusion was formed in the center of the channel. The RC-ELC devices achieved a large memory window of 2.63 V as compared with 2.37 and 1.31 V for the conv-ELC and SPC ones, respectively. Since the only one perpendicular GB and the dominant protrusion at this GB were controlled at the middle of the channel, it reflected an enhanced electric field structure and an improved device-to-device uniformity. Therefore, the novel SONOS memories with RC poly-Si TFTs are promising for memory-in-pixel and system-on-panel applications.

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