Rapid Prediction of RRAM RESET-State Disturb by Ramped Voltage Stress

Wun-Cheng Luo, Kuan-Liang Lin, Jiun-Jia Huang, Chung-Lun Lee, and Tuo-Hung Hou

***Abstract*—This letter proposes a novel technique for predicting with high confidence the disturbance of the resistive-switching random access memory (RRAM) RESET state based on ramped voltage stress. The technique yields statistical distributions and voltage acceleration parameters equivalent to those of a conventional constant voltage method. Several ramp rates and acceleration models were validated for the accuracy regarding conversion between the two methods. The proposed method not only reduces the time and cost of reliability analysis but also provides a quantitative link between disturbance properties and the widely available RRAM data measured by a linear voltage ramp. Additionally, the non-Poisson area scaling supports the localized filament model.**

***Index Terms*—Read disturb, reliability, resistive switching, resistive-switching random access memory (RRAM), voltage acceleration model.**

I. Introduction

RESISTIVE-switching random access memory (RRAM) has emerged as a promising candidate for nonvolatile memory applications. The switching characteristics and mechanisms have received significant attention recently [1], [2]. However, long-term reliability based on statistically significant data has received less focus despite being crucial for any commercial nonvolatile memory technology. One of the most prominent reliability concerns for RRAM is read disturb. In the popular bipolar-switching RRAM, SET and RESET occur at different voltage polarities. A positive read voltage less than the SET voltage is frequently chosen to prevent the SET (low-resistance)-state disturb, whereas the RESET (high-resistance)-state disturb must be carefully engineered. A recent study by Chen *et al.* [3] has revealed a surprisingly wide statistical distribution of read disturb time $t_{\rm RD}$, posing significant challenges for high-density memory arrays. $t_{\rm RD}$ was typically characterized by time-consuming constant voltage stress (CVS). As a result, most read disturb measurements only reported the result of a single device [4], which is insufficient to statistically project reliability limits for real applications. Alternative methods for rapid prediction are urgently required to facilitate a comprehensive reliability analysis. In contrast, RRAM switching using a linear voltage ramp is a significantly faster measurement, and thus, it is widely reported [5]. However, the quantitative correlation between data from the linear voltage ramp and data from read disturb has not yet been established.

This letter statistically examines the read disturb of the RESET state in a bipolar-switching HfO_2 RRAM. Read disturb and SET only differ in the magnitude of applied voltage, and both can be explained by the recovery of percolation paths (conductive filaments) in metal oxide [2], [5]. Inspired by the similar percolation model of dielectric breakdown [6]–[8], ramped voltage stress (RVS) developed from the breakdown theory was proposed to rapidly predict the RESET-state disturb. The proposed method not only reduced the time and cost of reliability analysis but also provided a quantitative link to the widely available RRAM switching data measured by the linear voltage ramp. Additionally, this letter also addressed the voltage acceleration model and $t_{\rm RD}$ dependence on device area, which are both crucial for reliability projection.

II. Experimental Procedures

$Ni/HfO_2/p^+$-Si memory cells were fabricated on heavily doped p^+-Si wafers. First, 30-nm HfO_2 thin films were deposited by metal–organic chemical vapor deposition at 500 °C using $Hf(OtBu)_2(mmp)_2$ and O_2 as precursors. Then, Ni top electrodes (TEs) with a thickness of 100 nm were defined using sputtering and liftoff processes. The area was 10^4 μm^2 unless otherwise noted. Voltage was applied to the Ni TEs at room temperature while the p^+-Si substrates (bottom electrodes) were grounded using an Agilent 4156B parameter analyzer. The memory cells exhibited reproducible bipolar resistive switching after the initial forming process. The switching characteristics and mechanism have been discussed in detail elsewhere [9]. $t_{\rm RD}$ and $V_{\rm SET}$ were measured using conventional CVS and RVS procedures on cells that were first programmed to the RESET state. The time duration of a linear voltage ramp with a 100-mV step was adjusted to realize different voltage ramp rates in RVS. The read disturb or SET events were monitored using a current threshold of 100 μA, and a current compliance value of 1 mA was applied to prevent permanent damage to the cell. Fluctuations of the critical RRAM parameters such as switching voltages and resistance are known to be substantial even for an identical device under cycling. This intrinsic stochastic nature is well explained by the percolation model [5], and it should be considered the fundamental limit of RRAM reliability. Therefore, instead of measuring numerous cells, which would be susceptible to other extrinsic effects such as device uniformity, an identical cell was reset at a negative

Manuscript received November 29, 2011; revised January 16, 2012; accepted January 18, 2012. Date of publication March 6, 2012; date of current version March 23, 2012. This work was supported by the National Science Council of Taiwan under Grant NSC 97-2218-E009-039-MY3. The review of this letter was arranged by Editor M. Jurczak.

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Digital Object Identifier 10.1109/LED.2012.2185838

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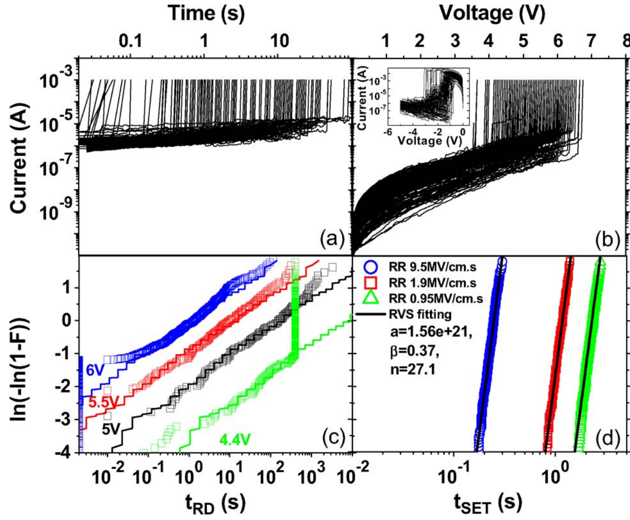

Fig. 1. (a) Current–time traces for CVS at 5.5 V. (b) Current–voltage traces for RVS with a constant ramp rate of 1.9 MV/cm · s. (Inset) RESET traces after RVS. (c) t_{RD} measurement by CVS (square symbols) at 4.4, 5, 5.5, and 6 V presented in a Weibull plot with an extracted β around 0.37. The solid lines refer to results converted from RVS. (d) t_{SET} measurement by RVS with three different ramp rates presented in a Weibull plot. The parameters in the power law model were fit from (2)–(4).

bias after every CVS or RVS measurement. At least 200 and 400 switching cycles were measured for every CVS and RVS condition, respectively. Random variation on resistance showed that no additional stress effect occurred during cycling. To select the representative cell, an upfront screening using RVS was first applied to cells across the wafer. The variation on switching voltages among different cells was confirmed significantly less than that of an identical cell under cycling (not shown). Fig. 1(a) shows the typical CVS current–time traces at 5.5 V, whereas Fig. 1(b) shows the typical RVS current–voltage traces with a constant ramp rate of 1.9 MV/cm · s. The relatively high V_{SET} and low RESET-state current in our device may be attributed to the choice of the Si bottom electrode [10]. The inset in Fig. 1(b) shows the typical RESET traces after RVS.

III. Results and Discussion

Similar to the statistical Weibull distribution of the constant voltage time-dependent dielectric breakdown, the cumulative failure (read disturb) probability F_{CVS} after stress time t at a constant stress voltage V_{ox} is defined as [7]

$$F_{\mathrm{CVS}}(t, V_{\mathrm{ox}}) = 1 - \exp\left[-\left(\frac{t}{\eta(V_{\mathrm{ox}})}\right)^{\beta}\right] \quad (1)$$

$$\eta(V_{\mathrm{ox}}) = a \cdot V_{\mathrm{ox}}^{-n} \quad (2)$$

where η is the characteristic time at the 63rd failure percentile and β is the Weibull slope. Here, the voltage acceleration process was described by the power law model in the dielectric breakdown theory with prefactor a and acceleration exponent n [11]. However, any appropriate voltage acceleration model, such as the popular E-model $(\eta = \tau_0 \exp(-\gamma E))$ and 1/E-model $(\eta = \tau_E \exp(-G/E))$, can be also used. Fig. 1(c) shows the t_{RD} results in a Weibull plot with an extracted β of 0.37 independent of the CVS voltages. The measurement

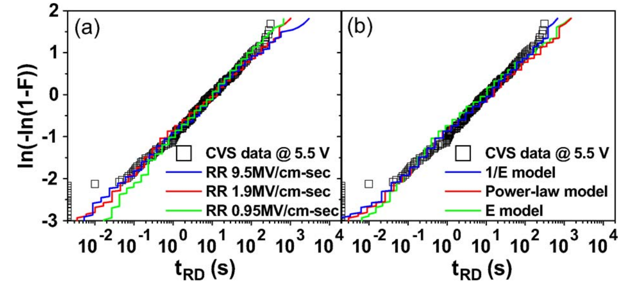

Fig. 2. (a) Comparison of three ramp rates in RVS-to-CVS conversion. The power law model was applied in the conversion. (b) Comparison of three voltage acceleration models in RVS-to-CVS conversion. A constant ramp rate of 1.9 MV/cm · s was applied in RVS. $\beta = 0.37$, E-model parameters $\tau_0 = 4e + 10$ s, $\gamma = 4.1$ cm/MV, and 1/E-model parameters $\tau_E = 8.2e - 13$ s and $G = 56.3$ MV/cm were used in the conversion.

over 400 s was terminated for CVS at 4.4 V, but the tail of the distribution demonstrated a fixed β as that obtained at high stress voltages, which allowed us to extrapolate with confidence to higher percentiles. The small β was explained by a very thin defective oxide layer, where the conductive filaments reconnected at the disturb condition [3]. The thickness fluctuation of this thin oxide layer during cycling may also contribute to the small β.

In Fig. 1(d), the measured time-to-SET t_{SET} from RVS is presented in a Weibull plot. The RVS method was typically several orders of magnitude faster than the conventional CVS method was in establishing a meaningful Weibull distribution, as evidenced in Fig. 1(c) and (d). RVS is equivalent to a series of discrete CVS steps with linearly ascending stress voltages. Assuming that the stress effects on defect generation are cumulative, (1) may be modified for the cumulative failure probability of RVS as [7]

$$F_{\mathrm{RVS}}(t_i, V_{\mathrm{ox},i}) = 1 - \exp\left[-\left(\frac{t_i}{\eta(V_{\mathrm{ox},i})}\right)^{\beta}\right], \ i = 1$$

$$= 1 - \exp\left[-\left(\frac{t_i - t_{i-1} + \tau_{i-1}}{\eta(V_{\mathrm{ox},i})}\right)^{\beta}\right], \ i \geq 2 \quad (3)$$

$$\tau_{i-1} = (t_{i-1} - t_{i-2} + \tau_{i-2}) \cdot \left(\frac{V_{\mathrm{ox},i-1}}{V_{\mathrm{ox},i}}\right)^{n} \quad (4)$$

where i is the index of discrete CVS steps at RVS, t_i is the cumulative stress time to the ith step, and τ_{i-1} is the equivalent age of CVS at $V_{\mathrm{ox},i}$ accounting for all RVS history until the previous $(i-1)^{\mathrm{th}}$ step, $F_{\mathrm{RVS}}(t_{i-1}, V_{\mathrm{ox},i-1}) = F_{\mathrm{CVS}}(\tau_{i-1}, V_{\mathrm{ox},i})$. Equation (4) was derived from the power law model, but alternative expressions may be also derived for other voltage acceleration models [7]. Parameters β, a, and n were fit from the RVS data using (2)–(4), as shown in Fig. 1(d) [7]. A constant Weibull slope β was assumed considering only monomodal distributions. In RVS–CVS conversion, time duration at each CVS step in RVS was converted to equivalent age at the use conditions of CVS using (4) and the extracted parameters in Fig. 1(d) [7]. The converted t_{RD} from RVS matched extremely well with those from CVS at all four stress voltages, as shown in Fig. 1(c). To further validate the conversion, three different RVS ramp rates were verified. The converted t_{RD} were all in good agreement with that from CVS, as shown in Fig. 2(a).

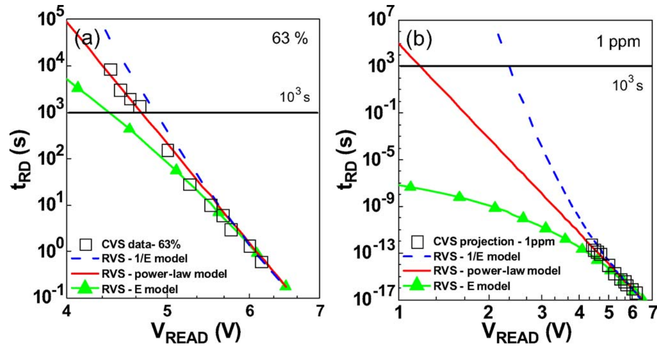

Fig. 3. Projection of reliable read voltage for a disturb lifetime of 10^3 s at both (a) high and (b) low failure percentiles. The symbols refer to the $t_{\rm RD}$ measurement or projection by multiple CVS, and the lines refer to the $t_{\rm RD}$ conversion from a single RVS with a constant ramp rate of 1.9 MV/cm · s and different voltage acceleration models.

The voltage acceleration model plays a significant role in the RVS–CVS conversion methodology and the projection to use conditions for CVS. Three models, i.e., the power law model, E-model, and 1/E-model, were evaluated regarding the RVS–CVS conversion, as shown in Fig. 2(b). Good quantitative agreement validated the conversion methodology of different acceleration models provided that the cumulative process of RVS was completely captured in (2)–(4). Using only a single set of RVS data, Fig. 3(a) further shows that all the three different models were reasonably accurate in predicting the CVS $t_{\rm RD}$ data between 5 and 6.15 V at the 63rd failure percentile. However, the discrepancy in extrapolation to low read voltages significantly increased among different acceleration models, particularly when predicting the lifetime at a low failure percentile of 1 ppm using (1), as shown in Fig. 3(b). The uncertainty of the conversion can be greatly reduced by predetermining the most applicable acceleration model using additional CVS $t_{\rm RD}$ data at low voltages. The CVS results at 4.4 to 4.7 V in Fig. 3(a) supported the power law model widely adopted for the ultrathin oxide breakdown [11]. This was consistent with the belief that the rupture/connection of conductive filaments in RRAM occurred within a very small portion of the entire oxide layer [1], [2]. A read voltage less than 1.1 V was sufficient to guarantee the lifetime of 10^3 s for the failure percentile at 1 ppm. However, this value is only valid for the particular samples analyzed in this letter. Prediction on other RRAMs should be separately examined using the similar analysis technique. Moreover, the area dependence on read disturb is critical for RRAM scaling. In the dielectric breakdown theory, the area scaling follows Poisson statistics in assuming a homogeneous probability of defect generation across the area. The time to breakdown is proportional to $A^{-1/\beta}$ [6]. In contrast, no area dependence was observed for RRAM $t_{\rm RD}$ measured by CVS, as shown in Fig. 4. The non-Poisson area scaling suggested that the disturb process was highly localized in a region significantly smaller than the device size, supporting the filament model in RRAM [1], [2]. Hence, the read disturb may not be greatly relieved by cell-size scaling alone.

IV. Conclusion

This letter has proposed a new RVS technique for the rapid prediction of RRAM RESET-state disturb. The proposed

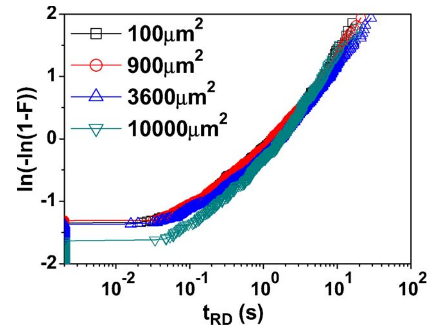

Fig. 4. Area dependence of $t_{\rm RD}$ measured by CVS at 6.15 V for areas in the range of $10^2 - 10^4$ μm^2.

method yielded $t_{\rm RD}$ distributions and voltage acceleration parameters equivalent to those of the time-consuming CVS method. The conversion between RVS and CVS was derived from the fundamental dielectric breakdown theory, independent of the use conditions such as the RVS ramp rate and the CVS voltage. Additionally, the non-Poisson area scaling suggested that the RESET-state disturb would probably continue to pose challenges for scaled RRAM in the future.

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