A Static Linear Behavior Analog Fault Model for Switched-Capacitor Circuits

Hao-Chiao Hong, *Member, IEEE*

***Abstract*—This paper proposes a static linear behavior (SLB) analog fault model for switched-capacitor (SC) circuits. The SC circuits under test (CUT) are divided into functional macros including the operational amplifiers, the capacitors, and the switches. Each macro has specified design parameters from the design's perspectives. These design parameters constitute a parameter set which determines the practical transfer function of the CUT. The SLB fault model defines that a CUT is faulty if its parameter set results in transfer functions whose frequency responses are out of the design specification. We analyzed the fault effects of the macros and derived their faulty signal-flow graph models with which the faulty transfer function templates of the CUT can be automatically generated. Based on the templates, we proposed a test procedure that can estimate all the parameters in the parameter set so as to test the CUT with multiple faults. Different from conventional single fault assumption, the proposed SLB fault model covers concurrent multiple parametric faults and catastrophic faults. In addition, it does not need to conduct fault simulations before test as conventional analog fault models do. As a result, it addresses the impractically long fault simulation time issue. A fully-differential low-pass SC biquad filter was adopted as an example to demonstrate how to design and use efficient multitone tests to test for the parameter set. The multitone test results acquired during the test procedure also reveal the distortion and noise performance of the CUT though the SLB fault model does not include them.**

***Index Terms*—Analog fault model, mixed-signal testing, parametric faults, switched-capacitor (SC).**

I. Introduction

A PRACTICAL fault model helps to simplify testing problems. We do not have to know what and where physical defects are but their faulty effects on the circuit behaviors. Based on the fault model, efficient tests can be generated to ensure the quality of the circuits under test (CUT) with a low test cost. For example, the stuck-at fault model is the most popular fault model for digital circuits. It has been successfully applied to test digital circuits for decades [1], [2].

However, analog fault models are not as mature as the digital ones [3]. Due to the lack of an adequate analog fault model, functional tests are widely adopted in testing analog circuits [1]. Remaining issues are what and how many functional tests are necessary to ensure the quality of the CUT.

The major issues of developing a practical analog fault model include the following [1], [2], [4].

1) *Zero noise margin*: Unlike digital circuits that have large noise margins, analog circuits have almost zero noise margins. It is hard to tell a fault-free analog response from a faulty one in time domain due to the presence of the intrinsic noise. Hence, most successful test methods of analog circuits are statistical to alleviate the effects of noise [1].
2) *Nondeterministic transfer functions*: The acceptable transfer function of an analog CUT is nondeterministic. Any transfer function whose frequency responses comply with the design specification passes the test. Therefore, making pass/fail decisions is more confusing for analog circuits.
3) *Too long fault simulation time*: Fault simulations are used to be substantial for efficient test generation which is one of the main applications of fault models. Conventionally, analog fault simulations are conducted with circuit-level simulators such as SPICE to provide good accuracy at the cost of a longer simulation time. However, the required analog fault simulation number is usually very large. Consequently, the required fault simulation time may become too long to be acceptable.
4) *Complex causal relationships*: Most analog circuit designs extensively use negative feedbacks to address the process, voltage, temperature, and noise (PVTN) variation issues. The feedbacks make analyzing the impacts of a defect of an element such as a transistor very difficult in the conventional way. It is analogous to the scenario that testing sequential digital circuits is more difficult than testing combinational digital circuits due to the feedbacks. To test sequential circuits, we usually have to well control their previous states by using scan chains. However, it is very laborious and not preferable to set the previous states of analog feedback circuits because of the extreme accuracy requirement of analog signals.

Analog faults are generally classified into two catalogs: catastrophic and parametric faults [5], [6]. A catastrophic fault is a fault that changes the circuit netlist such as a short or an open wire. Catastrophic faults usually result in a dramatic change of the CUT's transfer function [3]. On the other hand, parametric faults represent parameter shifts of the

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The author is with the Department of Electrical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: hchong@cn.nctu.edu.tw).

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components in the CUT such as variations of resistance values, capacitance values, and trans-conductances and intrinsic gains of transistors. Parametric faults lead to subtle changes of the coefficients in the transfer function of the CUT.

The great success of the stuck-at fault model of digital circuits inspired researches to extend its applications to analog circuits [7]–[9]. The catastrophic fault models help in generating efficient tests for quickly sieving out the open/short circuits in analog CUTs [10].

Parametric faults are more difficult to test [3], [11]–[14]. The main issue of testing parametric faults is that the parametric fault list of a single parameter consists of infinite possible values. For example, the PVTN variations would cause the capacitance value of a nominal 1 pF capacitor to be any value within 0.9 to 1.1 pF. In other words, every electrical parameter of a component is a random process whose sample space is infinite. The infinite parametric fault list makes the fault simulation time impractically long. To address this issue, [15]–[18] proposed adopting the structural information of the CUT to reduce the size of the fault set. Another approach to speed up fault simulations is truncating the fault list by considering the most likely faults to occur. Sensitivity analysis can be used to weight the faults [4], [12], [19]–[22]. Statistical approaches also provide fast fault simulations [23], [24].

Switched-capacitor (SC) circuits are very popular in implementing CMOS analog circuits. In this paper, we propose a static linear behavior (SLB) analog fault model for linear SC circuits. This paper is organized as follows. In Section II, we first review conventional design procedures of SC circuits and indicate some useful lessons to learn for testing SC circuits. Then, we define the SLB fault model on the basis of the lessons. Section III discusses the fault effects of linear SC circuits including both parametric and catastrophic faults of the basic building blocks in SC circuits. We derive the faulty signal flow graph (SFG) models of the basic building blocks and show how to automatically generate the faulty transfer function templates of the CUT with the faulty SFG models. With the faulty transfer function templates, we propose a test procedure that can estimate all the parameters in the parameter set so as to test the CUT in Section IV. We also illustrate how to design and conduct efficient tests of an example fully-differential SC biquad filter based on the proposed SLB fault model. Finally, Section V draws our conclusions.

II. Static Linear Behavior Fault Model

To derive a simple but accurate fault model for SC circuits, understanding how to design them is very instructive.

A. Conventional Design Procedure of Switched-Capacitor Circuits

A conventional design procedure of a linear SC circuit is as what follows [25], [26]. At the beginning, a target z-domain transfer function is designed according to the design specification. Next, the transfer function is manipulated to derive several equations which are used to construct the prototype circuits with ideal components. Then, the transfer function of the constructed prototype is analyzed and compared with the target transfer function to determine the capacitor ratios and the clock frequency.

The following step is to include the design parameters of the operational amplifiers (OPAMPs) to the transfer function of the prototype circuits to determine the requirements of the design parameters. In this step, the components are replaced by their linear behavior models. The most critical static design parameters of OPAMPs are their open-loop gains (OPGs) and input-referred offsets [27]–[29]. A too small OPG induces significant errors to the transfer function, while a too large offset would saturate the OPAMP or reduce the output swing of the OPAMP. Therefore, designers usually set some lowest bounds to the OPGs so that the OPAMPs introduce insignificant errors to the CUT's transfer function. It has been shown that the simulation results of a high-resolution SC Σ-Δ modulator with a linear behavior model considering the OPGs and offsets show good agreement with the measurement results [30].

Finally, the designer starts circuit-level designs of the OPAMPs and the switches, and assigns the capacitance values of the capacitors according to the noise requirements. From designers' perspectives, a good design should have moderate design margins to tolerate variations of transistors. In particular, a successful OPAMP design has simulated design parameters fitting in the derived requirements, regardless of what and how transistors are used to build it.

The design procedure provides some lessons.

1) The transfer function of a CUT is the most suitable item to test if the CUT is faulty.
2) Every design parameter in the transfer function of the CUT is a parametric fault candidate. In practice, all the parameters vary simultaneously due to the PVTN variations. Hence, practical parametric faults are multiple.
3) The OPGs and offsets are the key static parameters of the OPAMPs that may lead to faulty transfer functions. Fault-free OPAMPs usually have insignificant impacts on the transfer function of the CUT.
4) The capacitor ratios rather than the absolute capacitance values determine the frequency responses of the CUT. In practice, special layout techniques are often used to enhance the accuracy of the capacitor ratios [31], [32].
5) Transistors are used to build the desired macros. Electrical properties of individual transistors are not important as long as the macro's design parameters do not result in a transfer function out of the design specification. As a consequence, linear behavior models are suitable for the macros constructed by transistors such as the OPAMPs [27], [33]. Following designer's circuit partition reduces the complexity of the test problems and thus is more appealing.

B. Proposed Static Linear Behavior Fault Model

The proposed SLB fault model examines the accuracy of the CUT's z-domain transfer function. We assume the sampling clock period is not an issue so that the responses of the CUT are fully settled. On the basis of fully-settled responses, the frequency responses of the CUT are uniquely determined by its z-domain transfer function. If a CUT is faulty by the SLB fault model, it is also faulty when the responses are not fully-

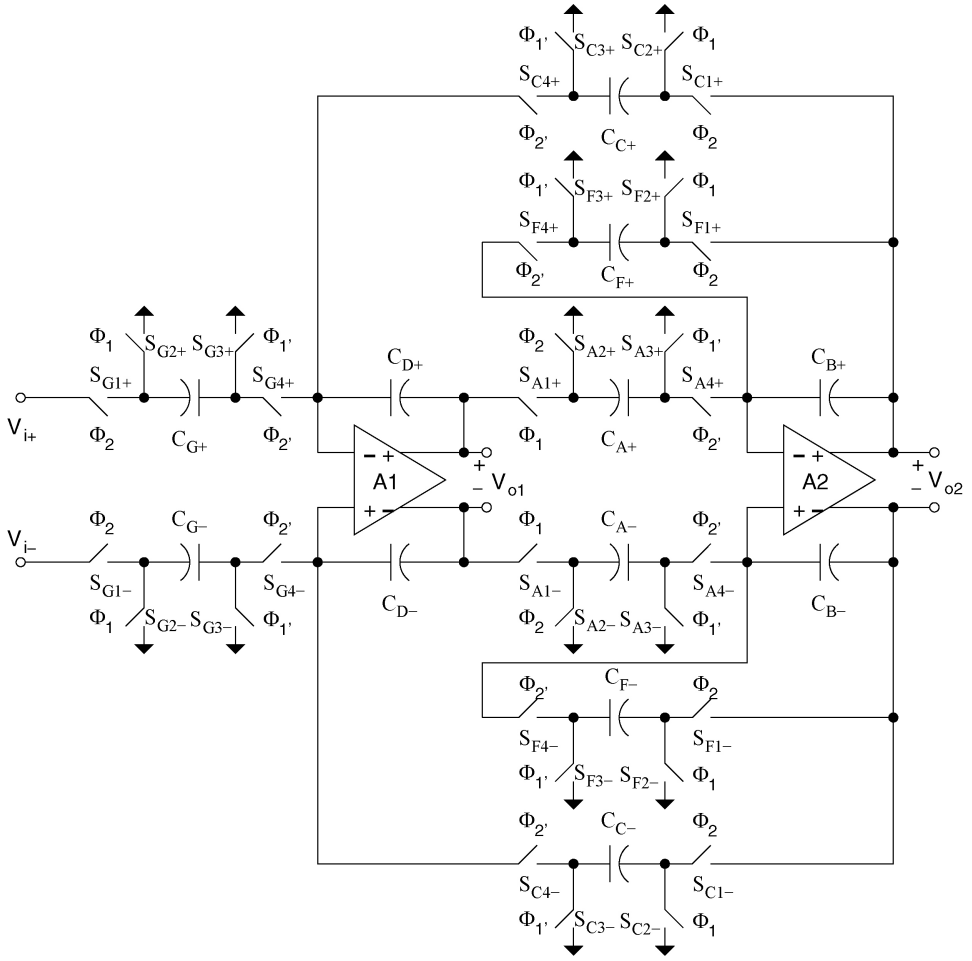

Fig. 1. Schematic of the SC biquad.

settled. The scenario is analogous to the stuck-at faults versus the delay faults of digital circuits.

Based on the lessons learned in Section II-A, we define the SLB fault model as the following.

1) *Applicable Circuits:* The SLB fault model is applicable to linear SC circuits whose transfer functions can be expressed by rational z-domain transfer functions. SC filters are such examples. For those SC circuits that contain additional nonlinear circuit blocks such as comparators, they can be divided into the applicable part and the rest part. Design-for-testability (DfT) techniques such as IEEE 1149.4 mixed-signal test bus [34] can be used for the partition during tests.

2) *Parameter Set:* Every CUT owns a parameter set which consists of the following parameters.

1) OPAMPs: the OPGs and the input-referred offsets of all OPAMPs. The OPGs have the minimal specification and the offsets have the maximal specification.
2) Capacitors: the capacitance ratios of the capacitors to the corresponding feedback capacitors in the CUT. Note that the SLB fault model does not set any specification to the capacitor ratios as to the OPAMPs' OPGs and offsets.
3) Switches: every delay-free and delayed SC branch containing the switches has additional catastrophic fault activators.

Later in Section III, we will discuss why these parameters are defined as parametric fault candidates in detail. We will also depict what the SC branches are and define the corresponding catastrophic fault activators.

3) *Fault Model:* A CUT is defined to be faulty if its parameter set results in transfer functions whose frequency responses are out of the design specification. It is worthy to note that since the SLB fault model adopts the design specification as the thresholds to make the final pass/fail decision of the CUT, these threshold values are deterministic and independent of the variations of process and operation conditions. Consequently, the proposed SLB fault model does not suffer from ambiguous thresholds.

4) *Undetectable Parametric Faults and Parametric Fault Coverage:* A parametric fault is said to be undetectable if its value cannot be derived from the test results.

The parametric fault coverage is defined as the ratio of the number of the parameters that can be estimated according to the test results to the total number of the parameters in the parameter set excluding the catastrophic fault activators of the SC branches.

5) *Equivalent Faults:* Two faults are equivalent if they result in the same transfer function of the CUT.

TABLE I
DESIGN PARAMETERS OF THE CUT

Parameters	Designated Values	Specification
C_A	1.147096 pF	n/a
C_B	16.36952 pF	n/a
C_C	0.382366 pF	n/a
C_D	11.47096 pF	n/a
C_F	1.147096 pF	n/a
C_G	0.382366 pF	n/a
A_1	80 dB	>60 dB
A_2	80 dB	>60 dB

6) *Fault Masking:* A parametric fault is said to be masked if it becomes undetectable due to the presence of some other faults.

III. FAULTS AND FAULTY SIGNAL FLOW GRAPH MODELS OF SWITCHED-CAPACITOR CIRCUITS

In the following, we use a Fleischer–Laker low-pass SC biquad shown in Fig. 1 as an example to explain the faults in linear SC circuits and their faulty behaviors. Specifically, we will derive the SFG models of the basic building blocks of linear SC circuits under faults. The SFG analysis method is very popular for analyzing SC circuits [35]. It is a systematic approach that can automatically generate the transfer functions of the CUT. With the derived faulty SFG models, an EDA tool can be built to automatically derive the faulty transfer function templates of any linear SC circuit. Then, we test for the parameters in the parameter set according to the templates and use the tested transfer functions to make the pass/fail decision based on the SLB fault model.

A. Circuits Under Test

Fig. 1 depicts the schematic of the example CUT. Like general SC circuits, the SC biquad consists of OPAMPs, switches, and capacitors. The design specification of the CUT consists of a passband from DC to 20 kHz, a sampling rate of 6.144 MHz, a passband gain inbetween -3 to 3 dB, a passband ripple within ± 0.5 dB, a stopband after 1 MHz, and a minimum stopband attenuation of 40 dB in the stop band. Following the design procedure described in Section II-A, the target parameter set and the specification are summarized in Table I.

B. Fault-Free Signal Flow Graph Models

Fig. 2 shows the common building blocks to implement SC circuits and their SFG models.

The SFG of a single-ended SC circuit is constructed by replacing every integrator and SC branch shown in Fig. 2 with the corresponding model listed in Table II. The resulted SFG of the CUT is shown in Fig. 3. It is worthy to note that Fig. 3 also represents the SFG of the fully-differential implementation shown in Fig. 1. After simple manipulations, the overall input and output relationship (IOR) of the CUT can be derived from the SFG which is

$$V_{O2}(z) = STF_{H2}(z)V_i(z) + OTG_{12}V_{OS1} + OTG_{22}V_{OS2}. \quad (1)$$

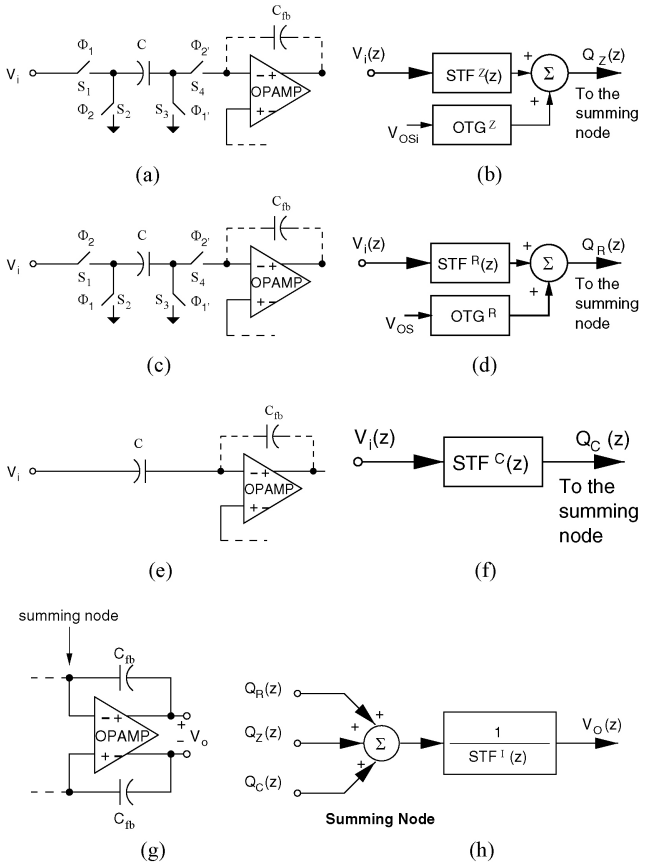

Fig. 2. Common building blocks in linear SC circuits and their SFG models. (a) Delayed SC branch. (b) SFG of the delayed SC branch. (c) Delay-free SC branch. (d) SFG of the delay-free SC branch. (e) Purely capacitive branch. (f) SFG of the purely capacitive branch. (g) Integrator. (h) SFG of the integrator.

Equation (1) includes the signal transfer function (STF) and the offset transfer gain (OTG) where the STF is an AC term expressed as

$$STF_{H2}(z) = \frac{-STF_A^Z(z)STF_G^R(z)}{DEN(z)} \quad (2)$$

$$DEN(z) = STF_A^Z(z)STF_C^R(z) + STF_D^I(z)STF_F^R(z) - STF_B^I(z)STF_D^I(z) \quad (3)$$

and the OTGs are DC terms whose values are

$$OTG_{12} = (OTG_G + OTG_C)\frac{-STF_A^Z(z)}{DEN(z)}\bigg|_{z=1}$$

$$OTG_{22} = (OTG_A + OTG_F)\frac{-STF_D^I(z)}{DEN(z)}\bigg|_{z=1}. \quad (4)$$

By Table II and (1)–(3), the design target of the STF of the biquad is

$$V_{O2}(z) = \frac{-\frac{C_A}{C_B}\frac{C_G}{C_D}z^{-1}V_i(z)}{(1+\frac{C_F}{C_B}) - (2 - \frac{C_AC_C}{C_BC_D} + \frac{C_F}{C_B})z^{-1} + z^{-2}}, \quad (5)$$

because the fault-free OPAMPs have zero offsets.

The SFG also shows the IOR of the internal output, V_{O1}, of the CUT is

$$V_{O1}(z) = STF_{H1}(z)V_i(z) + OTG_{11}V_{OS1} + OTG_{21}V_{OS2} \quad (6)$$

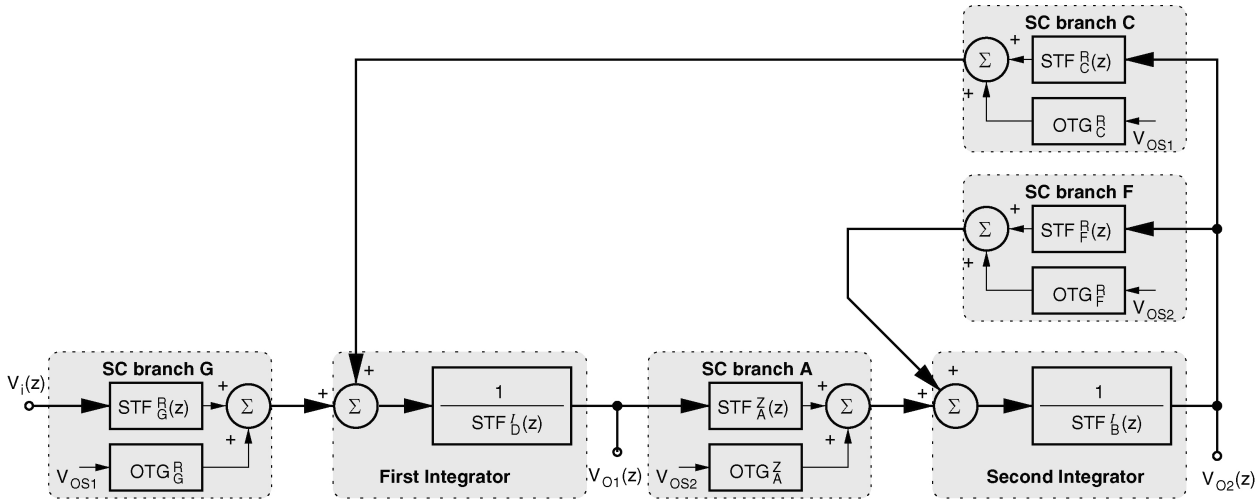

Fig. 3. SFG of the SC biquad.

TABLE II
FAULT-FREE SFG MODELS OF THE SC BRANCHES AND THE INTEGRATOR WITH AN IDEAL OPAMP

Network	Schematic	SFG Model	
Delayed branch	Fig. 2(a)	$STF^Z(z) = Cz^{-1}$	$OTG^Z = C$
Delay-free branch	Fig. 2(c)	$STF^R(z) = -C$	$OTG^R = C$
Purely capacitive branch	Fig. 2(e)	$STF^C(z) = -C(1 - z^{-1})$	N/A
Integrator	Fig. 2(g)	$STF^I(z) = C_{fb}(1 - z^{-1})$	N/A

where

$$STF_{H1}(z) = \frac{STF_G^R(z)(STF_F^R(z) - STF_B^I(z))}{DEN(z)} \tag{7}$$

and

$$OTG_{11} = (OTG_G + OTG_C) \times \left.\frac{(STF_F^R(z) - STF_B^I(z))}{DEN(z)}\right|_{z=1}$$
$$OTG_{21} = (OTG_A + OTG_F)\left.\frac{-STF_C^R(z)}{DEN(z)}\right|_{z=1}. \tag{8}$$

C. Faulty Signal Flow Graph Models of Single-Ended Switched-Capacitor Circuits

Recall that a faulty CUT is defined as the one whose transfer functions lead to frequency responses out of the design specification. Therefore, it is preferable to derive the STF containing all the design parameters with which we can make the pass/fail decision once the design parameters are known. Following the SFG analysis procedure but with the faulty SFG models of the components is an appealing approach. In the following, we will discuss the fault effects of the catastrophic and parametric faults of every building blocks and derive the corresponding faulty SFG models.

1) *Faults of OPAMPs:* Every OPAMP is defined to have two parametric faults including its OPG and input-referred offset and their corresponding specification.

The catastrophic faults in an OPAMP are very fatal because the OPAMP itself is a very sensitive design. Short faults of the transistors in an OPAMP usually result in zero AC output. Their faulty syndromes are as if the OPAMP has a zero OPG. Similarly, open faults of the transistors in an OPAMP usually lead to significant degradation of the OPG and/or increase of the offset. Nevertheless, the fault effects of the catastrophic faults of an OPAMP are covered by the two parametric faults of the same.

Let A_1, A_2, V_{OS1}, and V_{OS2} represent the OPGs and the input-referred offset voltages of the two OPAMPs of the example CUT, respectively. Detailed circuit analyses show that the finite OPGs of the OPAMPs change the term $STF^I(z)$ in Table II to be

$$STF^I(z) = C_{fbi}(\alpha_i - \beta_i z^{-1}) \tag{9}$$

where

$$\begin{aligned} \alpha_i &= 1 + \frac{C_{Ti}}{A_i C_{fbi}} \\ \beta_i &= 1 + \frac{C_{Ti} - C_{cbi}}{A_i C_{fbi}}. \end{aligned} \tag{10}$$

C_{fbi}, C_{Ti}, and C_{cbi} represent the feedback capacitance value, the total capacitance value of all SC branches connecting to the input node of the OPAMP, and the total capacitance value of the purely capacitive branches of the ith integrator, respectively. For the biquad, we have

$$\begin{aligned} C_{T1} &= C_C + C_D + C_G + C_{p1} \\ C_{T2} &= C_A + C_B + C_F + C_{p2} \\ C_{fb1} &= C_D \\ C_{fb2} &= C_B \\ C_{cb1} &= C_D + C_{p1} \\ C_{cb2} &= C_B + C_{p2}. \end{aligned} \tag{11}$$

C_{p1} and C_{p2} are the parasitic capacitors at the input nodes of the first and the second OPAMPs, respectively. These two parasitic capacitors have no significant effect on the transfer function of the CUT if the OPGs of the OPAMPs are high enough.

2) *Faults of Capacitors:* Each capacitor may introduce a parametric fault if its capacitance results in a faulty STF. Note that it is the capacitor ratios of the capacitors to the feedback capacitors of the corresponding integrators that determine the coefficients of the transfer function, rather than the absolute capacitance values. Hence, the parametric fault number of the capacitors in the CUT is equal to the difference of the total capacitor number and the feedback capacitor number of the CUT.

The open/short catastrophic faults of a capacitor are equivalent to zero/infinite capacitance values. Therefore, it is sufficient to examine the parametric faults only.

3) *Fault Effects of Switches:* The switches have digital functions, turn-on and turn-off. The variations of their on-resistance values do not matter since we assume every response of the CUT is fully-settled. Hence, the stuck-open/short fault model for digital circuits is suitable for the switches as well [36].

In Fig. 2, only the delayed and delay-free SC branches contain switches. Similar to the cases of digital circuits, it is adequate to assume only one of the four switches of the same SC branch has a stuck fault at a time. The faulty effects of the stuck switches can be analyzed by using the charge conservation principle.

Let us analyze the impacts of the stuck switches on the SFG model of a delayed SC branch. If S_1 or S_4 is stuck-open, then no charge will be transferred to the integrator. So do the stuck-short S_2, stuck-open S_2, the stuck-short S_3, and stuck-open S_3. These are equivalent faults whose faulty SFG models are the same as that of the delayed SC branch with a zero C. Similarly, the circuit analysis results show the delayed SC branch with a stuck-short S_1 has a faulty SFG model equivalent to that of a purely capacitive branch with the same capacitance C.

The fault effect of the stuck-short S_4 in a delayed SC branch is derived as follows. When ϕ_1 is active, the inverting input node of the OPAMP is V_{OS} according to the virtual short property. As a result, the turn-on switch S_3 has a voltage drop of V_{OS} which induces a constant current flowing through it. Since the integrator has a very large input capacitance according to the Miller theory, most of the current is drawn from the OPAMP rather than from the delayed SC branch. The current will change the stored charges in the feedback capacitor C_{fb} by an amount of $V_{OS}T_1/R_{\text{on}}C_{fb}$, where R_{on} and $T1$ represent the on-resistance of the switch S_3 and the active period of ϕ_1, respectively. Meanwhile, the capacitor C samples a voltage difference of $V_i - V_{OS}$. When ϕ_2 is active, the stored charges in C are transferred to C_{fb}. By the charge conservation principle, we have

$$V_o(z) = \frac{Cz^{-1}V_i(z) - C_{\text{on}}V_{OS}}{C_{fb}(\alpha - \beta z^{-1})} \tag{12}$$

where C_{on} is defined as $\equiv T_1/R_{\text{on}}$. Equation (12) indicates the stuck-short S_4 can be considered as a fault-free delayed SC branch but introducing a different offset.

Most stuck faults of the switches on the delay-free SC branch have similar fault effects to that of the delayed SC branch. The only exceptions are the stuck-open S_2 and the stuck-open S_3. Detailed analyses show these faults turn the faulty delay-free SC branch into a purely capacitive one whose capacitance is C.

Table III lists the catastrophic faults of the switches and the faulty SFG models of the two kinds of single-ended SC branches. For the STF parts, the catastrophic faults of the switches result in either a zero SFG or an SFG of a purely capacitive branch. For the OTG parts, the faults lead to either a zero OTG or an OTG of $-C_{\text{on}}$. More generalized faulty SFG models of the faulty single-ended SC branches are expressed in the following with the help of the defined catastrophic fault activators.

The STF, $STF^Z(z)$, and the OTG, OTG^Z, of the faulty delayed SC branch are defined as

$$STF^Z(z) = -F_C C + (1 - F_0)Cz^{-1} \tag{13}$$

and

$$OTG^Z = (1 - F_0)C - F_4(C_{\text{on}} + C). \tag{14}$$

The operand F_0 represents the catastrophic fault activator of the equivalent stuck faults of a delayed SC branch that result in a zero STF. Meanwhile, F_C is the catastrophic fault activator of the equivalent stuck faults turning the delayed SC branch into a purely capacitive one. F_4 is the catastrophic fault activator of the stuck-short S_4 of the delayed SC branch. The values of the catastrophic fault activators are either one if the faults are excited, or zero when the faults are not activated.

Similarly, the STF and the OTG models of the faulty delay-free SC branch can be written as

$$STF^R(z) = -C(1 - F_0) + F_C Cz^{-1} \tag{15}$$

and

$$OTG^R = (1 - F_0 - F_C')C - F_4(C_{\text{on}} + C) \tag{16}$$

where F_0, F_C', F_C, and F_4 are the catastrophic fault activators of the faulty delay-free SC branch.

The overall IOR of the faulty CUT can be derived from the same SFG shown in Fig. 3 but with the faulty STF and OTG models expressed by (13)–(16).

It is worthy to note that the faulty STF and OTG models can cover the cases that multiple catastrophic faults occur on the same SC branch. For instance, if both stuck-open S_1 and stuck-short S_2 occur in a delay-free SC branch, the faulty STF model is still zero. In addition, the equivalent faults of $F_C = 1$ are masked by the equivalent faults of $F_0 = 1$. Take the case that both the stuck-open S_1 and the stuck-open S_2 occur simultaneously as an example, the resulted faulty STF is zero. As a consequence, it is not necessary to consider the faults excited by $F_C = 1$ when we examine the faults activated by $F_0 = 1$ of the same SC branch.

TABLE III
FAULTY SFG MODELS OF THE SINGLE-ENDED SC BRANCHES WITH CATASTROPHIC FAULTS

Block	Catastrophic Fault List	Catastrophic Fault Activators of the STF	Faulty $STF^{Z/R}(z)$	Catastrophic Fault Activators of the OTG	Faulty $OTG^{Z/R}$
Delayed SC branch Fig. 2(a)	S_1 stuck-open	$F_0 = 1$	0	$F_0 = 1$	0
	S_2 stuck-open	$F_0 = 1$	0	$F_0 = 1$	0
	S_3 stuck-open	$F_0 = 1$	0	$F_0 = 1$	0
	S_4 stuck-open	$F_0 = 1$	0	$F_0 = 1$	0
	S_1 stuck-short	$F_C = 1$	$-C(1 - z^{-1})$	As fault-free	C
	S_2 stuck-short	$F_0 = 1$	0	$F_0 = 1$	0
	S_3 stuck-short	$F_0 = 1$	0	$F_0 = 1$	0
	S_4 stuck-short	As fault-free	$\simeq Cz^{-1}$	$F_4 = 1$	$-C_{\text{on}}$
Delay-free SC branch Fig. 2(c)	S_1 stuck-open	$F_0 = 1$	0	$F_0 = 1$	0
	S_2 stuck-open	$F_C = 1$	$-C(1 - z^{-1})$	$F'_C = 1$	0
	S_3 stuck-open	$F_C = 1$	$-C(1 - z^{-1})$	$F'_C = 1$	0
	S_4 stuck-open	$F_0 = 1$	0	$F_0 = 1$	0
	S_1 stuck-short	$F_C = 1$	$-C(1 - z^{-1})$	As fault-free	C
	S_2 stuck-short	$F_0 = 1$	0	$F_0 = 1$	0
	S_3 stuck-short	$F_0 = 1$	0	$F_0 = 1$	0
	S_4 stuck-short	As fault-free	$\simeq -C$	$F_4 = 1$	$-C_{\text{on}}$

D. Faulty Signal Flow Graph Models of Fully-Differential Switched-Capacitor Circuits

Most SC circuits are fully-differential for better noise immunity and common-mode interference rejection. For the fully-differential circuits, the parametric faults result in different coefficients of the transfer function as they do in the single-ended implementation.

The fault effects of the stuck switches in the fully-differential SC circuits are somewhat different from their single-ended counterparts. In a fully-differential SC circuit, the primary output is composed of the two outputs of the two differential signal paths. Each path contributes a half of the fault-free primary output.

Generally speaking, an OPAMP has either a high common-mode rejection ratio or a zero output due to the failure of the common-mode feedback. The latter case is covered by the fatal parametric fault $A = 0$. Given the OPAMPs having fault-free CMRRs, a stuck switch only affects one of the two differential signal paths. As a result, the overall faulty transfer function of the CUT can be derived from the fault-free half circuit and the faulty half circuit.

Table IV lists the stuck faults and the corresponding faulty SFG models of the SC branches in fully differential implementation. We assume each fully-differential SC branch pair either is catastrophic-fault-free or has only one of the fault activators exercised at a time. The generalized STF and the OTG models of the faulty delayed SC branch can be expressed as

$$STF^{Z}(z) = -F_C C/2 + (1 - F_0/2)Cz^{-1} \tag{17}$$

and

$$OTG^{Z} = (1 - F_0/2)C - F_4(C_{\text{on}} + C)/2. \tag{18}$$

On the other hand, the STF and the OTG models of the faulty delay-free SC branch are

$$STF^{R}(z) = -C(1 - F_0/2) + F_C \frac{C}{2} z^{-1} \tag{19}$$

and

$$OTG^{R} = (1 - F_0/2 - F'_C/2)C - F_4(C_{\text{on}} + C)/2. \tag{20}$$

The faulty IOR of the fully-differential CUT including all the possible faults can be derived from the same SFG shown in Fig. 3 by replacing the SFG models with the corresponding faulty SFG models expressed by (17)–(20). The resulted STF of V_{O2} is

$$STF_{H2F}(z) = \frac{C_A C_G}{C_B C_D} \frac{NUM_{2F}(z)}{DEN_F(z)} \tag{21}$$

where

$$NUM_{2F}(z) = \frac{F_{CA}}{2} + \left(\frac{F_{0A} + F_{0G}}{2} - 1\right) z^{-1} + \frac{F_{CG}}{2} z^{-2} \tag{22}$$

and

$$\begin{aligned} DEN_F(z) = & \\ & \left[\beta_1\beta_2 + \left(-\frac{F_{CC}}{2}\right)\frac{C_A}{C_B}\frac{C_C}{C_D} + \frac{F_{CF}}{2}\beta_1\frac{C_F}{C_B}\right] z^{-2} \\ + & \left[\left(-\frac{F_{0C} + F_{0A}}{2} + 1\right)\frac{C_A}{C_B}\frac{C_C}{C_D}\right. \\ - & \left.\left(\frac{\alpha_1 F_{CF} - \beta_1 F_{0F}}{2} + \beta_1\right)\frac{C_F}{C_B} - \alpha_1\beta_2 - \alpha_2\beta_1\right] z^{-1} \\ - & \frac{F_{CA}}{2}\frac{C_A}{C_B}\frac{C_C}{C_D} + \left(\frac{1 - F_{0F}}{2}\right)\alpha_1\frac{C_F}{C_B} + \alpha_1\alpha_2. \end{aligned} \tag{23}$$

The additional subscripts of the fault activators in the above equations indicate in which SC branch the activated fault is. Similarly, we have

$$STF_{H1F}(z) = \frac{NUM_{1F}(z)}{DEN_F(z)} \tag{24}$$

where

$$\begin{aligned} NUM_{1F}(z) = & -\frac{F_{CG}}{2}\beta_2\frac{C_G}{C_D}z^{-2} \\ - & \left(\beta_2 - \frac{F_{CG} + F_{CF}}{2}\frac{C_F}{C_B} + \frac{\alpha_2 F_{CG} - \beta_2 F_{0G}}{2}\right)\frac{C_G}{C_D}z^{-1} \\ - & \left(1 - \frac{F_{0F} + F_{0G}}{2}\right)\frac{C_F}{C_B}\frac{C_G}{C_D} - \left(\alpha_2 - \frac{\alpha_2 F_{0G}}{2}\right)\frac{C_G}{C_D}. \end{aligned}$$

TABLE IV
FAULTY SFG MODELS OF THE SC BRANCHES IN FULLY DIFFERENTIAL IMPLEMENTATION

Block	Catastrophic Fault List	Catastrophic Fault Activators of the STF	Faulty $STF^{Z/R}(z)$	Catastrophic Fault Activators of the OTG	Faulty $OTG^{Z/R}$
Delayed SC branch Fig. 2(a)	S_1 stuck-open	$F_0 = 1$	$Cz^{-1}/2$	$F_0 = 1$	$C/2$
	S_2 stuck-open	$F_0 = 1$	$Cz^{-1}/2$	$F_0 = 1$	$C/2$
	S_3 stuck-open	$F_0 = 1$	$Cz^{-1}/2$	$F_0 = 1$	$C/2$
	S_4 stuck-open	$F_0 = 1$	$Cz^{-1}/2$	$F_0 = 1$	$C/2$
	S_1 stuck-short	$F_C = 1$	$-C(1/2 - z^{-1})$	As fault-free	C
	S_2 stuck-short	$F_0 = 1$	$Cz^{-1}/2$	$F_0 = 1$	$C/2$
	S_3 stuck-short	$F_0 = 1$	$Cz^{-1}/2$	$F_0 = 1$	$C/2$
	S_4 stuck-short	As fault-free	$\simeq Cz^{-1}$	$F_4 = 1$	$C/2 - C_{\text{on}}$
Delay-free SC branch Fig. 2(c)	S_1 stuck-open	$F_0 = 1$	$-C/2$	$F_0 = 1$	$C/2$
	S_2 stuck-open	$F_C = 1$	$-C(1 - z^{-1}/2)$	$F'_C = 1$	$C/2$
	S_3 stuck-open	$F_C = 1$	$-C(1 - z^{-1}/2)$	$F'_C = 1$	$C/2$
	S_4 stuck-open	$F_0 = 1$	$-C/2$	$F_0 = 1$	$C/2$
	S_1 stuck-short	$F_C = 1$	$-C(1 - z^{-1}/2)$	As fault-free	C
	S_2 stuck-short	$F_0 = 1$	$-C/2$	$F_0 = 1$	$C/2$
	S_3 stuck-short	$F_0 = 1$	$-C/2$	$F_0 = 1$	$C/2$
	S_4 stuck-short	As fault-free	$\simeq -C$	$F_4 = 1$	$C/2 - C_{\text{on}}$

The values of α_1, α_2, β_1, and β_2 follow (10), but the corresponding values in (11) are modified to be

$$\begin{aligned} C_{T1} &= (1 - F_{0C}/2)C_C + C_D + (1 - F_{0G}/2)C_G + C_{p1} \\ C_{T2} &= (1 - F_{0A}/2)C_A + C_B + (1 - F_{0F}/2)C_F + C_{p2} \\ C_{fb1} &= C_D \\ C_{fb2} &= C_B \\ C_{cb1} &= C_D + F_{CC}C_C/2 + F_{CG}C_G/2 + C_{p1} \\ C_{cb2} &= C_B + F_{CA}C_A/2 + F_{CF}C_F/2 + C_{p2}. \end{aligned} \tag{25}$$

Equations (21)–(25) will be used as the templates in Section IV for estimating the capacitor ratios of the example CUT with the test data.

IV. DESIGN OF EFFICIENT TESTS BASED ON THE SLB FAULT MODEL

Several state-of-the-art DfT methods and tools have been proposed for testing SC filters [20], [36]–[41]. In the following, we propose a test procedure and illustrate how to design efficient tests to test the example CUT shown in Fig. 1 based on the proposed SLB analog fault model.

Recall our test goals are to estimate as many parameters in the parameter set of the CUT as possible so as to achieve a high parametric fault coverage, and to check if any catastrophic fault occurs. Multitone tests well suit for these purposes. Adopting multitone tests has many advantages. First, they are standard tests in industry. Second, the statistical nature of multitone tests addresses the zero noise margin issue of analog circuits. Third, they reduce the required test time comparing with single-tone tests. Finally, the test results of multitone tests contain the noise and distortion of the CUT though they are not included in the proposed SLB fault model.

A. Proposed Test Procedure to Test for the Parameter Set

To simplify the discussion, let us consider the catastrophic and parametric faults that do not change the transfer function templates of the CUT first. The IOR of the CUT can be derived from (21). The result is

$$\begin{aligned} V_{O2}(z) &= \frac{-\frac{C_A}{C_B}\frac{C_G}{C_D}z^{-1}V_i(z)}{(1+\frac{C_F}{C_B}) - (2 - \frac{C_AC_C}{C_BC_D} + \frac{C_F}{C_B})z^{-1} + z^{-2} + E(z)} \\ &+ \frac{\frac{C_A}{C_B}(\frac{C_G}{C_D} + \frac{C_C}{C_D})}{\frac{C_C}{C_D}\frac{C_A}{C_B} + \frac{(1+\frac{C_{p1}}{C_D})\frac{C_F}{C_B}}{A_1}} V_{OS1} \\ &+ \frac{(1 + \frac{C_{p1}}{C_D})(\frac{C_A}{C_B} + \frac{C_F}{C_B})/A_1}{\frac{C_C}{C_D}\frac{C_A}{C_B} + \frac{(1+\frac{C_{p1}}{C_D})\frac{C_F}{C_B}}{A_1}} V_{OS2} \end{aligned} \tag{26}$$

where

$$\begin{aligned} E(z) &\simeq \frac{(1+\frac{C_F}{C_B})(1+\frac{C_C+C_G+C_{p1}}{C_D})}{A_1} + \frac{1+\frac{C_A+C_F+C_{p2}}{C_B}}{A_2} \\ &- \left(\frac{\frac{C_{p1}}{C_D} + 2\frac{C_C}{C_D} + 2\frac{C_G}{C_D} + 1 + \frac{C_C}{C_D}\frac{C_F}{C_B} + \frac{C_G}{C_D}\frac{C_F}{C_B}}{A_1}\right. \\ &+ \left.\frac{1 + \frac{C_{p2}}{C_B} + 2\frac{C_A}{C_B} + 2\frac{C_F}{C_B}}{A_2}\right) z^{-1} \\ &+ \left(\frac{\frac{C_C}{C_D} + \frac{C_G}{C_D}}{A_1} + \frac{\frac{C_A}{C_B} + \frac{C_F}{C_B}}{A_2}\right) z^{-2}. \end{aligned}$$

It is very difficult to directly resolve all the parameters included in (26) with the test results. Hence, we suggest a test procedure as the following to make the tests easier.

1) *Test for the OPGs of the OPAMPs:* Recall that fault-free OPAMPs have insignificant influences on the transfer functions of the CUT. In other words, the terms containing A_1 and A_2 in (26) vanish if A_1 and A_2 are high enough. For example, Fig. 4 illustrates the amplitude frequency responses of the CUT versus various OPGs by assuming the rest of the circuits are ideal. Low OPGs of the OPAMPs reduce the loop gains of the integrators. As a result, the closed-loop gains of the integrators become smaller. For the example CUT, an OPG of 40 dB is sufficient to fit in the design specification. An

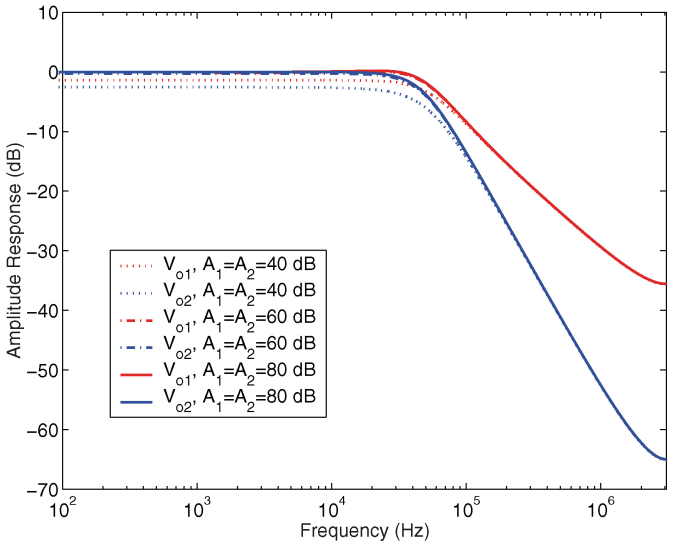

Fig. 4. Amplitude responses of the CUT versus OPAMPs' OPGs.

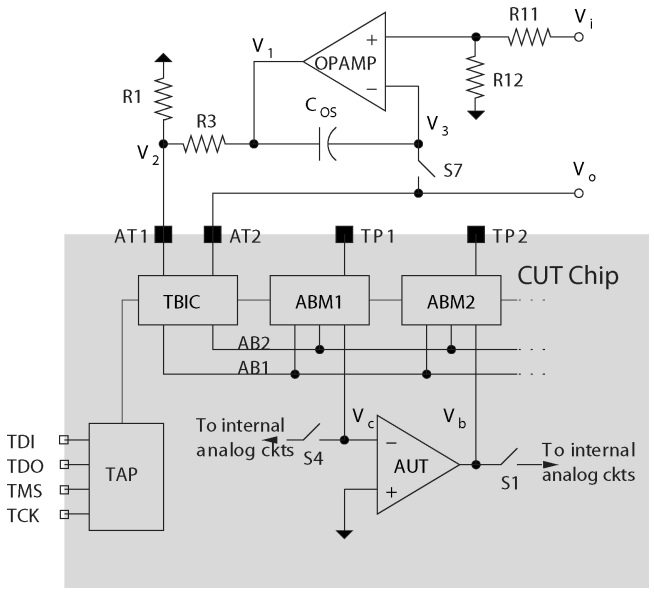

Fig. 5. Example test configuration for measuring the OPG of a single-ended AUT with IEEE 1149.4.

OPG less than 40 dB will result in a passband gain out of the design specification. This observation suggests that screening the passband gain of the CUT is a preliminary test for too low OPGs. If the tested passband gain is out of the design specification, then no further test is necessary since the CUT fails. Otherwise, the OPGs have to be tested in order to ease the estimation of the remaining parameters in the parameter set.

Note that it may not be necessary to test for how high the practical OPGs are. The reason is that designers usually add some design margins to the OPAMPs' OPGs in practice so as to enhance the harmonic distortion performance of the CUT [42]. Since our main goal of testing the OPAMP's OPG is to ensure the finite OPGs introducing insignificant errors so as to simplify the following capacitor ratio estimation procedure, testing for the real OPG values may not be necessary. For the example CUT, the frequency responses of the CUT with 60 dB OPGs are almost the same as those with 80 dB OPGs. Hence, we just want to make sure if the OPAMPs' OPGs of the example CUT are higher than 60 dB, even though their actual values may be 80 dB. If the test results show they are, then the error term $E(z)$ in (26) approximates to zero. Consequently, (26) can be simplified as

$$V_{O2}(z) = \frac{-\frac{C_A}{C_B}\frac{C_G}{C_D}z^{-1}V_i(z)}{(1+\frac{C_F}{C_B})-(2-\frac{C_AC_C}{C_BC_D}+\frac{C_F}{C_B})z^{-1}+z^{-2}} + (1+\frac{C_G}{C_C})V_{OS1} \quad (27)$$

which is much simpler to solve.

The test configuration proposed in [43] can be used to test the OPGs of the OPAMPs. The required auxiliary circuits can be built off-chip in conjunction with simple DfT circuits and/or with IEEE 1149.4 mixed-signal test bus in order to conduct the tests [2]. Fig. 5 shows an implementation example. The resistors $R2$, $R4$, $R5$, and $R10$, and the switch $S4$ of the original structure in [43] are saved because the CMOS OPAMPs in SC circuits have zero input bias currents and do not drive resistive loads. For every OPAMP under test (AUT) on the chip, we add two analog boundary modules (ABMs), two switches ($S1$ and $S4$) and two test pins. Note that the test pins (TP1 and TP2) are optional. We can leave them floating to save the area of the additional I/O pads. The test access port (TAP) controller accepts the test commands and controls the test bus interface circuit (TBIC) and the ABMs.

When testing the OPG of the AUT, the TAP controller configures the TBIC, ABM1, and ABM2 so that V_2, the analog test bus 1 ($AB1$), and V_c connect together. Meanwhile, the output of the AUT V_b passes through the ABM2, the analog test bus 2 ($AB2$), the TBIC, and reaches the $AT2$ pin. The ABMs of the other AUTs are isolated from the analog test buses ($AB1$ and $AB2$) and the AUT is isolated from the internal circuits by turning off the switches $S1$ and $S4$ in Fig. 5. The test first turns on $S7$ to store the offset voltage of the CUT on the capacitor C_{OS}. Then, $S7$ is turn off and the OPG is measured according to the amplitude ratio of V_o and V_i and the resistance ratios.

2) *Test for the Capacitor Ratios:* The next step is to test for the capacitor ratios. The CUT has four capacitor ratios under test including C_G/C_D, C_C/C_D, C_A/C_B, and C_F/C_B. The test problem is equivalent to solving (28) given k test frequencies ω_k and the corresponding test results t_k

$$\frac{C_F}{C_B}t_k(1-e^{-j\omega_kT}) + \frac{C_AC_G}{C_BC_D}e^{-j\omega_kT} + \frac{C_AC_C}{C_BC_D}t_ke^{-j\omega_kT} = -t_k(1-e^{-j\omega_kT})^2. \quad (28)$$

Mathematically, we cannot estimate all the four capacitor ratios according to (28) no matter how many t_k are given. It is because (28) has the form of three variables; hence, at most three variables can be found. Observing the DC term of the primary output in (27) does not help because V_{OS1} is unknown yet. It implies the parametric fault coverage never reaches 100% if the primary output is the only observable variable.

To enhance the fault coverage, we need additional observation points. The most suitable observation nodes in SC circuits are the outputs of the OPAMPs because adding test loads to them does not change the z-domain transfer functions of the CUT. Hence, we additionally adopt the test results of the intermediate output $V_{O1}(z)$ to estimate all the four capacitor ratios. Again, simple DfT circuits and/or IEEE 1149.4 can be used to observe $V_{O1}(z)$ with a very small on-chip hardware overhead. By (24), the IOR of $V_{O1}(z)$ approximates to

$$\begin{aligned} V_{O1}(z) &\simeq \frac{(-1-\frac{C_F}{C_B}+z^{-1})\frac{C_G}{C_D}V_i(z)}{(1+\frac{C_F}{C_B})-(2-\frac{C_AC_C}{C_BC_D}+\frac{C_F}{C_B})z^{-1}+z^{-2}} \\ &- (1+\frac{C_A}{C_F})V_{OS2} \end{aligned} \quad (29)$$

assuming that the OPAMPs have high enough OPGs. This equation provides additional independent relationships of the capacitor ratios

$$\begin{aligned} (\frac{C_F}{C_B}t_k+\frac{C_G}{C_D})(1-e^{-j\omega_kT}) &+ \frac{C_AC_C}{C_BC_D}t_ke^{-j\omega_kT}+\frac{C_GC_F}{C_DC_B} \\ &= -t_k(1-e^{-j\omega_kT})^2. \end{aligned} \quad (30)$$

By (28) and (30), all the capacitor ratios can be estimated, now.

3) *Test for the Offsets of the OPAMPs:* After obtaining all the capacitor ratios, the offsets of the two OPAMPs can be calculated according to the DC terms of the measured spectra, (27), and (29). We now acquire all the parameters in the parameter set. In other words, a 100% parametric fault coverage is achieved.

4) *Diagnosis After Test:* The final step of the test procedure is to derive the actual STF of the CUT according to the test data. The pass/fail decision is made based on if the frequency responses of the tested STF conform to the design specification.

By the proposed diagnosis after test method, we do not have to measure the amplitude responses at the other frequencies and still can ensure whether the frequency responses of the CUT complies with the design specification.

If one of F_{Cx} is excited, there may be no solution since the templates of the CUT's transfer functions become different. In such cases, (21) to (25) can be used as the templates to find the solutions by activating F_{Cx} one at a time.

A final remark on the proposed test procedure is that the multitone test data are not for making the final pass/fail decisions, but for preliminary checking if the CUT fails. Performing the diagnosis after test is a must for making the final pass/fail decision with the SLB fault model.

B. Design the Multitone Tests

Note that the test results t_k are complex numbers. Theoretically, the test results of a single-tone test of an output provide us two independent equations to estimate the capacitor ratios. In practice, the accuracy of the test equipment is limited and thus the selection of the stimulus tones is not straightforward. Sensitivity-based methods [20], [44] and statistical analysis approaches [23], [24] are very helpful to design the required stimulus tones.

An appealing way to conduct the tests is to check the design specification and to test for the parameters with the same tests. This can be achieved by conducting the multitone test whose stimuli consisting of a low-frequency tone, a tone at the passband edge, a tone at the corner frequency, and a tone at the stopband edge for the CUT.

The amplitude response of the low frequency tone directly shows the passband gain of the CUT. However, the phase response of the tone is too insignificant to be useful. Hence, the test results at the low-frequency tone usually provides us only one effective equation for solving the parameters.

The amplitude response of the tone at the passband edge in conjunction with that of the low-frequency can be used to preliminarily check the passband ripple. The passband-edge tone is an optional one for estimating the capacitor ratios because the test results of the passband-edge tone are highly dependent on those of the low-frequency tone for the fault-free CUT. If the CUT is faulty so that the corner frequency becomes lower, then the test results of this tone would provide extra data to estimate the capacitor ratios.

The frequency responses at the corner frequency are usually significantly different from those of the tones within passband. Hence, they are useful data for estimating the capacitor ratios.

Similarly, the tested frequency responses at the stopband edge can be used to preliminarily check the stop band attenuation. Since the results are very different from those of the other three tones, they are essential for estimating the capacitor ratios.

Depending on the capacitor number and design of the CUT, additional and/or different test tones may be necessary to solve the templates. An intuitive suggestion of selecting the stimulus frequencies is selecting the tones on the poles and zeros of the CUT's transfer function or in the transition band so that the test responses are significantly different.

C. Test Example

A test example of the CUT is given here to show the details. The first step is to derive the templates of the faulty transfer functions of the CUT using the proposed faulty SFG models. The procedure and results have been discussed and shown in Section III.

Next, we first test for the OPAMPs' OPGs following the proposed test procedure. Assume the tested gains are higher than 70 dB, then the approximations of (27) and (29) are valid. The two equations will be used as the templates to estimate the capacitor ratios.

Then, a four-tone test whose stimulus consists of 350 Hz, 20 kHz, 61 kHz, and 1 MHz tones is applied to the CUT. The four tones locate on a low frequency, the passband edge, the nominal pole of the CUT, and the stop band according to the discussion in Section IV-B.

Figs. 6 and 7 show the example four-tone test results. The blank area of Fig. 6 highlights the design window of the CUT. It is interesting to note that the amplitude responses of the internal output, V_{O1}, conventionally do not have design specification because it is not accessible. If it does, the results shown in Fig. 7 can be used to test it, too.

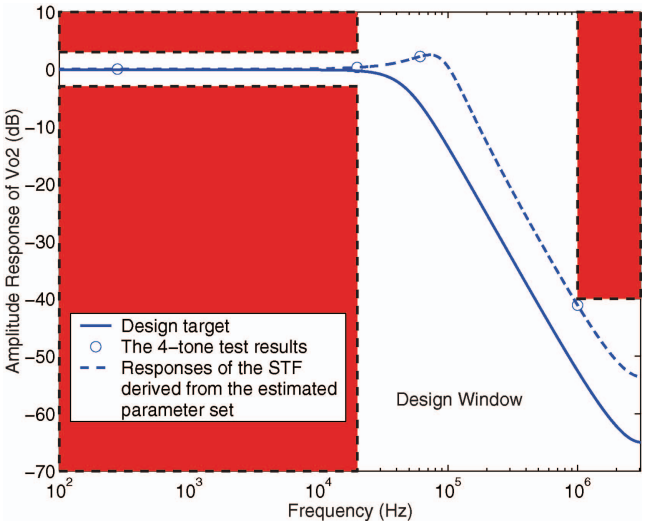

Fig. 6. Example test results of the primary output of the CUT.

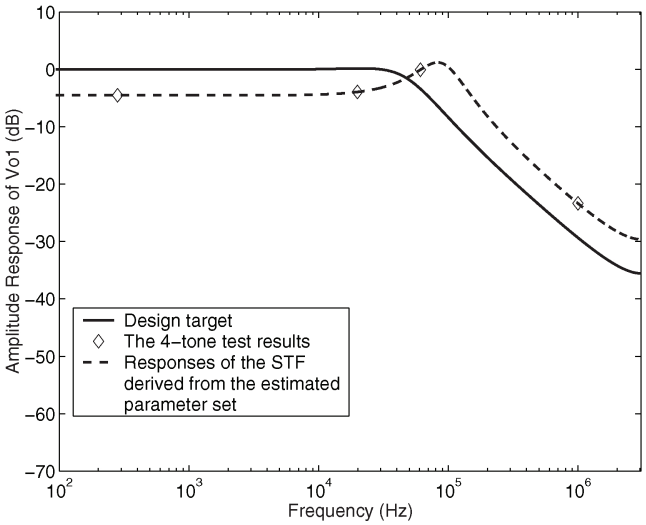

Fig. 7. Example test results of the internal output of the CUT.

Fig. 6 indicates the amplitude responses of the primary output V_{O2} of the four tones are all within the design window. It is worthy to note that a CUT passing the four-tone test does not need to be fault-free. The frequency responses of the four tones are preliminary checks only. If any one of them does not comply with the design specification, then the CUT certainly fails. If they do, we still have to proceed the following steps before making the final pass/fail decision.

The final steps are to estimate all the capacitor ratios, to find the offsets of the OPAMPs, and to check the frequency responses of the derived transfer function with the design specification. By using the test results of both outputs of the CUT, (28), and (30), the estimated capacitor ratios are listed in Table V. Based on the results of Table V and the DC terms of the output spectra of the four-tone test, the offsets of the OPAMPs are derived. A too large offset is a substantial signature for indicating a weak OPAMP and thus it is worthy to test for.

Finally, the amplitude responses of the CUT are calculated according to the estimated parameters and plotted in Fig. 6.

TABLE V
ESTIMATED CAPACITOR RATIOS OF THE CUT ACCORDING TO THE 4-TONE TEST RESULTS

Parameters	Design Targets	Estimated Values
C_A	$0.0701C_B$	$0.1323C_B$
C_C	$0.0333C_D$	$0.0654C_D$
C_F	$0.0701C_B$	$0.0778C_B$
C_G	$0.0333C_D$	$0.0659C_D$
A_1	80 dB	>70 dB
A_2	80 dB	>70 dB

The example CUT passes the test according to the plots. Note that the estimated C_A and C_C are twice as large as their design targets. Such huge deviations may be considered as severe parametric faults by conventional parametric fault models. However, there is no reason to reject the CUT because the CUT's frequency responses are still within the design window. The information of Table V is also very useful for diagnosing a faulty CUT to find the root causes of the failure.

The proposed SLB fault model and test procedure can be used to test different kinds of SC filters such as high-pass filters, all-pass filters, and high-order filters as well. All we have to do are deriving the faulty templates of the CUT's transfer functions according to the proposed faulty SFG models, and designing the tests to estimate all the design parameters on the templates by following the proposed test procedure.

D. Distortion and Noise

Although the proposed fault model does not include the distortion and noise of the CUT, the test results inherently present their values because multitone tests are standard tests for them in the industry. This is another advantage of conducting multitone tests to detect the faults.

Note that the presence of the harmonic distortions due to moderate nonlinearity of the CUT does not affect the resolved results of the capacitor ratios. It is because the harmonic distortions generated by the CUT would affect the stimulus responses only if the harmonic tones and the other stimuli locate on the same frequencies. A simple way to avoid this issue is choosing the stimulus frequencies so that no stimulus tone locates on the multiples of the others. Similarly, the noise may be an issue if and only if the noise significantly deteriorates the test responses on the stimulus frequencies. The noise issue can be addressed by observing a longer period of the CUT's responses. In fact, doubling the observation period reduces the power spectral densities of the noise on the stimulus frequencies by 3 dB.

V. CONCLUSION

We proposed the SLB analog fault model for linear SC circuits. The fault model partitions the CUT into functional macros, including the OPAMPs, the capacitors, and the switches. Each macro has specified design parameters from the design's points of view. These design parameters constitute the parameter set and determine the transfer function of the CUT. A CUT is defined to be faulty if the tested parameter set results in transfer functions whose frequency responses are

out of the design specification. Different from conventional single fault assumption, the SLB fault model covers concurrent multiple parametric faults and catastrophic faults. We also proposed a test procedure to test for all the design parameters in the parameter set. The test procedure conducts diagnosis after test instead of fault simulations before test to address the impractically long fault simulation time issue. An SC low-pass biquad filter was adopted as an example to demonstrate the effectiveness of the SLB fault model and the proposed test procedure. The multitone test results acquired during the proposed test procedure also reveal the distortion and noise performance of the CUT though the SLB fault model does not include them. Extending the fault model to include the timing related faults would be an interesting topic for future research.

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Hao-Chiao Hong (S'98–M'04) received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Tsing-Hua University, Hsinchu, Taiwan, in 1990, 1992, and 2003, respectively.

From 1997 to 2001, he was with Taiwan Semiconductor Manufacturing Company, Hsinchu, where he developed mixed-signal IPs for customers and process vehicles. He joined Intellectual Property Library Company, Hsinchu, as a Senior Manager with the Analog IP Department in August 2001. Since February 2004, he has been with National Chiao Tung University, Hsinchu, where he is currently an Associate Professor with the Department of Electrical Engineering. His main research interests include the design-for-testability, built-in self-test, and calibration techniques for mixed-signal systems and high performance mixed-signal circuit design.

Dr. Hong received the Best Paper Award from the 2009 IEEE International Symposium on Very Large Scale Integration (VLSI) Design, Automation and Test. He served as the Executive Secretary of the Mixed-Signal and RF Consortium of the Ministry of Education, Taiwan, from 2006 to 2008, and the Executive Secretary of the Heterogeneous Integration Consortium of the Ministry of Education, Taiwan, from 2008 to 2009. He has also served as the Program Chair of the Fifth VLSI Test Technology Workshop in 2011. He is a Life Member of the Taiwan IC Design Association and of the VLSI Test Technology Forum, Taiwan.