A 2-D Analytic Model for the Threshold-Voltage of Fully Depleted Short Gate-Length Si-SOI MESFET's

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Abstract— **A two-zone Green's function solution method is proposed to analytically model the potential distribution in the silicon film of fully depleted SOI MESFET's, in which the exact solution of 2-D Poisson's equation is obtained by using the appropriate boundary conditions. From the derived analytic 2-D potential distribution, the bottom potential in the active silicon film is used to analyze the drain-induced barrier lowering effect and the threshold voltage is defined in terms of minimum channel potential barrier. The results of the developed analytic threshold-voltage model are compared with those of 2-D numerical simulation, and good agreements are obtained for the gate length down to 0.1 μm with wide ranges of structure parameters and bias conditions.**

NOMENCLATURE

$\epsilon_{si}(\epsilon_{ox})$ Dielectric permittivity of Si (SiO_2).

L_g Gate length of the SOI MESFET.

$t_{si}(t_{ob})$ Thickness of silicon film (buried oxide).

k_m Eigenvalue for x-direction, $k_m = m\pi/L_g$.

k_n^i Eigenvalue for y-direction in region $i(i = \text{I, II})$, $k_n^I = \frac{(n-\frac{1}{2})\pi}{t_{si}}$, $k_n^{II} = \frac{(n-\frac{1}{2})\pi}{t_{ob}}$. Region I is silicon film and region II is buried oxide.

N_D The doping concentration in the silicon film.

V_{bi} Built-in potential of the source(drain)/channel high-low ($n^+ - n$) junction.

ϕ_{Bn} Barrier height of the gate metal-semiconductor contact.

ϕ_{bi} Built-in potential of the gate Schottky barrier, $\phi_{bi} = \phi_{Bn} - V_n$; V_n is the potential difference between the conduction band and the Fermi level of silicon film.

$V_{gs}(V_{ds})$ Gate-source (drain-source) voltage.

V_{BS} Oxide substrate-source voltage.

V_{FB} Flatband voltage of the substrate oxide

V_T Threshold voltage of the SOI MESFET.

$\Psi_{\min}$ The bottom potential minimum of the silicon film.

$x_{\min}$ The position of the bottom potential minimum.

D_s^m The Fourier coefficient of the electric displacement at the Si-SiO_2 interface. $D_s^m = \frac{2}{L_g}\int_0^{L_g} D_s(x') \sin k_m x'\, dx'$. D_s is the normal electric displacement.

$A_n^s(A_n^d)$ Fourier coefficient of boundary potential at the source (drain) side in silicon film. $A_n^s = \frac{2}{t_{si}}\int_0^{t_{si}} \Psi_I(0, y') \cos k_n^I y'\, dy'$, $A_n^d = \frac{2}{t_{si}}\int_0^{t_{si}} \Psi_I(L_g, y') \cos k_n^I y'\, dy'$.

$B_n^s(B_n^d)$ Fourier coefficient of boundary potential at the source (drain) side in buried oxide. $B_n^s = \frac{2}{t_{ob}}\int_0^{t_{ob}} \Psi_{II}(0, y') \cos k_n^{II} y'\, dy'$, $B_n^d = \frac{2}{t_{ob}}\int_0^{t_{ob}} \Psi_{II}(Lg, y') \cos k_n^{II} y'\, dy'$.

Q_B^m The Fourier coefficient of the channel charge density in silicon film. $Q_B^m = \frac{2}{L_g}\int_0^{L_g} qN_D \sin k_m x'\, dx'$.

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I. INTRODUCTION

As MOS devices shrink to deep submicrometer regime, the gate-oxide thickness becomes one of the important scaling parameters, and thin-gate oxide of several tens angstroms or less will be required. However, the growth of high-quality and low-defect density thin-oxide layer will be a bottleneck for future CMOS ULSI technology. In general, some oxide-related reliability issues due to hot-carrier effects and radiation/plasma damages are inevitable for thinner oxide. In addition, tunneling will occur when thickness is scaled down below 40 Å. Therefore, there exists an inherent limit for MOSFET technology advancement. From this point of view, the Si-MESFET could be a replacement for MOSFET scaled to an utmost limit.

The metal-semiconductor field-effect transistor (MESFET) was first proposed by Mead in 1966 [1] and was eventually fabricated on the GaAs epitaxial layer [2]. The active n-GaAs layer was formed on the semi-insulating GaAs substrate either through ion implantation or by epitaxial growth. Owing to the intrinsically high mobility of GaAs material, the MESFET's are widely used in high-speed logic circuit and microwave amplifier. The absence of gate oxide makes the MESFET device naturally immune to oxide-related problems such as radiation/plasma damages and hot-carrier effects. Besides, the channel of MOSFET device is formed by the inversion layer at the gate oxide-silicon interface, thus carriers suffer from high normal fields and serious roughness scattering, leading to drastic reduction of effective mobility and transconductance. However, the channel of MESFET device is formed in the

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undepleted bulk region which is usually near the bottom of the active layer, thus carrier mobility is less degraded. This is one of the advantages for the MESFET devices against the MOSFET devices. Moreover, the built-in voltage across the channel to source (drain) high-low $(n^+ - n)$ junction of a MESFET device is about 0.2 V which is smaller than that of a MOSFET device (about 0.9 V). Therefore, the MESFET does not need to concern about the punch-through effect but it is a serious problem for deep submicrometer MOSFET. Since the gate of MESFET is a metal-semiconductor Schottky contact, the voltage swing is limited within a relatively small range, depending on the barrier height. Hence, the MESFET is a good candidate for low-power applications [3], [4].

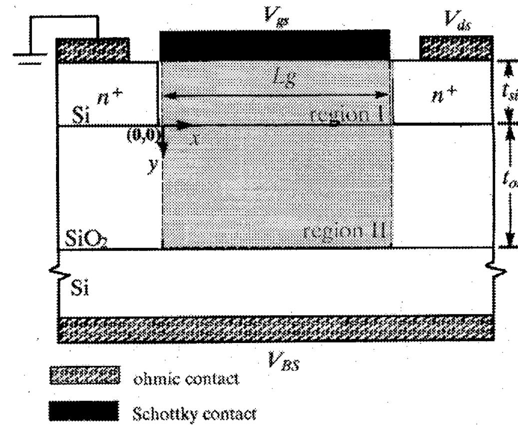
In this paper, the threshold-voltage model of fully depleted (normally off type or enhancement mode) SOI MESFET's is analytically developed. The exact solutions of 2-D Poisson's equations in both silicon film and buried oxide are solved by the Green's function solution technique without additional assumptions. In Section II, the boundary conditions are described and the Green's function solution method is discussed in detail. In Section III, the derived 2-D potential distribution is verified by 2-D numerical analysis and further applied to analyze the drain-induced barrier lowering effect and the threshold voltage for wide ranges of structure parameters and bias conditions. The results of the developed analytic threshold-voltage model are compared with those of 2-D numerical simulation, and good agreements are obtained. The calculated results show that the SOI MESFET has smaller short gate-length effect under careful selection of device parameters and applied biases. At last, a concluding remark is given in Section IV.

II. Basic Analysis

The silicon MESFET fabricated on a SIMOX wafer is shown in Fig. 1, in which a two-zone Green's function solution method is used to solve the potential distribution in both silicon film and buried oxide. The coordinate system used in our mathematical analysis is indicated in Fig. 1. Since the Green's functions are determined according to the boundary conditions specified, we first discuss the boundary conditions and then the Green's function solution.

A. Boundary Conditions

We focus on a self-aligned fully depleted MESFET structure shown in Fig. 1. In region I (silicon film), the source/drain boundary conditions are represented by the built-in potential across the source/drain to active channel high-low $(n^+ - n)$ junctions as marked by (I-a) and (I-b) in Fig. 1. The gate is a Schottky barrier formed by a metal-semiconductor contact, so the top surface boundary condition is chosen as the Dirichlet type while the Neumann type is considered for the bottom surface boundary condition, as marked by (I-c) and (I-d) in Fig. 1. In region II (buried oxide region), the boundary potentials along the y-direction are assumed to vary linearly [5] as described by (II-a) and (II-b) in Fig. 1. The oxide bottom potential is related to the substrate bias voltage and flatband voltage of buried oxide as expressed by (II-d) in Fig. 1.



$$(I-a): \Psi_I(0,y) = V_{bi} \qquad (II-a): \Psi_{II}(0,y) = \frac{V_{BS} - V_{FB} - V_{bi}}{t_{ob}} \cdot y + V_{bi}$$

$$(I-b): \Psi_I(L_g,y) = V_{bi} + V_{ds} \qquad (II-b): \Psi_{II}(L_g,y) = \frac{V_{BS} - V_{FB} - V_{bi} - V_{ds}}{t_{ob}} \cdot y + V_{bi} + V_{ds}$$

$$(I-c): \Psi_I(x,-t_{si}) = V_{gs} - \phi_{bi} \qquad (II-c): \frac{\partial \Psi_{II}}{\partial y}\bigg|_{y=0^+} = -r\frac{D_s}{\epsilon_{ox}}$$

$$(I-d): \frac{\partial \Psi_I}{\partial y}\bigg|_{y=0^-} = -\frac{D_s}{\epsilon_{si}} \qquad (II-d): \Psi_{II}(x,t_{ob}) = V_{BS} - V_{FB}$$

Fig. 1. The basic structure of a self-aligned thin-film SOI MESFET.

From electrodynamics, it reveals clearly that the normal electric displacement must be continuous across the interface between different media except the existence of fixed interface charge density. Thus, we can specify the normal interface electric displacement as D_s as marked by (I-d) in Fig. 1, i.e.,

$$\epsilon_{si}E_{si} = \epsilon_{ox}E_{ox} + \sigma = D_s \tag{1}$$

where E is the normal electric field with the subscript denoting the material and σ is the fixed interface charge density. We see from (1) that the electric displacement in oxide side is changed by the fixed interface charge density. The latter half of (1) can be rewritten as

$$\epsilon_{ox}E_{ox} = rD_s \tag{2}$$

where an "effective ratio" r is introduced to consider the effect of fixed interface charge density. Thus, the interface boundary condition in region II is expressed as the Neumann type as marked by (II-c) in Fig. 1. Note that the normal electric displacement D_s can be solved by using the continuity of potentials at the silicon-oxide interface.

B. Green's Function Solution Technique

The Green's function solution method provides a formal solution procedure for partial differential equation subject to boundary conditions. Lin and Wu [6] first applied this method to analytically solve the 2-D potential distribution

of bulk MOSFET devices. Chin and Wu [7] applied this method to MESFET devices, and Guo and Wu [5] developed a multizone Green's function solution method to model thin-film SOI MOSFET devices. Furthermore, the discretized Green's function solution method had also been used to implement a 2-D numerical device simulator used in this paper [8].

The 2-D Poisson's equation for the SOI MESFET structure shown in Fig. 1 can be expressed by

$$\nabla^2\Psi(x, y) = \begin{cases} -\frac{\varrho(x,y)}{\epsilon_{si}} & -t_{si} < y < 0 \\ 0 & 0 < y < t_{ob} \end{cases} \quad (3)$$

where the x- and y-coordinates represent the length and depth directions, respectively. The analytic domain is confined in $0 < x < L_g$ and $-t_{si} < y < t_{ob}$. The exact solution of the 2-D Poisson's equation in this finite region subject to the boundary conditions discussed above can be obtained by means of Green's theorem and expressed as

$$\Psi(x, y) = \int\int \frac{\varrho(x', y')}{\epsilon} G(x, y; x', y')\, dx'\, dy' + \int G(x, y; x', y') \frac{\partial \Psi}{\partial n'}\, dS' - \int \Psi(x', y') \frac{\partial G}{\partial n'}\, dS' \quad (4)$$

where $G(x, x'; y, y')$ is the Green's function satisfying $\nabla^2 G = -\delta(x - x')\delta(y - y')$; n' is the outward normal direction on the boundary surface.

According to the boundary condition types described above, the Green's functions can be determined and summarized as follows:

$$G_x^I(x, x'; y, y') = \frac{2}{Lg} \sum_{m=1}^{\infty} \sin k_m x \sin k_m x' \cdot \begin{cases} \frac{\cosh k_m y' \sinh k_m (t_{si}+y)}{k_m \cosh k_m t_{si}} & y < y' \\ \frac{\cosh k_m y \sinh k_m (t_{si}+y')}{k_m \cosh k_m t_{si}} & y' < y \end{cases} \quad (5a)$$

$$G_x^{II}(x, x'; y, y') = \frac{2}{Lg} \sum_{m=1}^{\infty} \sin k_m x \sin k_m x' \cdot \begin{cases} \frac{\cosh k_m y' \sinh k_m (t_{ob}-y')}{k_m \cosh k_m t_{ob}} & y < y' \\ \frac{\cosh k_m y \sinh k_m (t_{ob}-y)}{k_m \cosh k_m t_{ob}} & y' < y \end{cases} \quad (5b)$$

$$G_y^i(x, x'; y, y') = \frac{2}{t_i} \sum_{n=1}^{\infty} \cos k_n^i y \cos k_n^i y' \cdot \begin{cases} \frac{\sinh k_n^i x \sinh k_n^i (L_g-x')}{k_n^i \sinh k_n^i L_g} & x < x' \\ \frac{\sinh k_n^i x' \sinh k_n^i (L_g-x)}{k_n^i \sinh k_n^i L_g} & x' < x \end{cases} \quad (5c)$$

where i denotes the region concerned, i.e., $i = I(II)$ for the region $I(II)$; $t_I = t_{si}$, $t_{II} = t_{ob}$; and k_m, k_n^I, and k_n^{II} are eigenvalues as given in the nomenclature. The term $G_x^i(G_y^i)$ denotes the Green's function used for the integral along the x- (y-) direction in the Region i. Substituting Green's functions (5) and boundary conditions into the Green's theorem (4), the general forms of the 2-D potential distribution in each region can be obtained as

Region I:

$$\begin{aligned}\Psi_I(x, y) = &\sum_{m=1}^{\infty} \frac{Q_B^m}{\epsilon_{si}} \frac{\sin k_m x}{k_m^2} \left[1 - \frac{\cosh k_m y}{\cosh k_m t_{si}}\right] + \sum_{n=1}^{\infty} \frac{\cos k_n^I y}{\sinh k_n^I L_g} \\ &\cdot [A_n^s \sinh k_n^I (L_g - x) + A_n^d \sinh k_n^I x] \\ &+ \sum_{m=odd}^{\infty} \frac{4(V_{gs} - \phi_{bi})}{m\pi} \frac{\sin k_m x \cosh k_m y}{\cosh k_m t_{si}} \\ &- \sum_{m=1}^{\infty} \frac{D_s^m}{\epsilon_{si}} \frac{\sin k_m x \sinh k_m (t_{si} + y)}{k_m \cosh k_m t_{si}}. \end{aligned} \quad (6)$$

Region II:

$$\begin{aligned}\Psi_{II}(x, y) = &\sum_{n=1}^{\infty} \frac{\cos k_n^{II} y}{\sinh k_n^{II} L_g} \cdot [B_n^s \sinh k_n^{II} (L_g - x) + B_n^d \sinh k_n^{II} x] \\ &+ \sum_{m=1}^{\infty} \frac{r D_s^m}{\epsilon_{ox}} \frac{\sinh k_m (t_{ob} - y)}{k_m \cosh k_m t_{ob}} \\ &+ \sum_{m=odd}^{\infty} \frac{4(V_{BS} - V_{FB})}{m\pi} \frac{\sin k_m x \cosh k_m y}{\cosh k_m t_{ob}} \end{aligned} \quad (7)$$

where the coefficients A_n^s, A_n^d, B_n^s, B_n^d, D_s^m and Q_B^m are the Fourier coefficients described in the nomenclature.

The Fourier coefficients of interface normal displacement D_s could be solved by the continuity of the potentials in different materials along the interface at $y = 0$, i.e.,

$$\Psi_I(x, y = 0^-) = \Psi_{II}(x, y = 0^+). \quad (8)$$

Consequently, the result could be expressed as

$$\begin{aligned} D_s^m = \frac{1}{d^m} \Bigg[&\frac{Q_B^m}{\epsilon_{si} k_m^2 r} \left(1 - \frac{1}{\cosh k_m t_{si}}\right) + \frac{2(V_{gs} - \phi_{bi})}{m\pi} \frac{1 - (-1)^m}{\cosh k_m t_{si}} \\ &- \frac{2(V_{BS} - V_{FB})}{m\pi} \frac{1 - (-1)^m}{\cosh k_m t_{ob}} \\ &+ \sum_{n=1}^{\infty} \frac{2}{m\pi \left(1 + \frac{k_n^{I2}}{k_m^2}\right)} [A_n^s + (-1)^{m+1} A_n^d] \\ &- \sum_{n=1}^{\infty} \frac{2}{m\pi \left(1 + \frac{k_n^{II2}}{k_m^2}\right)} [B_n^s + (-1)^{m+1} B_n^d] \Bigg] \end{aligned} \quad (9)$$

where $d^m = \left(\frac{\tanh k_m t_{si}}{\epsilon_{si} k_m} + r \frac{\tanh k_m t_{ob}}{\epsilon_{ox} k_m}\right)$.

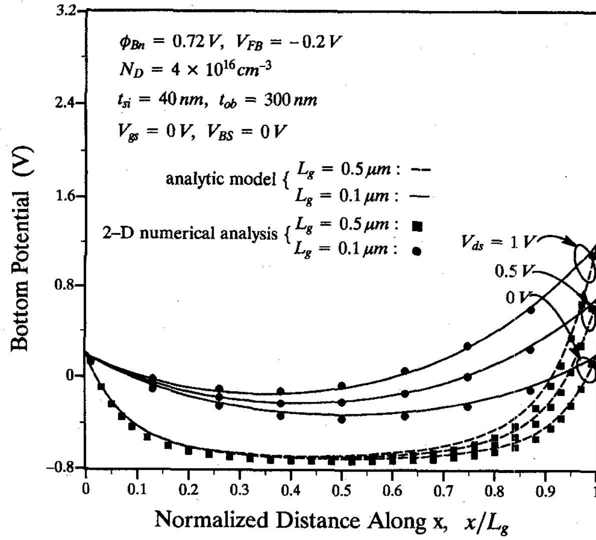


Fig. 2. The bottom potential distribution showing the drain-induced barrier lowering effect for $L_g = 0.5$ and 0.1 μm under different V_{ds}.

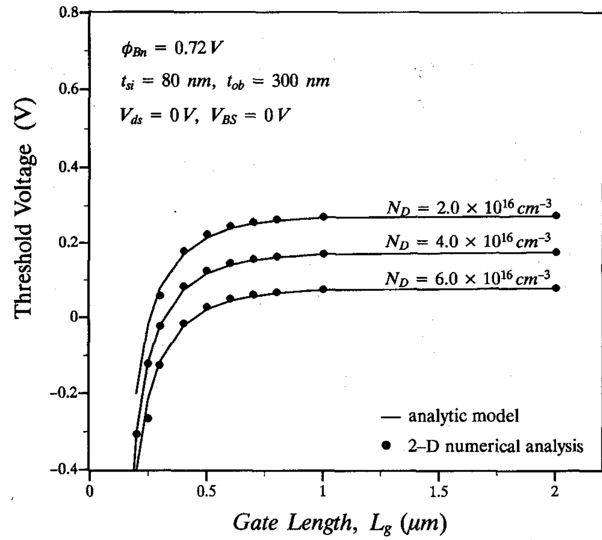


Fig. 4. The threshold voltage versus the gate length for different channel dopings.

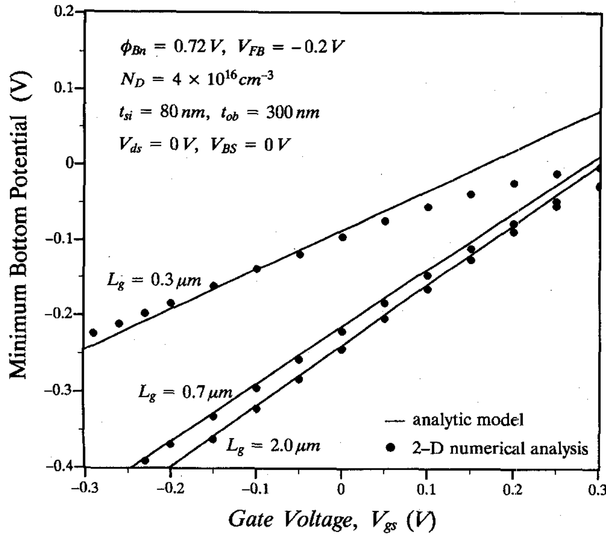


Fig. 3. The minimum bottom potential versus the gate bias for different gate lengths.

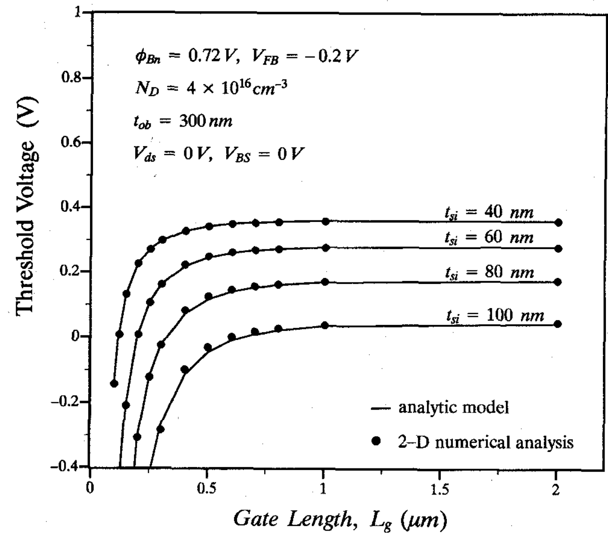


Fig. 5. The threshold voltage versus the gate length for different silicon-film thicknesses.

III. Applications and Verifications

A. Drain-Induced Barrier Lowering Effect

Since the SOI MESFET under consideration is normally off type (enhancement mode), the channel is fully depleted by the Schottky barrier potential at $V_{gs} = 0$. The bottom potential of silicon film can be used to monitor the subthreshold behavior of SOI MESFET's. From (6), we derive the bottom potential of silicon film as

$$\begin{aligned}\Psi_I(x, y=0) = &\sum_{m=1}^{\infty} \frac{Q_B^m}{\epsilon_{si}} \frac{\sin k_m x}{k_m^2}\left[1 - \frac{1}{\cosh k_m t_{si}}\right] \\ &+ \sum_{n=1}^{\infty} \frac{1}{\sinh k_n^I L_g} \\ &\cdot [A_n^s \sinh k_n^I (L_g - x) + A_n^d \sinh k_n^I x] \\ &+ \sum_{m=odd}^{\infty} \frac{4(V_{gs} - \phi_{bi})}{m\pi} \frac{\sin k_m x}{\cosh k_m t_{si}} \\ &- \sum_{m=1}^{\infty} \frac{D_s^m}{\epsilon_{si}} \frac{\sin k_m x \sinh k_m t_{si}}{k_m \cosh k_m t_{si}}. \end{aligned} \tag{10}$$

Note that computation of (10) is very fast for short gate-length devices; for example, only five terms in the Fourier series are needed for 0.3 μm device.

In order to verify the accuracy of the developed analytic model, the calculated results are compared with those computed by a 2-D numerical simulator [8]. Fig. 2 shows the calculated bottom potential as a function of the normalized

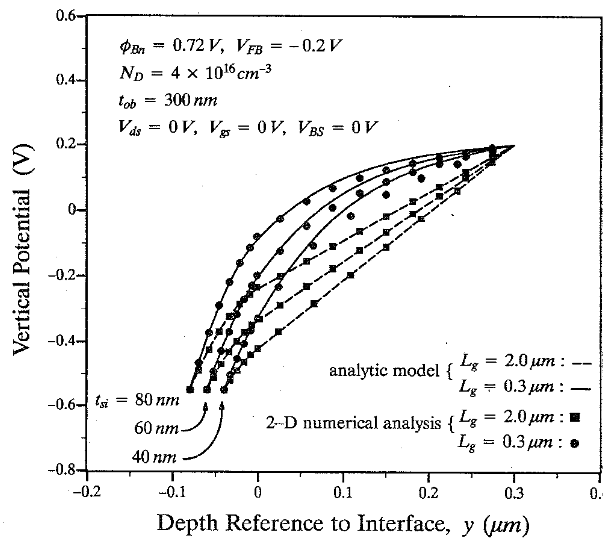


Fig. 6. The vertical potential distribution along depth-direction for $L_g = 2.0$ and 0.3 μm with silicon film thickness as a parameter.

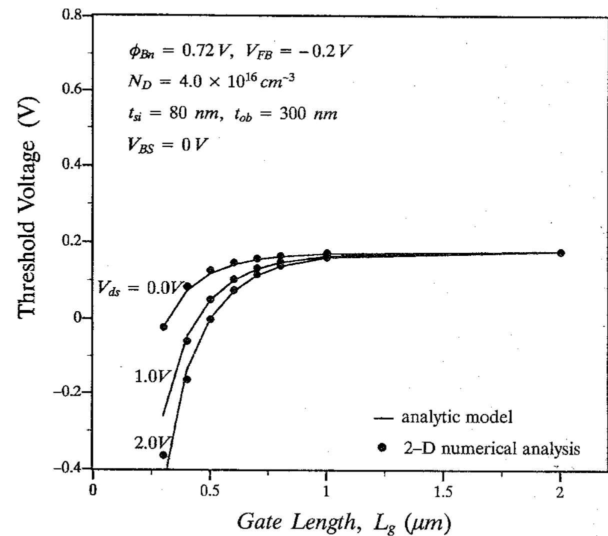


Fig. 7. The threshold voltage versus the gate length for different drain biases.

distance along the channel with the gate length as a normalization parameter for both long and short gate-length devices. It is clearly seen that good agreements between analytic model and 2-D numerical analysis are obtained for the gate length as short as 0.1 μm. As the gate length decreases, the minimum potential is elevated, hence the barrier is lowered. From Fig. 2, it can be seen that the drain-induced barrier lowering effect is much serious for short gate-length device. The channel barrier is substantially lowered by the applied drain bias for a short gate-length device, and the position of the minimum potential gradually shifts toward the source side. The doping level and the thickness of silicon film are chosen to turn the MESFET off for fully depleted MESFET operation. Note that the doping concentration in silicon film is considered to be uniform for simplicity.

B. Threshold Voltage

A conventional definition for the threshold voltage of a MESFET involves an abrupt transition between turn-on and turn-of operations. However, the drain current does not immediately decrease to zero for the gate bias below the threshold voltage but rather varies exponentially with the gate bias in the subthreshold region due to the formation of channel potential barrier. Fig. 3 shows the minimum bottom potential versus gate bias for different gate lengths. The discrepancies between comparisons at large gate bias indicate the turn-on operation of MESFET device, in which the analytic model for fully depleted operation is not valid. From the viewpoint of the potential barrier, we define the threshold voltage in terms of the channel barrier. From (10), the minimum bottom potential $\Psi_{\min}$ can be obtained by

$$\left|\frac{\partial \Psi(x,0)}{\partial x}\right|_{x=x_{\min}} = 0 \tag{11}$$

where $x_{\min}$ is the position of the minimum bottom potential and can be solved iteratively by

$$\begin{aligned}&\sum_{m=1}^{\infty}\frac{Q_B^m}{\epsilon_{si}}\frac{\cos k_m x_{\min}}{k_m}\left[1-\frac{1}{\cosh k_m t_{si}}\right]\\&\quad+\sum_{n=1}^{\infty}\frac{k_n^I}{\sinh k_n^I L_g}\\&\quad\cdot\left[-A_n^s\cosh k_n^I(L_g-x_{\min})+A_n^d\cosh k_n^I x_{\min}\right]\\&\quad+\sum_{m=odd}^{\infty}\frac{4(V_{gs}-\phi_{bi})}{L_g}\frac{\cos k_m x_{\min}}{\cosh k_m t_{si}}\\&\quad-\sum_{m=1}^{\infty}\frac{D_s^m}{\epsilon_{si}}\frac{\cos k_m x_{\min}\sinh k_m t_{si}}{\cosh k_m t_{si}}=0.\end{aligned} \tag{12}$$

Therefore, the minimum bottom potential can be written as

$$\begin{aligned}\Psi_{\min}=&\sum_{m=1}^{\infty}\frac{Q_B^m}{\epsilon_{si}}\frac{\sin k_m x_{\min}}{k_m^2}\left[1-\frac{1}{\cosh k_m t_{si}}\right]\\&+\sum_{n=1}^{\infty}\frac{1}{\sinh k_n^I L_g}\\&\cdot\left[A_n^s\sinh k_n^I(L_g-x_{\min})+A_n^d\sinh k_n^I x_{\min}\right]\\&+\sum_{m=odd}^{\infty}\frac{4(V_{gs}-\phi_{bi})}{m\pi}\frac{\sin k_m x_{\min}}{\cosh k_m t_{si}}\\&-\sum_{m=1}^{\infty}\frac{D_s^m}{\epsilon_{si}}\frac{\sin k_m x_{\min}\sinh k_m t_{si}}{k_m\cosh k_m t_{si}},\end{aligned} \tag{13}$$

and the threshold-voltage is defined in terms of minimum channel barrier to be

$$\Psi_{\min} - V_{bi} = -0.3 \text{ V}. \tag{14}$$

Fig. 4 shows the threshold voltages versus the gate length for SOI MESFET's with the channel doping as a parameter and t_{si} = 80 nm, t_{ob} = 300 nm. It is shown that the threshold voltage of MESFET's is decreased as the channel

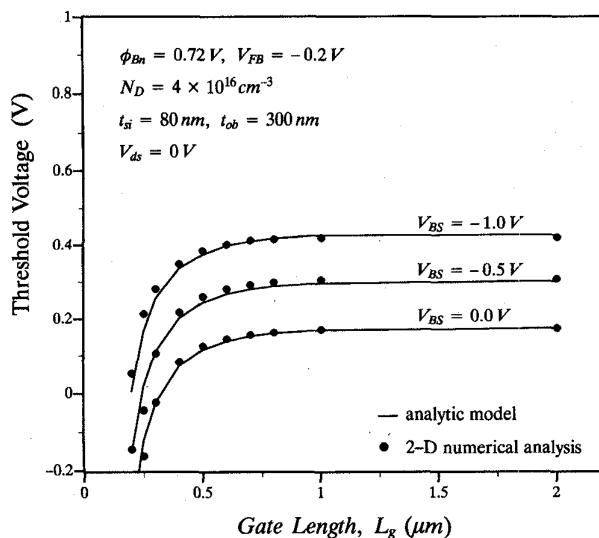


Fig. 8. The threshold voltage versus the gate length for different substrate biases.

doping increases. The calculated results using 2-D numerical analysis are also shown for comparisons and good agreements are obtained for the gate length as short as 0.3 μm. For even shorter devices, the threshold voltage becomes negative and the MESFET becomes the normally on device. For a fixed Schottky barrier height in a given gate metal, the channel doping is a key parameter for designing the threshold voltage and the drain current. Considering the voltage swing and low-power application of normally off type MESFET's, the lower threshold-voltage is preferred. Another parameter controlling the threshold voltage is silicon film thickness. The calculated results for different film thicknesses from 100 nm to 40 nm are shown in Fig. 5, in which the channel doping and the oxide thickness remain the same. It is observed that device with thinner silicon film has smaller threshold shift, thus exhibiting smaller short gate-length effect. The vertical potential distribution at the channel center ($x = L_g/2$) along the depth-direction with different silicon-film thicknesses is shown in Fig. 6 for L_g = 2.0 and 0.3 μm. For thinner silicon film device, more voltage is dropped across the buried oxide, and the silicon bottom potential keeps low, thus the channel barrier is increased. The silicon film thickness effect can be evaluated by the "specified aspect ratio," t_{si}/L_g. The decrease of silicon film thickness effectively increases the gate-length, so the short gate length effect is suppressed substantially.

In addition to the device structure parameters, the bias condition can also be used to control the threshold voltage of a SOI MESFET device. Fig. 7 shows the drain bias effect on the threshold voltage. The threshold-voltage shift for $V_{ds} = 2.0$ V is several times that for $V_{ds} = 0$ V. The detail of drain-induced barrier lowering has been interpreted previously. Fig. 8 shows the effects of substrate biases, in which the negative substrate bias suppresses the formation of channel conduction by pulling down the bottom potential. Comparing with the backgating effect of GaAs MESFET, the substrate bias of SOI MESFET is a controllable parameter which helps the modulation of threshold voltage in addition to structure parameters and makes the design of SOI MESFET devices more flexible.

IV. CONCLUSIONS

The exact solution of 2-D Poisson's equation for fully depleted SOI MESFET devices has been derived by means of a two-zone Green's function solution method with the appropriate boundary conditions. The calculated results are compared with 2-D numerical analysis and good agreements are obtained. This indicates that the assumptions of constant source (drain) potential and linear potential at oxide edges are reasonable for thin-film SOI MESFET's and no additional assumptions are needed. Based on the accurate 2-D potential distribution model, the bottom potential of silicon film is derived to monitor the subthreshold behavior of SOI MESFET's and the threshold voltage is defined in terms of channel barrier. It is shown that the results of developed analytic threshold-voltage model match well with those of 2-D numerical analysis for wide ranges of device structure parameters and bias conditions. It is clearly shown that the thinner silicon film is preferred due to smaller short gate-length effect and the heavy channel doping can be used to obtain lower threshold voltage for low-power applications. Furthermore, the substrate bias is useful for controlling the threshold voltage, thus making the design of a thin-film SOI MESFET more flexible. This accurate analytic model gives a fast and clear physical insight and provides a powerful tool for deep-submicrometer SOI MESFET's design.

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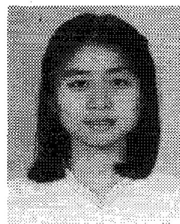

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