Low-Power Sub-Harmonic Direct-Conversion Receiver With Tunable RF LNA and Wideband LO Generator at U-NII Bands

Jin-Siang Syu, *Student Member, IEEE*, and Chinchun Meng, *Member, IEEE*

***Abstract*—A low-power tunable-band sub-harmonic direct-conversion receiver covering the whole Unlicensed National Information Infrastructure band is demonstrated using 0.18-μm CMOS technology. The RF band is selected by tuning varactors at the loads of the two-stage low-noise amplifier, while a wideband octet-phase generator is applied at the local oscillator (LO) port. The band tuning of both an *LC* tank and a transformer and the design of an optimal transformer turn ratio are fully discussed in this paper. Vertical-NPN bipolar junction transistors in a standard CMOS process are used at the mixer switching core for excellent $1/f$ noise performance. As a result, the receiver achieves a 48/50 voltage gain and 4.5/4.8-dB noise figure with a $1/f$ noise corner of 70 kHz when the RF band is tuned to 5.2/5.8 GHz, respectively. The dc current consumption of the RF front-end (including the LO buffer) is 8.5 mA at a 1.8-V supply.**

***Index Terms*—Direct-conversion receiver (DCR), low-noise amplifier (LNA), octet phase, phase shifter, sub-harmonic mixer (SHM), vertical-NPN (V-NPN).**

I. Introduction

THE low-noise amplifier (LNA) plays an important role in low-power, low-noise receiver design since the LNA must provide sufficient gain to suppress the noise figure (NF) of the whole receiver chain, but itself adds as little noise as possible. However, the design challenge increases dramatically under power constraints. In this paper, our application is focused on the Unlicensed National Information Infrastructure (U-NII) radio band, consisting of three frequency bands of 100 MHz each in the 5-GHz band: 5.15–5.25 GHz (for indoor use only), 5.25–5.35 GHz, and 5.725–5.825 GHz. Although the LNA has a low transconductance gain (g_m) due to its low dc current, the high load resistance [high quality factor (Q)] provides sufficient voltage gain for a better NF of the whole receiver at the cost of the RF bandwidth. In addition, a narrower RF bandwidth results in little received noise and interference from other channels or other communication systems. Thus, a tunable/switchable narrowband LNA has better gain/noise performance than a wideband LNA at a given power consumption. As a result, a two-stage LNA with tunable loads, including the first-stage *LC* tank and the second-stage transformer load, is employed in this study.

A direct-conversion receiver (DCR), i.e., zero-IF receiver, is well suited to low-power applications due to its simple circuit structure when compared to heterodyne or low-IF architectures. However, the dc offset, $1/f$ noise and IIP_2 problems are the primary issues for this system instead of the image and spurious problems of non-zero-IF architectures. A sub-harmonic mixer (SHM) is chosen for a low output dc offset due to the absence of local oscillator (LO) self-mixing [1]. In addition, MOS switching cores are directly replaced by vertical-NPN (V-NPN) bipolar-junction transistors (BJTs) available in a standard 0.18-μm CMOS process. The BJT devices have a $1/f$ noise corner of below 1 kHz [2], [3]. Further, an *LC* filter is applied at the common emitter node to greatly improve the IIP_2 performance [4]. Moreover, by using both resonance inductors (at mixer LO port and the *LC* filter) and sub-harmonic mixing structure, the proposed SHM overcomes the low cutoff frequency (f_T) of V-NPN BJTs and successfully operates at over three times the transistor f_T. On the other hand, a wideband LO octet-phase signal generator is chosen to avoid tuning both RF and LO bands simultaneously.

Since the RF LNA is a tunable-band structure while the mixer and the LO generator have wideband topologies, a tunable narrowband sub-harmonic direct-conversion receiver (SH-DCR) is proposed to cover the whole U-NII bands for the RF bandwidth around 200 MHz. Fig. 1 shows the block diagram of the proposed SH-DCR, including a two-stage tunable-band LNA, in-phase/quadrature (I/Q) SHMs with V-NPN BJT switching core, I/Q variable-gain amplifiers (VGAs) and a wideband LO octet-phase generator. The design of a single-in-differential-out two-stage tunable-band LNA is fully described in Section II. Section III presents the details of the down-conversion circuits, while Section IV reports the measurement results. Conclusions are given in Section V.

II. Two-Stage Tunable-Band LNA

The impedance of a parallel *LC* tank with lossy inductor $(sL + R_s)$ is

$$Z(s) = \frac{R_s + sL}{1 + sCR_s + s^2LC}. \tag{1}$$

Manuscript received November 15, 2011; accepted December 03, 2011. Date of publication January 23, 2012; date of current version March 02, 2012. This work was supported by the National Science Council of Taiwan under Contract NSC 98-2221-E-009-033-MY3, Contract NSC 99-2221-E-009-049-MY3, and Contract NSC 98-2218-E-009-008-MY3, and by the Ministry of Education (MoE) Aim for the Top University (ATU) Program under Contract 95W803.

The authors are with the Department of Electrical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: ccmeng@mail.nctu.edu.tw).

Digital Object Identifier 10.1109/TMTT.2011.2182657

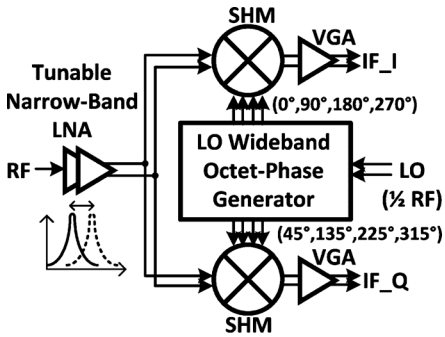


Fig. 1. Block diagram of the I/Q SH-DCR with a tunable narrowband LNA and a wideband LO generator using 0.18-μm CMOS technology.

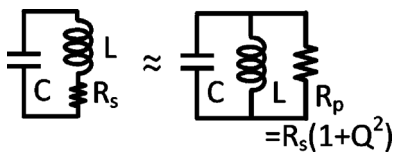


Fig. 2. Schematic of an *LC* tank with a lossy inductor.

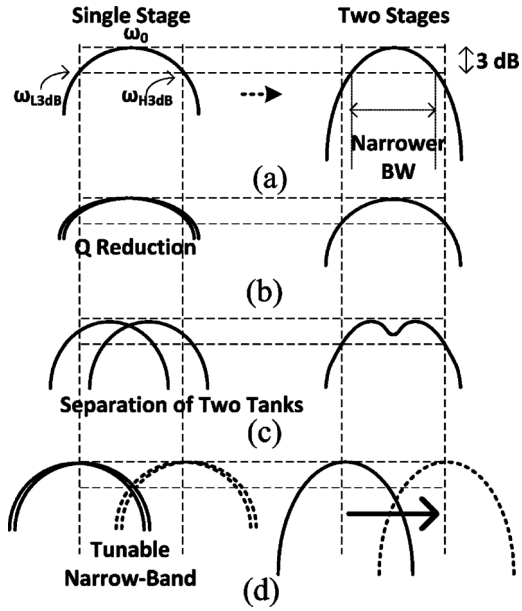


Fig. 3. (a) Frequency response of the single/two stage(s) of *LC* resonator(s). (b) Q reduction for each tank. (c) Wideband response with separation of tanks. (d) Tunable narrowband response.

Typically, the series resistance can be assumed as $R_s = (\omega/Q)L \equiv \alpha L$, where α is close to a constant, only relating to the geometrical shape (including width, spacing, and thickness). Thus,

$$|Z|_{\max} = \left[1 + \left(\frac{\omega_0}{\alpha}\right)^2\right] \cdot \alpha L = (1+Q^2)R_s = R_p \qquad (2)$$

when $(\omega_0^2 + \alpha^2)LC = 1$, as proven in Appendix A. This is why an *LC* tank with a lossy inductor is commonly approximated as an *RLC* parallel tank, as shown in Fig. 2.

Further, in Appendix A, a more general case, n stages of *RLC* tanks in cascade with the same Q, is considered for bandwidth. Thus, an m-dB bandwidth can be calculated as $k\omega_0/Q$, where $k = \sqrt{10^{m/10n} - 1}$, which is defined in Appendix A. If the target bandwidth boundaries are ω_L and ω_H, the required Q can be obtained by

$$Q = \frac{k\omega_0}{\Delta\omega} = k\frac{\sqrt{\omega_H\omega_L}}{\omega_H - \omega_L} \qquad (3)$$

where the center frequency is $\sqrt{\omega_H\omega_L}$, as also shown in Appendix A. Note that the 3-dB bandwidth of a single-stage *LC* tank is ω_0/Q by adopting $k = 1$.

By (3), to achieve a 3-dB bandwidth covering the whole U-NII band (5.15–5.825 GHz), the Q should be lower than 8.11. More strictly, if the gain flatness is required to be within 1 dB covering the whole band, the Q should be reduced to below 4.13. For a single-stage common-source (or cascode) LNA with *RLC* resonance load, the voltage gain can be simply expressed as $g_m \times R_P = g_m Q\sqrt{L/C}$ at the center frequency $\omega_0 = 1/\sqrt{LC}$. Generally speaking, the typical achievable Q value of an on-chip inductor is around 10. Thus, when compared to a wideband approach with $Q < 4.13$. Over 2.4 times the g_m (or extra 7.6-dB gain) is required to maintain the same voltage gain of the LNA or the IF VGA gain should be increased if the NF of the RF front-end is acceptable. Either way, the power consumption is increased.

On the other hand, if multiple tanks are in cascade and located at the same frequency, the greater number of stages in cascade results in a smaller k and thus a narrower bandwidth, as also described in Fig. 3(a). Either a Q value reduction or a separation of resonance frequencies can fulfill the original bandwidth requirement, as illustrated in Figs. 3(b) and (c), respectively. However, gain degrades when using either method.

For the requirements of low-power, high-gain, low-noise, and RF bandwidth of 5.15–5.825 GHz in this study, a two-stage cascode LNA with a tunable RF band is chosen. A two-stage LNA is required for a sufficient gain to suppress the NF of the following SHMs at a low dc current consumption. The center frequencies of the two stages are set to be the same and vary together, as described in Fig. 3(d). Thus, a higher gain is obtained when compared with the wideband solutions, especially in a low-power condition. Since the IF bandwidth is much lower than the RF bandwidth, the frequency response of the narrow RF tank is still nearly constant within the IF bandwidth (< 50 MHz).

The schematic of a two-stage cascode LNA is shown in Fig. 4. An *LC* tank is used at the load of the first stage and a transformer at the second stage. A series inductor L_g is sufficient for an input matching covering 5–6 GHz. Further, a gain tuning transistor (M_5) is in parallel with the cascode transistor in the second stage to reduce the gain when a large RF signal is applied. Note that the gain tuning approach using tunable M_5 and fixed-biased M_4 is a prototype. The cascode device can be broken into more branches with weighted sizes (not only M_4 and M_5), and thus a more gentle slope of the tuning curve can be achieved by digitally switching on/off the bias of each branch [5].

The frequency tuning capability of both an *LC* tank and a transformer load with a varactor are fully discussed as follows.

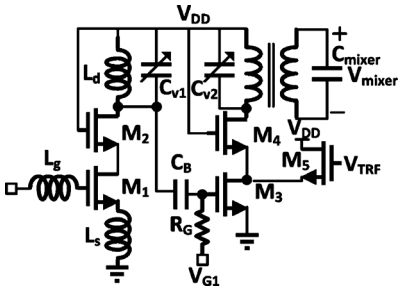


Fig. 4. Two-stage LNA with a tunable first-stage LC tank and a tunable second-stage transformer load, while a gain tuning transistor is applied in the second stage.

A. Frequency Tuning of an LC Tank

Assume the higher/lower RF bandwidth boundaries (ω_H/ω_L) are 5.825/5.15 GHz, respectively. Thus, the first-stage LC tank follows:

$$\begin{cases} L_d C_{\min} = \dfrac{1}{\omega_H^2} \\ L_d C_{\max} = \dfrac{1}{\omega_L^2}. \end{cases} \tag{4}$$

As a result,

$$\frac{C_{\max}}{C_{\min}} = \left(\frac{\omega_H}{\omega_L}\right)^2 = 1.28. \tag{5}$$

However, $C(V) = C_{\text{const}} + C_v(V)$ where C_{const} is a constant capacitance including device and substrate capacitances, and $C_V(V)$ is a capacitance of a varactor ranging from $C_{V,\min}$ to $C_{V,\max}$. Typically, in the CMOS process, a MOS varactor $C_V(V)$ operating in an accumulation mode has a tuning ratio $(C_{V\max}/C_{\min})$ of 2.5. Moreover, if the varactor capacitance ratio C_r is defined as $C_{V,\min}/C_{\text{const}}$,

$$\frac{C_{\max}}{C_{\min}} = \frac{C_{\text{const}} + C_{V,\max}}{C_{\text{const}} + C_{V,\min}} = \frac{1 + 2.5 \times C_r}{1 + C_r} > 1.28. \tag{6}$$

That is, C_r should be set above 0.23 to cover the whole U-NII band. The C_{const} can be changed by modifying the size of the cascode transistor, the following common-source transistor, and the dc blocking capacitance. Thus, in this study, C_{const} is tuned to 0.4 pF and $C_r = 0.3$ and $C_{\max}/C_{\min}$ are around 0.7/0.52 pF, respectively. Further,

$$L_d = \frac{1}{(\omega_H^2 C_{\min})} = \frac{1}{[\omega_H^2 (1 + C_r) C_{\text{const}}]}. \tag{7}$$

Thus, the calculated L_d is around 1.44 nH. Finally, the used inductor in the first-stage LNA has an inductance of 1.42 nH, Q of 11, and $f_{Q\max}/f_{\text{res}}$ of 13.5/30 GHz, respectively.

B. Frequency Tuning of a Transformer Load

On the other hand, the second-stage LNA has a transformer load to generate differential output signals. An n:1 transformer model is illustrated in Fig. 5(a) with the turn ratio $n = \sqrt{L_1/L_2}$, coupling coefficient $k = M/\sqrt{L_1 L_2}$, and

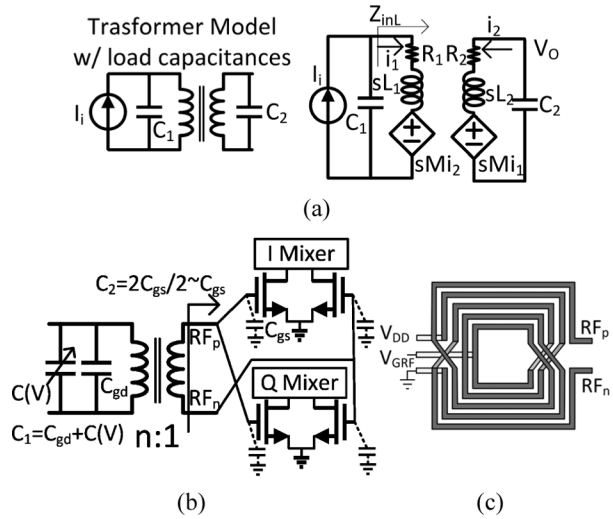


Fig. 5. (a) Transformer model with a capacitance load C_1/C_2 at the primary/secondary coil, respectively. (b) Schematic of the LNA transformer with an input varactor and output pure capacitance load. (c) Layout construction of the 2:3 transformer.

mutual inductance M. Similar to an inductor, the series resistance of each coil is assumed to be proportional to the series inductance. That is, $R_i = (\omega/Q_i)L_i \equiv \alpha_i L_i$, $i = 1, 2$, similar to the inductor model.

Here, we focus on the situation of a pure capacitive load, which is especially suitable for an active mixer load. C_1/C_2 consists of the loading capacitance $C_{\text{in}}/C_{\text{out}}$ and the intrinsic parasitic capacitance C_{p1}/C_{p2} of the transformer at each input/output node. The transimpedance gain (Z_T) is considered because the output current of the cascode LNA is fed to the transformer and then the differential output voltage is directly transferred to the transconductance (g_m) stage of the following active mixer, as indicated in Fig. 5(b).

Following the lumped model in Fig. 5(a), the Z_T can be expressed as

$$Z_T(s) = \frac{sM}{\left[\begin{array}{l}(1 + sR_1C_1 + s^2L_1C_1)(1 + sR_2C_2 + s^2L_2C_2) \\ -s^4M^2C_1C_2\end{array}\right]} \tag{8}$$

which is derived in Appendix B.

Fig. 6(a) shows the frequency response of Z_T in a normalized frequency condition. As shown in Fig. 6(a), Z_T usually has two peak frequencies $\omega_{\max L} = \omega_0/\sqrt{1+k}$ and $\omega_{\max H} = \omega_0/\sqrt{1-k}$, where $\omega_0 = 1/\sqrt{L_1C_1}$ when Q of the transformer is high. The mathematical derivation is also summarized in Appendix B. However, $\omega_{\max H}$ tends to be infinity for high coupling condition and is not suitable for real applications. Thus, $\omega_{\max L}$ is typically chosen. In addition, the optimal turn ratio $n_{\text{opt}} = \sqrt{CR} = \sqrt{C_2/C_1}$ is obtained after a thorough derivation in Appendix B if $\alpha_1 = \alpha_2 = \alpha_0$ (which is true for the two coils on the same layer with the same linewidth). Fig. 6(b) shows the Z_T at a target frequency with respect to $X = CR/n^2$ for different input/output loading capacitance. The peak gain occurs at $X = 1$, as predicted.

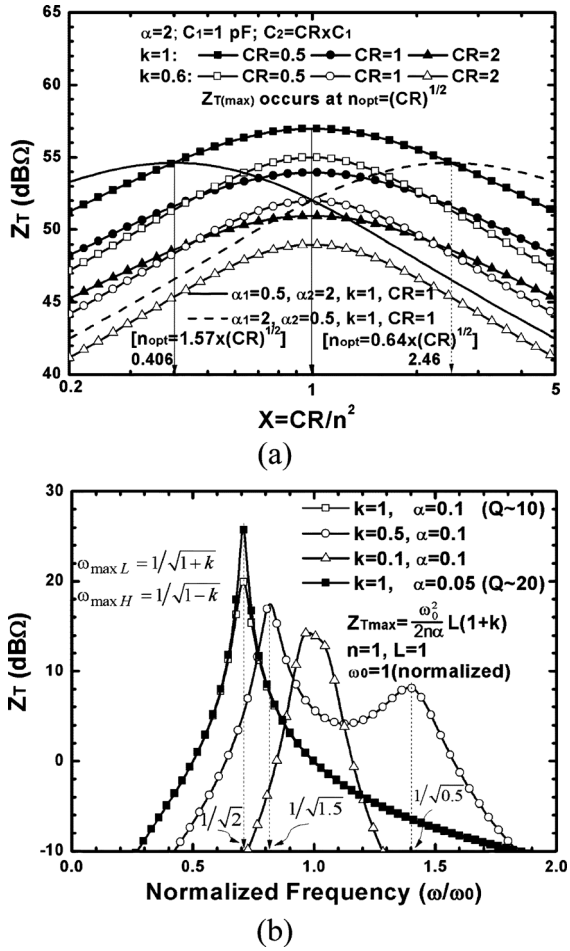


Fig. 6. (a) Transimpedance gain (Z_T) of a transformer as a function of frequency. (b) Z_T at a target frequency with respect to $X = n^2/CR$ for different input/output loading capacitance.

When $n = \sqrt{CR}$, i.e., $L_1C_1 = L_2C_2 = 1/\omega_0^2$, the peak gain $|Z_T(\omega_{\max L})|$ can be simplified as

$$|Z_T| = \frac{\omega^2 L_1}{2n\alpha_0}(1+k)^2 = Q\frac{\omega L_1}{2n}(1+k)^2 = \frac{\omega_0^2 L_1}{2n\alpha_0}(1+k). \quad (9)$$

The reason is also indicated in Appendix B. It is noteworthy that if $\alpha_1 \neq \alpha_2$, which is true especially for a stacked transformer using two layers, $n_{\rm opt}$ shifts. Fig. 6(b) also shows that $n_{\rm opt}$ increases if $\alpha_1 < \alpha_2$, and vice versa. However, the case of $\alpha_1 = \alpha_2$ is suitable for our study.

Further, if varactors are employed at both nodes, and $L_1C_{1(V)} = L_2C_{2(V)}$ is still fulfilled, then

$$\frac{\omega_H^2}{\omega_L^2} = \frac{C_{1,\max}}{C_{1,\min}} = \frac{C_{2,\max}}{C_{2,\min}} \quad (10)$$

which is the same as the result of a parallel LC tank because the peak frequency $\omega_{\rm pk}$ is proportional to tank resonance frequency $\omega_0(\omega_{\rm pk} = \omega_0/\sqrt{1+k})$.

On the other hand, if only C_1 can be tuned, assuming $L_2C_2 = 1/\omega_0^2$, yields

$$\frac{\omega_H^2}{\omega_L^2} = \left(\frac{C_{1,\max}}{C_{1,\min}}\right)^{1/2} \quad (11)$$

which is derived in Appendix C.

That is, the tuning capability of a transformer with only one varactor on either side is half of a parallel LC tank or a transformer with varactor loads at both sides. Thus, a higher C_r should be applied to cover the desired frequency range. As shown in Fig. 5(b), C_1 mainly consists of the varactor and the $C_{\rm gd}$ of the cascode device in the second-stage LNA. Besides, at the output stage, the differential capacitances of the transconductance stage of the mixers are in series, but I and Q mixers are in parallel. Therefore, the differential load capacitance C_2 is approximately equal to $C_{\rm gs}$ of a single transistor.

Similar to an LC tank, the decision of the varactor value can also be applied. Thus,

$$\frac{C_{1,\max}}{C_{1,\min}} = \frac{C_{1,\rm const} + C_{V1,\max}}{C_{1,\rm const} + C_{V1,\min}} = \frac{1 + 2.5 \times C_r}{1 + C_r} = 1.637. \quad (12)$$

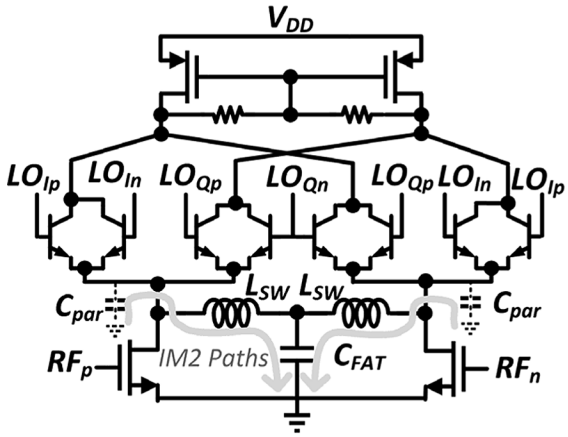
Thus, C_r should be larger than 0.417 and is set to 0.5 in this study. If $C_{1,\rm const}$ is set to 0.3 pF, $C_{1,\max}/C_{1,\min} = 1.05/0.45$ pF, respectively. $C_{1,\rm center} = (C_{1,\max} \times C_{1,\min})^{1/2} = 0.687$ pF, while $C_2 = C_{\rm gs} = 0.3$ pF. The best transformer turn ratio n is $(0.3/0.687)^{1/2} = 0.66 \approx 2/3$. Thus, a 2:3 planar single-to-differential transformer is chosen. The layout construction of the 2:3 transformer load is shown in Fig. 5(c), while the linewidth is 9 μm, line spacing is 2 μm, and the outer diameter is 190 μm.

III. I/Q Sub-Harmonic Downconverter

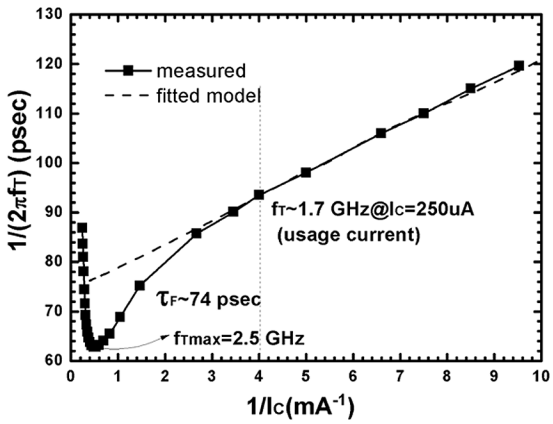
A. SHM

An SHM has better dc-offset output than a fundamental mixer inherently [1]. A top-LO SHM [6], [7] is applied because of a lower voltage headroom requirement and a better isolation when compared with a stacked-LO SHM at the cost of a larger LO power requirement. Additionally, parasitic V-NPN BJTs, obtained in a deep-n-well CMOS process without an extra mask [3], is applied at the mixer switching core to directly eliminate the $1/f$ noise problem, as shown in Fig. 7(a). Fig. 7(b) shows the $1/(2\pi f_T)$ as a function of $1/I_C$ of the measured data and simulated data using our fitted model with modified forward base transit time (TF) and the junction capacitance (CJC and CJE), while the dc model is provided by foundry. Besides, in this study, 0.25-mA dc current flows into one BJT transistor, and hence, the BJT only operates at around 1.7 GHz, as indicated in Fig. 7(b). That means a receiver covering U-NII bands (5.15–5.825 GHz) is rarely achievable originally. However, using both the sub-harmonic operation and differential resonance inductors, an SHM operated at three times the transistor f_T is achieved in this study. Four differential inductors are in parallel with the base nodes of the switching core of the I/Q mixers and the output nodes of the LO generator to reduce both the conversion loss of the switching operation and the LO loss of the LO generator simultaneously. The details about the LO loss reduction will be discussed in Section III-B.

On the other hand, self-mixing, transconductor nonlinearity, switching pair nonlinearity, and mismatch in load resistors are the main reasons for the $\rm IIP_2$ degradation in downconversion mixers [8]. Self-mixing of RF signals due to coupling into the LO port can be significantly reduced by means of layout concerns, e.g., metal lines carrying RF and LO signals should never



(a)



(b)

Fig. 7. (a) Top-LO sub-harmonic Gilbert mixer with V-NPN BJT in the switching core while an *LC* network is applied for an IM_2 improvement. (b) Measured $1/(2\pi f_T)$ versus $1/I_C$ of the V-NPN BJT used in the mixer core (emitter area $= 2 \times 2\ \mu\mathrm{m}^2$). The base transit time is around 74 ps.

cross each other, or should be kept orthogonal. Further, employing highly linear polysilicon resistors makes the effect from load resistor nonlinearity negligible. Device nonlinearity of RF transconductor generates the second-order inter-modulation distortion (IM_2) components. A perfectly matched switching stage upconverts the input differential baseband spectrum at mixer output. However, the RF IM_2 components leak into the IF output by the low-frequency gain of the switching pairs if mismatches in the switching stage devices are considered. In principle, low-frequency RF IM_2 components can be filtered out by ac coupling the switching stage. However, additional power consumption resulting from biasing the input stage and mixer core separately is not desirable in our low-power application.

In this study, an *LC* filter $(L_{\mathrm{SW}} - C_{\mathrm{FAT}} - L_{\mathrm{SW}})$ is applied to filter out the IM_2 current in RF transconductor [4], as shown in Fig. 7, since the shunt inductor L_{SW} has a relatively low impedance at low frequencies and the IM_2 current can be directly shorted to ground by the bypass capacitor (C_{FAT}) applied at the center-tapped node of the symmetric inductor. It is noteworthy that C_{FAT} should be large enough for an IIP_2 improvement. In this study, C_{FAT} is 15 pF. When compared to the

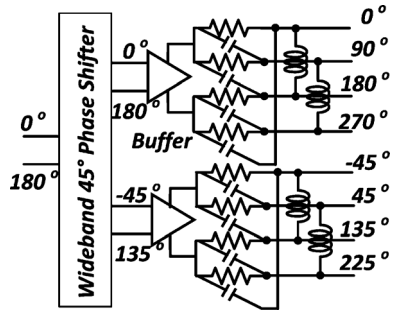


Fig. 8. Block diagram of an *LC* octet-phase generator including a wideband 45° phase shifter, cross-coupled buffer amplifiers, and single-stage PPF with resonance inductors.

tens of megahertz RF applications, the IIP_2 value drops dramatically due to the parasitic capacitance C_{par} at high frequencies [4]. The L_{SW} in the *LC* filter can also resonate out the parasitic C_{par}. Thus, both the high-frequency gain and the IIP_2 performance of the Gilbert mixer can be improved.

For a chip area concern, a 3-D symmetric inductor realization is used [9]. The symmetrical 3-D inductors (effectively six turns from metal 6 to metal 1) with 8-μm linewidth, 2-μm line spacing, and 70-μm outer diameter are applied at the *LC* filters in I/Q mixers and have the differential inductance of 2.4 nH and $Q = 3.6$ at around 5–6 GHz.

B. Wideband LO Octet-Phase Generator

The proposed wideband octet-phase signal generator used at the LO port of the SHM, shown in Fig. 8, consists of a differential-type wideband 45° phase shifter [1], [10], two differential buffer amplifiers, and two polyphase filters (PPFs) with symmetrical inductor loads.

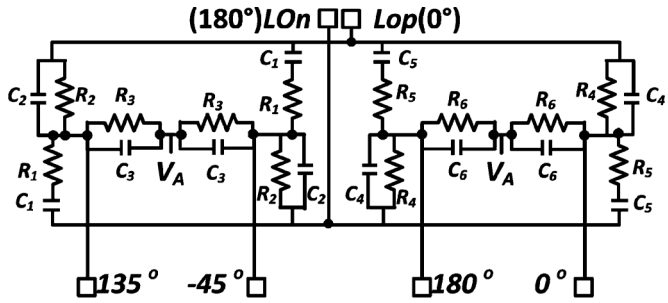
The LO amplitude/phase should be very accurate covering around 2.5–3 GHz (i.e., 2LO frequency of 5–6 GHz). A first-order *RC* phase shifter has perfect 45° phase shift only at a single frequency and a tunable version of the phase shifter using varactors is needed. However, it is difficult to tune both RF and LO parts of the narrowband structures in a precise way for practical use. Thus, a second-order *RC* phase shifter is employed to cover a given bandwidth without tuning. The schematic of the phase shifter is shown in Fig. 9(a) and the *RC* relations are summarized as follows:

$$\begin{cases} R_1C_1 = R_2C_2 = R_3C_3 = \dfrac{1}{(2\pi f_1)} \\ R_4C_4 = R_5C_5 = R_6C_6 = \dfrac{1}{(2\pi f_2)} \\ R_2 = abR_1, R_3 = bR_1 \\ R_4 = abR_5, R_6 = bR_5. \end{cases} \tag{13}$$

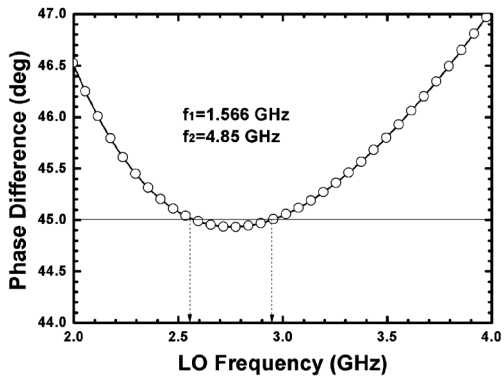
The output voltage of the phase shifter can be expressed as

$$V_{oi} = (-1)^i \frac{V}{a+1} \frac{1 - F_i^2 + jF_i(2-ab)}{1 - F_i^2 + jF_i\left(2 + \dfrac{ab}{a+1}\right)} \tag{14}$$

where $F_i = f/f_i$, $i = 1$ or 2.



(a)



(b)

Fig. 9. (a) Schematic of a differential-type wideband 45° phase shifter. (b) Phase difference of the phase shifter with respect to frequency.

To obtain balanced amplitudes of all nodes at all frequencies, $b = 4(a+1)/a^2$ should be chosen and the voltage loss can also be expressed as

$$V_{oi} = (-1)^i \frac{V}{a+1} \frac{1 - F_i^2 - jkF_i}{1 - F_i^2 + jkF_i} \tag{15}$$

where $k = 2 + 4/a$, $i = 1$ or 2.

As a result,

$$\begin{cases} |V_{o1}| = |V_{o2}| = \dfrac{V}{a+1} \\ \Delta\phi = \phi_2 - \phi_1 = \pi - 2\tan^{-1}\left(\dfrac{kF_2}{1-F_2^2}\right) \\ \qquad\quad +2\tan^{-1}\left(\dfrac{kF_1}{1-F_1^2}\right). \end{cases} \tag{16}$$

According to (16), the voltage loss only depends on the coefficient a, and is independent of frequency. A smaller a results in a lower loss; thus, $a = 1 (b = 8)$ is chosen in this study to achieve a voltage loss of 6 dB. Besides, the phase error varies as the two center frequencies f_1 and f_2. Thus, f_1/f_2 are set at 1.566/4.85 GHz, respectively, for the perfect 45° LO phase difference at 2.55 and 2.95 GHz, as shown in Fig. 9(b). Thus, ideal phase error below ±0.1° is achieved covering the LO frequency from 2.5 to 3 GHz.

The amplitude/phase relationships derived above hold true when the load impedance is infinity. When a PPF is cascaded after the phase shifter for quadrature signal generation, the low input impedance of the PPF results in a significant phase error. Conversely, if the resistance is set high (e.g., over kΩ), i.e., the capacitance of the PPF should be small because $\omega_{\rm LO} = 1/RC$, the voltage loss due to the output capacitance loadings is unacceptable [11]. As a result, an inter-stage buffer amplifier is inserted to provide a high load impedance for the phase shifter and a low source impedance for the following PPF. Parallel inductors resonate the capacitance including the loading mixer capacitances and PPF capacitance at $\omega_{\rm LO}$ to obtain a higher output impedance and reduce the PPF loss. Fig. 10 shows the schematic of the cross-coupled differential buffer amplifier [12]. The voltage gain is described as

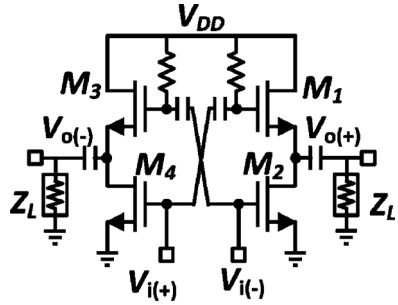


Fig. 10. Cross-coupled differential voltage buffer applied in the LO generator.

$$\begin{cases} v_{o(+)} = v_{i(+)} \dfrac{g_{m1} Z_L}{1 + g_{m1} Z_L} + v_{i(-)} \left[-g_{m2} \left(\dfrac{1}{g_{m1}} || Z_L \right) \right] \\ \qquad\quad = \dfrac{Z_L}{1 + g_{m1} Z_L} \left[g_{m1} v_{i(+)} - g_{m2} v_{i(-)} \right] \\ v_{o(-)} = -\dfrac{Z_L}{1 + g_{m1} Z_L} \left[g_{m2} v_{i(+)} - g_{m1} v_{i(-)} \right] \end{cases} \tag{17}$$

where g_{m1} is the transconductance of the M_1/M_3, g_{m2} is the transconductance of M_2/M_4, and Z_L is the load impedance of the following stage.

Ideally, the voltage gain $(\Delta V_o/\Delta V_i)$ is $2g_m Z_L/(1 + g_m Z_L)$ if $g_m = g_{m1} = g_{m2}$. When compared with a single common-source amplifier with a diode-connected load or a common-drain amplifier, the cross-coupled amplifier has twice the voltage gain and can reduce the amplitude/phase error of the input signals. If input differential signals have amplitude imbalance and phase error, i.e., $v_-(i) = -E_r v_+(i)$, where E_r is a complex value near to unity. The ratio of the differential outputs is expressed as

$$\begin{aligned} \frac{v_{-(o)}}{v_{+(o)}} &= \frac{g_{m1} v_{-(i)} - g_{m2} v_{+(i)}}{g_{m1} v_{+(i)} - g_{m2} v_{-(i)}} = -\frac{g_{m1} E_r + g_{m2}}{g_{m1} + g_{m2} E_r} \\ &= -1, \qquad \text{if } g_{m1} = g_{m2}. \end{aligned} \tag{18}$$

That is, the output voltages are perfectly differential if $g_{m1} = g_{m2}$ even though the input signals have certain amplitude/phase mismatches.

As mentioned, the capacitance loadings (mixers) of the PPF result in an incredible loss. The peaking inductors are in parallel with the SHM cores. The 3-D inductor of 11 turns with 8-μm linewidth, 2-μm line spacing, and an outer diameter of only 100 μm is used at the LO port. The differential inductance is 12 nH and $Q = 3.5$ at around 2.5–3 GHz. By simulation, the placement of the 3-D inductor reduces 3-dB LO power loss when compared with a pure capacitive mixer load, although the inductor Q is not high.

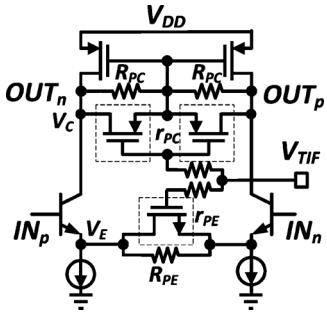


Fig. 11. VGA with a modified R-r attenuation method of both load and emitter attenuators while V-NPN BJTs are employed at the transconductance stage.

C. IF Variable-Gain Amplifier

V-NPN BJTs are also used at the input g_m stage of the IF amplifier to eliminate the $1/f$ noise problem. Besides, the g_m of a BJT transistor is much larger than that of a MOS transistor for the same bias current. Thus, the voltage gain of the VGA is improved using V-NPN BJTs. Conventionally, the quasi-exponential function was realized by an R-r attenuation load with a combination of the constant resistance R of the rigid resistance and the variable resistance r implemented by a MOS transistor in the triode region, as shown in Fig. 11 [13], [14]. The impedance of the R-r attenuator can be expressed as $R/(1 + R \times g_{\rm ds})$, and has an approximate exponential characteristic in a certain region [13]. It is well known that $g_{\rm ds}$ is proportional to the gate overdrive voltage $(V_{\rm OV})$ in the triode region. Thus, we can control the impedance of the attenuation load with the R-r exponential function. The R-r attenuation load is typically implemented at the load of the VGA. However, the output 1-dB compression point $({\rm OP}_{\rm 1dB})$ degrades in low-gain mode due to the limited input linear range, especially for a BJT input g_m cell. Therefore, both loading and emitter R-r attenuators are applied to maintain the ${\rm OP}_{\rm 1dB}$ of the VGA, especially in low-gain mode. The equivalent two-section R-r attenuation results in a wider linear-in-decibel tuning range ($\sim$ 20 dB) while typically a one-section R-r attenuator has a linear-in-decibel tuning region of approximately 10 dB.

The schematic of the VGA with both loading/emitter R-r attenuators is shown in Fig. 11. A pMOS is employed at the drain node and an nMOS is chosen for the emitter degeneration. The drain–source resistance $(R_{\rm ds} = 1/g_{\rm ds})$ of the nMOS/pMOS transistor in the triode region decreases/increases as the IF tuning voltage $V_{\rm TIF}$ increases. Thus, the voltage gain has a positive gain slope with respect to the $V_{\rm TIF}$.

The differential voltage gain of the VGA can be easily formulated as

$$A_V = \frac{g_m R_C}{1 + g_m \dfrac{R_E}{2}} \tag{19}$$

where $R_E = R_{\rm PE} \| r_{\rm PE}$ and $R_C = R_{\rm PC} \| r_{\rm op} \| r_{\rm on} \| r_{\rm PC} \approx R_{\rm PC} \| r_{\rm PC}$ while assuming $r_{\rm op}, r_{\rm on} \gg R_{\rm PC}$. $R_{{\rm PE},C}$ is the rigid resistor and $r_{{\rm PE},C}$ is the nMOS/pMOS drain–source resistance in the triode region.

Fig. 12(a) shows the calculated numerator $g_m \times R_C$ and the inverse of the denominator, $1/(1 + g_m \times R_E/2)$, as a function of the IF tuning voltage $(V_{\rm TIF})$. On the curve of $g_m \times R_C$, the transition $(T1_C)$ occurs when $r_{\rm PC}$ becomes larger than $R_{\rm PC}$. The curve of $1/(1 + g_m R_E/2)$ has two transitions, $T1_E$ and $T2_E$. $T1_E$ transition occurs as $r_{\rm PE}$ becomes smaller than $R_{\rm PE}$, while $T2_E$ occurs as $g_m R_E/2$ becomes less than 1 (i.e., $R_E < 2/g_m$). Typically, two tuning voltages should be used to control the two tuning operations. However, after proper design of bias points by transistor sizes, one tuning voltage can be adopted by properly overlapping the two constituent tuning curves. Since A_V is the multiplication of both curves, different sequences of transitions result in different composite tuning curves. Fig. 12(b) shows the calculated A_V for two sequences: (1) $T1_C < T1_E < T2_E$ and (2) $T1_E < T1_C < T2_E$, respectively. For the former sequence, there is a certain region with a constant voltage gain, which is not permissible for real applications, as shown in Fig. 12(b). On the contrary, a smooth tuning curve can be obtained by the latter sequence of $T1_E < T1_C < T2_E$.

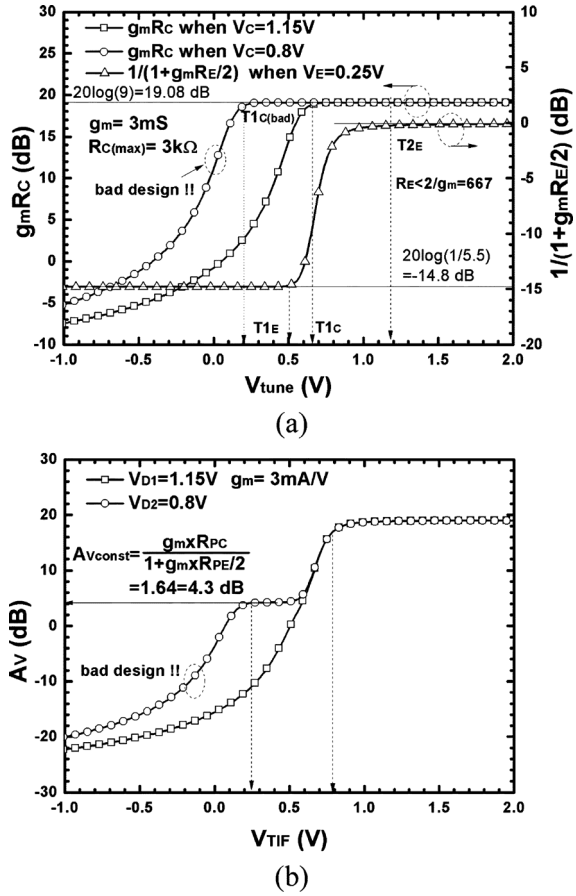


Fig. 12. (a) Numerator $(g_m R_C)$ and inverse of the denominator $[1/(1 + g_m R_E/2)]$ of the voltage gain (A_V) with different locations of transitions. (b) Corresponding A_V as a function of $V_{\rm TIF}$.

IV. Measurement Results

A die photograph of the low-power low-noise tunable-band SH-DCR for U-NII bands is shown in Fig. 13, and the die size is 1.4 $\times$ 1.05 mm^2. On-wafer measurement facilitates the RF performance. The current consumption of the first/second-stage LNA is 2.5/0.8 mA, while the mixer and VGA consume 1

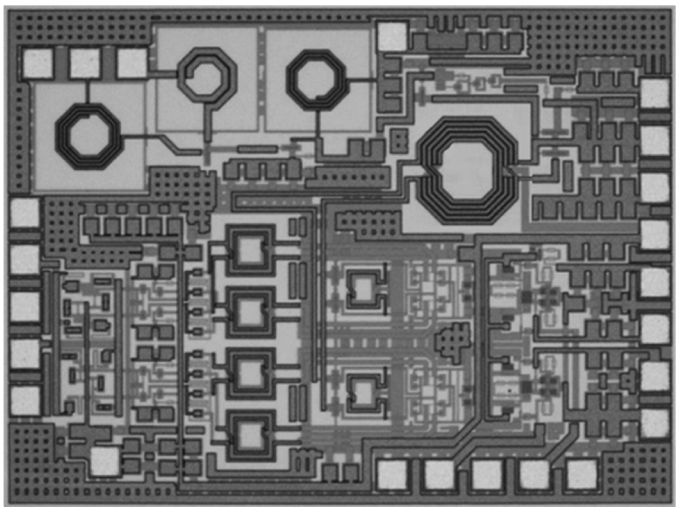


Fig. 13. Die photograph of the proposed SH-DCR with tunable narrowband LNA and wideband LO generator in a standard 0.18-μm CMOS process.

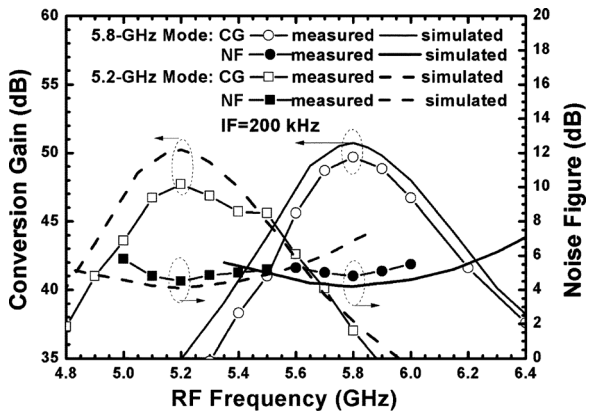


Fig. 14. CG and NF with respect to RF frequency of the proposed SH-DCR.

and 0.4 mA for each I/Q path, respectively. Besides, each LO buffer placed between 45° phase shifter and the PPF consumes 1.2 mA. Thus, the total current consumption is 8.5 mA at a 1.8-V supply. Fig. 14 shows the conversion gain (CG) and the NF as a function of RF frequency, while IF $=$ 200 kHz. Due to the tunable RF band, two situations with maximum CG at 5.2/5.8 GHz are reported. The 5.2-GHz mode is tested for U-NII-1 band and U-NII-2 band, while the 5.8-GHz mode is tested for the U-NII-3 band. The peak CG at 5.2/5.8 GHz is 48/50 at its corresponding maximum condition, while the minimum NF is 4.5/4.8 dB. Fig. 15 shows the CG with respect to the LO power when RF $=$ 5.2002/5.8002 GHz and LO $=$ 2.6/2.9 GHz, respectively. 7/8-dBm LO power is applied for all the following measurements. Note that the effective LO voltage at the switching core is around 0.3 V by simulation. Fig. 16 shows the NF with respect to IF frequency when LO $=$ 2.6/2.9 GHz, respectively, and the $1/f$ corner is around 70 kHz while the measured IF gain bandwidth is 50 MHz.

Fig. 17 shows the gain difference and I/Q phase error with respect to RF frequency. The phase/amplitude imbalance are extracted from the IF output waveforms measured by an oscilloscope. The phase error has a bowl shape and is less than $\pm 1^\circ$ within 4.5–6.4 GHz, while the amplitude imbalance is less

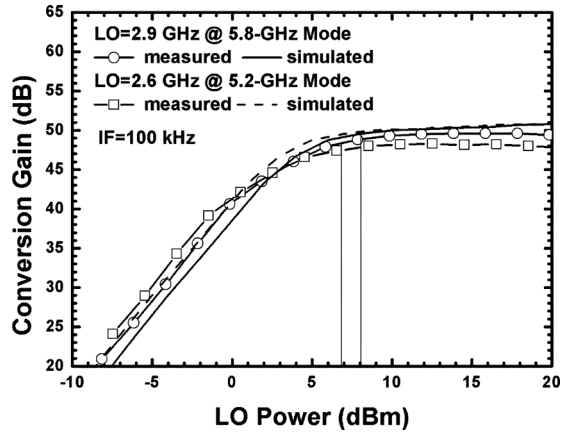


Fig. 15. CG with respect to LO power of the proposed SH-DCR.

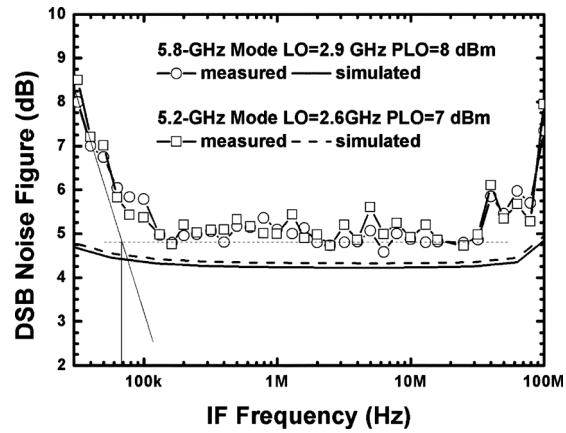


Fig. 16. NF of the proposed SH-DCR.

than ± 0.6 dB. Fig. 18(a) shows the CG as a function of the LNA RF tuning voltage (V_{TRF}) at RF $=$ 5.2/5.8 GHz, respectively, while Fig. 18(b) indicates the CG with respect to the VGA IF tuning voltage (V_{TIF}). A tuning range exceeding 20 dB is achieved by each RF/IF tuning scheme. Fig. 19 shows the IIP_2 of the SH-DCR of ten samples. The minimum IIP_2 is 26/23 dBm at 5.2/5.8 GHz band, respectively. Note that using a differential LNA can further decrease the differential imbalance of the mixer inputs and thus increase the overall IIP_2 at the cost of extra dc current consumption.

The LO-to-RF isolation is over 75 dB, while the LO frequency ranging from 2.5 to 3.2 GHz, as shown in Fig. 20(a). As shown in Fig. 20(b), the dc offset due to self-mixing is strongly reduced because 63/70-dB LO rejection is obtained at LO $=$ $1/2\times$RF $=$ 2.6/2.9 GHz, respectively. The worst case dc offset due to LO self-mixing can be calculated as [15]

$$V_{\text{DC-offset}} = V_{\text{LO-LEA}} \cdot CG_{\text{LO}}. \tag{20}$$

where $V_{\text{LO-LEA}}$ represents the observed LO leakage at the RF port and $\mathrm{CG}_{\mathrm{LO}}$ stands for the CG of a mixer when the input signal is applied at LO frequency. Thus, the dc offset due to LO self-mixing is around -93 dBm (i.e., 5 μV) at LO near both 2.6/2.9-GHz bands. In addition, the input return loss is greater than 10 dB covering 5–6 GHz, as shown in Fig. 21. Finally, the circuit performance is summarized and compared with the state-of-the-art DCRs in Table I. A DCR with fundamental

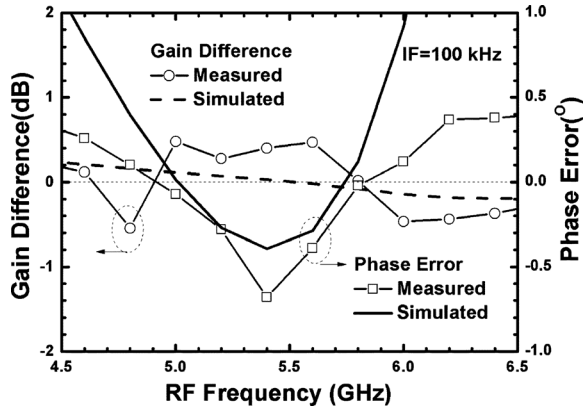


Fig. 17. Gain difference and phase error of the IF I/Q outputs of the proposed SH-DCR.

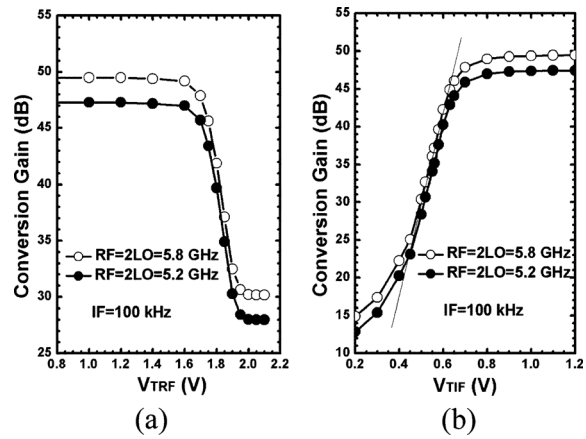


Fig. 18. CG with respect to: (a) RF tuning voltage (V_{TRF})and (b) IF tuning voltage (V_{TIF}) of the proposed SH-DCR.

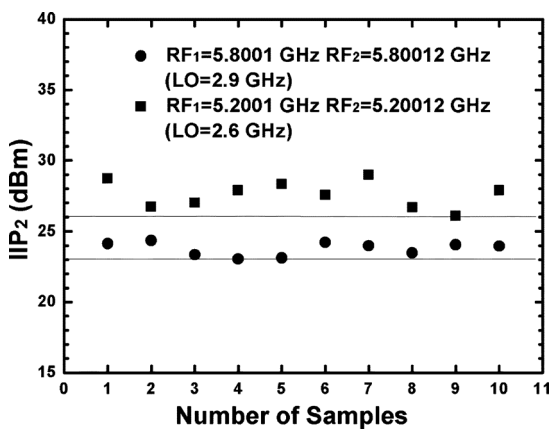
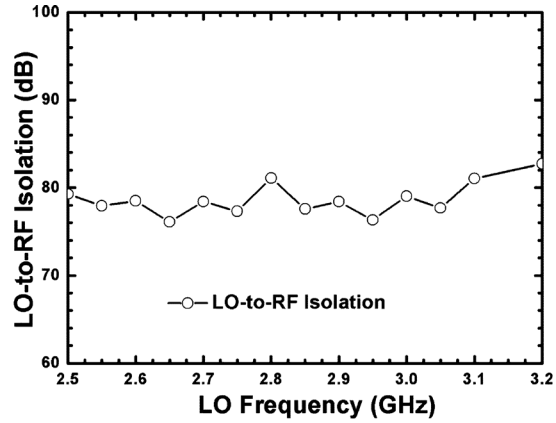


Fig. 19. IIP_2 of the proposed SH-DCR.



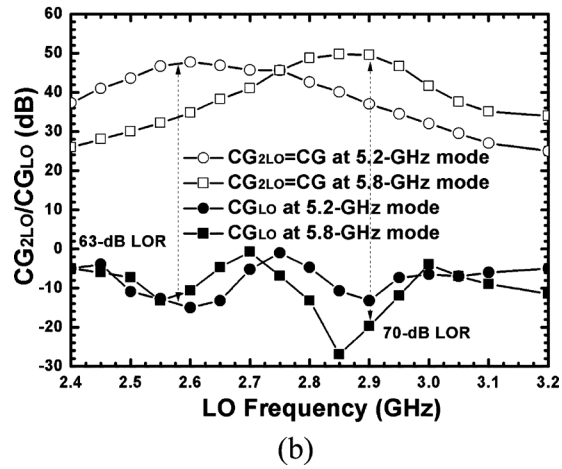


Fig. 20. (a) LO/2LO-to-RF isolation. (b) CG when $\mathrm{RF} = \mathrm{LO} + \mathrm{IF}$ and $\mathrm{RF} = 2\mathrm{LO} + \mathrm{IF}$ of the proposed SH-DCR.

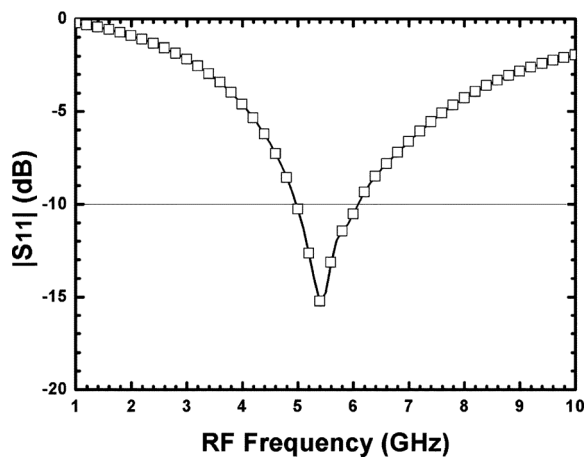


Fig. 21. Input matching of the proposed SH-DCR.

mixers [16]–[18] has simpler downconversion circuit structures than that with SHMs [15], [19], [20], but has a worse output dc offset due to LO self-mixing. Both passive mixers [16], [17] and BJT active mixers (including using SiGe HBT technology [18]–[20] or V-NPN BJT in standard CMOS process in this study) have excellent $1/f$ noise corner when compared with the CMOS active mixers [15].

The proposed tunable-band LNA structure can save power consumption when compared to the wideband structure since the IF channel bandwidth is very narrow, as discussed in Section II. The BJT used as the IF g_m stage also helps save current consumption because of its higher g_m when compared with that of the nMOS device for the same dc current without degrading the $1/f$ noise property, as indicated in Section III-C. In addition, although the 45° phase shifter and the PPF are well-known building blocks, direct cascading two blocks for octet-phase generation may cause incredible loss due to the loading effect. After detailed analyses in Section III-B, the insertion of the inter-stage buffer amplifier not only keeps the phase accuracy of the phase shifter, but also solves the voltage

TABLE I
PERFORMANCE COMPARISONS OF SUB-HARMONIC DIRECT-CONVERSION RECEIVERS

Reference	[16]	[17]	[18]	[19]	[20]	[15]	This Work
Topology (**F**: fundamental; **SH**: sub-harmonic **P**: Passive, **A**:Active)	**F, P**	**F, P**	**F, A**	**SH, A**	**SH, A**	**SH, A**	**SH, A** (Top-LO, w/ BJT core)
RF Frequency (GHz)	5.15-5.35	5	5.8	5.8	5	5-6	5.2/5.8 (Tunable)
Conversion Gain (dB)	29	26	20.23	13.6	18-20	26.2	48/50 28/30 (low gain)
LO Power (dBm)	0	N/R	-10[1]	0	−5	15.5	7/8
Noise Figure (dB)	5.3	3.5	9.89	9.7	6.8	7.2/5.2[2]	4.5/4.8
$1/f$ noise corner (kHz)	45	200	--	--	--	3000	70
IIP_3 (dBm)	−21	−2	-6.76	N/R	N/R	−12.5	−34/−36 −14/−15 (low gain)
IIP_2 (dBm)	13	18-24	21	N/R	29[3]	45.9[3]	26/23
DC offset (mV)	N/R	0.4[4]	<1	N/R	N/R	0.001[4]	0.005[4]
Supply Voltage (V)	--	1.8	2.8-3.75	2.7	3.3	1	1.8
Power Dissipation (mW)	I_d=17.5 mA	72	64[5]	16.74[3]	52.8	45.5	15.3
Technology	0.18μm CMOS	0.13μm CMOS	SiGe HBT (f_T=47 GHz)	SiGe HBT (f_T=50 GHz)	SiGe HBT (f_T=50 GHz)	0.18μm CMOS	0.18μm CMOS

[1] 2LO input for LO divider
[2] After inductively coupled plasma (ICP) post process
[3] Only mixers
[4] Calculated using $V_{LO\text{-}LEA} \times CG_{LO}$
[5] Only LNA+I/Q mixers (excluding LO divider)

loss of the PPF while the peaking inductors are placed after the PPF to further reduce the LO power loss. Through design optimizations above, the proposed tunable-band SH-DCR has less power consumption than these at similar bands in the references listed in Table I, but maintains excellent gain/noise performance.

V. CONCLUSION

A 0.18-μm CMOS low-power SH-DCR has been demonstrated using a tunable narrowband RF LNA and wideband LO generator. A tunable narrowband structure has better performance than a wideband design at a given power consumption. In addition, V-NPN BJTs have been applied to the LO switching core for $1/f$ noise improvement. With the resonance inductors and sub-harmonic mixing operation, the proposed downconversion mixer operates at three times the f_T of the V-NPN BJTs. As a result, the demonstrated receiver achieves 48/50-dB voltage gain, 4.5/4.8-dB NF, and the $1/f$ noise corner is around 70 kHz when the RF band is tuned at 5.2/5.8 GHz, respectively. Besides, IIP_2 is 26/23 dBm, while the calculated dc offset is only around 5 μV.

APPENDIX A
DERIVATION OF THE PEAK GAIN AND THE CORRESPONDING CRITERION OF THE LC TANK WITH LOSSY INDUCTOR

As mentioned in Section II, the impedance of the LC tank with $R_s = \alpha L$ can be expressed as

$$Z(s) = \frac{R_s + sL}{1 + sCR_s + s^2LC} = \frac{\alpha L + sL}{1 + s\alpha LC + s^2LC}. \quad \text{(A1)}$$

Thus,

$$|Z| = \frac{\sqrt{\omega^2 + \alpha^2}L}{\sqrt{(1-\omega^2LC)^2 + (\alpha\omega LC)^2}}. \quad \text{(A2)}$$

Take the differentiation by C, $|Z|_{\max}$ occurs at $(\omega^2 + \alpha^2)LC = 1$.

As a result,

$$\begin{aligned} |Z|_{\max} &= |Z|_{(\omega=\omega_0=\sqrt{1/(LC)-\alpha^2})} \\ &= \frac{(\omega_0^2+\alpha^2)L}{\alpha} \\ &= \left[1 + \left(\frac{\omega_0}{\alpha}\right)^2\right] \cdot (\alpha L) \\ &= (1+Q^2) \cdot R_s \\ &\equiv R_p. \end{aligned} \quad \text{(A3)}$$

Dividing (A2) by (A3), $|Z|/|Z|_{\max}$ can be obtained as

$$\begin{aligned} \frac{|Z|}{|Z|_{\max}} &= \frac{\dfrac{\sqrt{\omega^2+\alpha^2}L}{\sqrt{(1-\omega^2LC)^2+(\alpha\omega LC)^2}}}{\left[\dfrac{(\omega_0^2+\alpha^2)L}{\alpha}\right]} \\ &= \frac{\alpha\sqrt{\omega^2+\alpha^2}}{\sqrt{[\omega^2-(\omega_0^2+\alpha^2)]^2+(\alpha\omega)^2}} \\ &\quad \left[\because (\omega_0^2+\alpha^2)LC = 1\right] \\ &= \frac{\dfrac{1}{Q}\sqrt{\left(\dfrac{\omega}{\omega_0}\right)^2 + \dfrac{1}{Q^2}}}{\sqrt{\left[\dfrac{\omega^2}{\omega_0^2} - \left(1+\dfrac{1}{Q^2}\right)\right]^2 + \left(\dfrac{1}{Q}\dfrac{\omega}{\omega_0}\right)^2}}. \end{aligned} \quad \text{(A4)}$$

Further, substitute $W = (\omega/\omega_0)$ for simplicity and assume $Q = \omega_0/\alpha \gg 1$ for a high-Q condition, $|Z|/|Z|_{\max}$ can be rewritten as

$$\frac{|Z|}{|Z|_{\max}} = \frac{\dfrac{W}{Q}}{\sqrt{(W^2-1)^2 + \left(\dfrac{W}{Q}\right)^2}}. \quad \text{(A5)}$$

More generally, the $|Z|/|Z|_{\max}$ for the n stages of LC tanks in cascade can be expressed as

$$\frac{|Z|}{|Z|_{\max}} = \left(\frac{\frac{W}{Q}}{\sqrt{(1-W^2)^2 + \frac{W^2}{Q^2}}} \right)^n. \tag{A6}$$

The m-dB bandwidth is calculated by letting $|Z|/|Z|_{\max} = 1/10^{-m/20}$. As a result,

$$W^2 \pm \frac{k}{Q} W - 1 = 0 \tag{A7}$$

where $k = \sqrt{10^{m/10n} - 1}$. Thus,

$$W = \frac{\sqrt{\left(\frac{k}{Q}\right)^2 + 4} \pm \frac{k}{Q}}{2}. \tag{A8}$$

$\Delta W = W_H - W_L = k/Q$, where W_H and W_L are the two solutions of (A8).

Besides, if ω_H and ω_L are the target bandwidth boundaries, the center frequency is $\sqrt{\omega_H \omega_L}$ because $W_H \times W_L = 1$. The Q value for a target bandwidth from ω_L to ω_H can thus be obtained by

$$Q = \frac{k\omega_0}{\Delta\omega} = k\frac{\sqrt{\omega_H \omega_L}}{\omega_H - \omega_L}. \tag{A9}$$

Appendix B
Derivation of the Transimpedance Gain of a Transformer

The input impedance seen from the primary coil of the transformer ($Z_{\text{in}L}$), shown in Fig. 5(a), can be expressed as

$$\begin{aligned} Z_{\text{in}L} &= R_1 + sL_1 + sM\frac{i_2}{i_1} \\ &= R_1 + sL_1 - \frac{s^2M^2}{R_2 + sL_2 + \frac{1}{sC_2}}. \end{aligned} \tag{B1}$$

The Z_T of the transformer can thus be calculated as follows:

$$\begin{aligned} &Z_T(s) \\ &= \frac{V_o}{I_i} = \frac{i_1}{I_i} \times \frac{i_2}{i_1} \times \frac{V_o}{i_2} \\ &= \frac{1}{1 + sC_1 Z_{inL}} \times \frac{-sM}{R_2 + sL_2 + \frac{1}{sC_2}} \times \frac{-1}{sC_2} \\ &= \frac{sM}{(1+sR_1C_1+s^2L_1C_1)(1+sR_2C_2+s^2L_2C_2) - s^4M^2C_1C_2} \\ &= \frac{sM}{\left[\begin{array}{l}(1 + s\alpha_0 L_1C_1 + s^2L_1C_1)(1 + s\alpha_0 L_2C_2 + s^2L_2C_2) \\ -s^4k^2L_1C_1L_2C_2\end{array}\right]} \\ &= \frac{sM}{\left(1 + \frac{s\alpha_0}{\omega_0^2} + \frac{s^2}{\omega_0^2}\right)\left(1 + \frac{s\alpha_0}{\omega_0^2}X + \frac{s^2}{\omega_0^2}X\right) - \frac{s^4k^2}{\omega_0^4}X} \end{aligned} \tag{B2}$$

where $X = (L_2C_2)/(L_1C_1) = CR/n^2$, $\omega_0 = 1/\sqrt{L_1C_1}$, $R_1 = \alpha_0 L_1$, $R_2 = \alpha_0 L_2$, and $M = k\sqrt{L_1L_2}$.

That is,

$$Z_T(\omega) = \frac{\omega\frac{k}{n}L_1}{\text{Re}(W,X) - j\text{Im}(W,X)} \tag{B3}$$

where

$$\begin{cases} W = \dfrac{\omega}{\omega_0} \quad Q = \dfrac{\omega}{\alpha_0} \\ \text{Re}(W,X) = (\dfrac{W^2}{Q})[1 + (1-2W^2)X] \\ \text{Im}(W,X) = 1 - W^2(X+1) + W^4X\left(1 - k^2 - \dfrac{1}{Q^2}\right). \end{cases}$$

Here, W and X should be determined to find the $|Z_T(W,X)|_{\max}$ at a certain operation frequency ω. For the equation above, $Q = \omega/\alpha_0$ is a constant at the target frequency ω. $|Z_T(W,X)|_{\max}$ occurs when $\text{Im}(W,X) = 0$, i.e.,

$$W_{\text{opt}}^2 = \frac{X + 1 \pm \sqrt{(X+1)^2 - 4XP}}{2XP} \tag{B4}$$

where $P = (1 - k^2 - 1/Q^2)$. Thus, Z_T can be rewritten as

$$|Z_T(X)| = \frac{Q\omega\frac{k}{n}L_1}{Z(X)}. \tag{B5}$$

where

$$Z(X) = W^2\left[1 + (1-2W^2)X\right] = \frac{P-2}{2P^2}U(X) + \frac{2}{P}$$

and

$$U(X) = \frac{X+1}{X}\left[X + 1 \pm \sqrt{(X+1)^2 - 4XP}\right].$$

To determine the optimal X for $Z_T(X)_{\max}$, $Z(X)_{\min}$ (or $U(X)_{\min}$) should be also achieved after complete calculation of

$$\begin{aligned} U' =& \frac{X-1}{X^2}\left\{X+1 \pm \frac{X}{\sqrt{(X+1)^2-4XP}}\left[(X+1)^2 - 2P\right]\right\} \\ =& 0 \end{aligned}$$

where $X = 1$ is the sole "positive" solution. Thus, the optimal turn ratio of a transformer $n_{\text{opt}} = \sqrt{CR} = \sqrt{C_2/C_1}$ by the definition of $X = (L_2C_2)/(L_1C_1) = CR/n^2$.

Further, substituting $X = 1$ into (B4) and (B5),

$$\begin{cases} W_{(X=1)}^2 = \dfrac{1 \pm \sqrt{1-P}}{P} \\ Z_{T\max(X=1)} = \dfrac{Q\omega\frac{k}{n}L_1}{\left\{\frac{2}{P}\left[\left(1 - \frac{2}{P}\right)(1 \pm \sqrt{1-P}) + 1\right]\right\}}. \end{cases} \tag{B6}$$

However, for a high-coupling condition ($P = 1 - k^2 - 1/Q^2 \to 0$), $\lim_{P\to 0} W_{\max H}^2 = (1 + \sqrt{1-P})/P \to \infty$ and $\lim_{P\to 0} Z_{T\max H} \to 0$. As a result, $W_{\max H}$ is not an applicable solution and thus $W_{\max L} = (1 - \sqrt{1-P})/P$ is typically chosen. If Q is large enough, i.e., $P = 1 - k^2$, $W_{\max L}^2 = 1/(1+k)$, and

$Z_{\min L} = 2k/(1+k)^2$. Thus, the maximum Z_T can be rewritten as

$$Z_T = \frac{Q}{2n}\omega L_1(1+k)^2. \tag{B7}$$

Appendix C
Derivation of the Tuning Capability of a Transformer With Only One Varactor in Either Side

A transformer with input/output capacitor loadings (C_1/C_2) is shown in Fig. 5(a). If only C_1 can be tuned, assume $L_2C_2 = 1/\omega_2^2$ and design $L_1C_{1,max} = 1/\omega_{1,\min}^2 = X_a/\omega_2^2$, $L_1C_{1,min} = 1/\omega_{1,\max}^2 = 1/(X_a\omega_2^2)$, where $X_a > 1$.

Since $X = \omega_1^2/\omega_2^2$, $\omega_1 = \omega_0$ (B4) can be rewritten as

$$\omega_{\text{opt}}^2 = \frac{\omega_1^2 + \omega_2^2 - \sqrt{(\omega_1^2+\omega_2^2)^2 - 4\omega_1^2\omega_2^2 P}}{2P} \tag{C1}$$

where $P = (1 - k^2 - 1/Q^2 \approx 1 - k^2$ is nearly a constant because Q is large. As a result,

$$\omega_H^2 = \frac{\omega_2^2}{2P}\left[X_a + 1 - \sqrt{(X_a+1)^2 - 4X_aP}\right] \tag{C2}$$

and

$$\omega_L^2 = \frac{\omega_2^2}{2P}\left[\frac{1}{X_a} + 1 - \sqrt{\left(\frac{1}{X_a}+1\right)^2 - 4\frac{1}{X_a}P}\right] = \frac{\omega_H^2}{X_a} \tag{C3}$$

That is,

$$\frac{\omega_H^2}{\omega_L^2} = X_a = \left(\frac{C_{1,\max}}{C_{1,\min}}\right)^{1/2}. \tag{C4}$$

References

[1] L. Sheng, J. C. Jensen, and L. E. Larson, "A wide-bandwidth Si/SiGe HBT direct conversion sub-harmonic mixer/downconverter," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1329–1337, Sep. 2000.

[2] W. Kluge, F. Poegel, H. Roller, M. Lange, T. Ferchland, L. Dathe, and D. Eggert, "A fully integrated 2.4-GHz IEEE 802.15.4-compliant transceiver for ZigBee™ applications," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2767–2775, Dec. 2006.

[3] I. Nam, K. Choi, J. Lee, H.-K. Cha, B.-I. Seo, K. Kwon, and K. Lee, "A 2.4 GHz low-power low-IF receiver and direct-conversion transmitter in 0.18-μm CMOS for IEEE 802.15.4 WPAN applications," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 4, pp. 682–689, Apr. 2007.

[4] M. Brandolini, P. Rossi, D. Sanzogni, and F. Svelto, "$A+78$ dBm IIP_2 CMOS direct downconversion mixer for fully integrated UMTS receivers," *IEEE J. Solid-State Circuits*, vol. 41, no. 3, pp. 552–559, Mar. 2006.

[5] M. Zargari, M. Terrovitis, S. H.-M. Jen, B. J. Kaczynski, M. Lee, M. P. Mack, S. S. Mehta, S. Mendis, K. Onodera, H. Samavati, W. W. Si, K. Singh, A. Tabatabaei, D. Weber, D. K. Su, and B. A. Wooley, "A single-chip dual-band tri-mode CMOS transceiver for IEEE 802.11a/b/g wireless LAN," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2239–2249, Dec. 2004.

[6] M. Goldfarb, E. Balboni, and J. Cavey, "Even harmonic double-balanced active mixer for use in direct conversion receivers," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1762–1766, Oct. 2003.

[7] K.-J. Koh, M.-Y. Park, C.-S. Kim, and H.-K. Yu, "Subharmonically pumped CMOS frequency conversion (up and down) circuits for 2-GHz WCDMA direct-conversion transceiver," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 871–884, Jun. 2004.

[8] D. Manstretta, M. Brandolini, and F. Svelto, "Second-order inter-modulation mechanisms in CMOS downconverters," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 394–406, Mar. 2003.

[9] W.-Z. Chen and W.-H. Chen, "Symmetric 3-D passive components for RF ICs application," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2003, pp. 599–602.

[10] R. S. Carson, *Radio Communications Concepts: Analog*. New York: Wiley, 1990.

[11] J.-S. Syu, C. C. Meng, Y.-H. Teng, and H.-Y. Liao, "Large improvement in image rejection of double-quadrature dual-conversion low-IF architectures," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 7, pp. 1703–1712, Jul. 2010.

[12] B. G. Perumana, R. Mukhopadhyay, S. Chakraborty, C.-H. Lee, and J. Laskar, "A low-power fully monolithic subthreshold CMOS receiver with integrated LO generation for 2.4 GHz wireless PAN applications," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2229–2238, Oct. 2008.

[13] Y.-S. Youn, J.-H. Choi, M.-H. Cho, S.-H. Han, and M.-Y. Park, "A CMOS IF transceiver with 90 dB linear control VGA for IMT-2000 application," in *VLSI Circuits Tech. Symp. Dig.*, Jun. 2003, pp. 131–134.

[14] Y.-S. Youn, C.-S. Kim, N.-S. Kim, and H.-K. Yu, "A 1 GHz-band low distortion up-converter with a linear in dB control VGA for digital TV tuner," in *IEEE Radio Freq. Integr. Circuits Symp. Dig.*, May 2001, pp. 257–260.

[15] H.-C. Chen, T. Wang, and S.-S. Lu, "A 5–6 GHz 1-V CMOS direct-conversion receiver with an integrated quadrature coupler," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1963–1975, Sep. 2007.

[16] S. Zhou and M.-C. F. Chang, "A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1084–1093, May 2005.

[17] M. Valla, G. Montagna, R. Castello, R. Tonietto, and I. Bietti, "A 72-mW CMOS 802.11a direct conversion front-end with 3.5-dB NF and 200-kHz $1/f$ noise corner," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 970–977, Apr. 2005.

[18] S. Chakraborty, S. K. Reynolds, H. Ainspan, and J. Laskar, "Development of 5.8GHz SiGe BiCMOS direct conversion receivers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2003, pp. 1551–1553.

[19] B. G. Choi and C. S. Park, "A 5.8 GHz SiGe HBT direct-conversion I/Q-channel sub-harmonic mixer for low power and simplified receiver architecture," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2005, pp. 177–180.

[20] R. Svitek and S. Raman, "5–6 GHz SiGe active I/Q subharmonic mixers with power supply noise effect characterization," *IEEE Microw. Wireless Compon. Lett.*, vol. 14, no. 7, pp. 319–321, Jul. 2004.

Jin-Siang Syu (S'09) was born in Taoyuan, Taiwan, in 1984. He received the B.S. degree in communication engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2006, and is currently working toward the Ph.D. degree in electrical engineering at National Chiao Tung University.

His current research interests are in the areas of RF integrated circuits (RFICs).

Mr. Syu is a member of Phi Tau Phi.

Chinchun Meng (M'02) received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1985, and the Ph.D. degree in electrical engineering from the University of California, Los Angeles (UCLA), in 1992.

He is currently a Full Professor with the Department of Electrical Engineering, National Chiao Tung University, Hsinchu, Taiwan. His current research interests are in the areas of RFICs, microwave and millimeter-wave integrated circuits (ICs).