ESD Protection Design for 60-GHz LNA With Inductor-Triggered SCR in 65-nm CMOS Process

Chun-Yu Lin, *Member, IEEE*, Li-Wei Chu, *Student Member, IEEE*, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*—To effectively protect the radio-frequency (RF) circuits in nanoscale CMOS technology from electrostatic discharge (ESD) damages, the silicon-controlled rectifier (SCR) devices have been used as main on-chip ESD protection devices due to their high ESD robustness and low parasitic capacitance. In this paper, an SCR device assisted with an inductor is proposed to improve the turn-on efficiency for ESD protection. Besides, the inductor can be also designed to resonate with the parasitic capacitance of the SCR device at the selected frequency band for RF performance fine tuning. Experimental results of the ESD protection design with inductor-triggered SCR in a nanoscale CMOS process have been successfully verified at 60-GHz frequency. The ESD protection design with inductor-triggered SCR has been implemented in cell configuration with compact size, which can be directly used in the RF receiver circuits. To verify the RF characteristics and ESD robustness in the RF receiver, the inductor-triggered SCR has been applied to a 60-GHz low-noise amplifier (LNA). Verified in a silicon chip, the 60-GHz LNA with the inductor-triggered SCR can achieve good RF performances and high ESD robustness.**

***Index Terms*—Electrostatic discharge (ESD), low-noise amplifier (LNA), silicon-controlled rectifier (SCR), 60 GHz.**

I. Introduction

THE 60-GHz frequency band has been allocated for unlicensed usage in the next-generation wireless communications [1]. The radio-frequency (RF) circuits operating at this 60-GHz frequency have the benefits of excellent interference immunity, high security, multi-gigabit speed, and frequency re-usable, due to short transmission distance [2]. Several RF transceivers operated at this frequency had been realized in CMOS technologies [3], [4]. Nanoscale CMOS technologies have been used to implement RF circuits with the advantages of scaling-down feature size, improving high-frequency characteristics, low power consumption, high integration capability, and low cost for mass production. However, the thinner gate oxide in nanoscale CMOS technology seriously degrades the electrostatic discharge (ESD) robustness of IC products [5]. The general requirement for a commercial IC product is to pass 2-kV human-body-model (HBM) ESD tests [6]. Therefore, an on-chip ESD protection circuit must be added at the first stage of the RF receiver. As shown in Fig. 1, the ESD protection circuit is added to the input ($\mathrm{RF_{IN}}$) pad of the low-noise amplifier (LNA) against ESD damages. Several ESD protection designs have been reported for RF circuits [7], [8]. Some ESD protection designs used for 60-GHz RF LNA were also presented [9]–[12]. To minimize the impacts from the ESD protection circuit on RF performances, the ESD protection circuit at the input pads must be carefully designed.

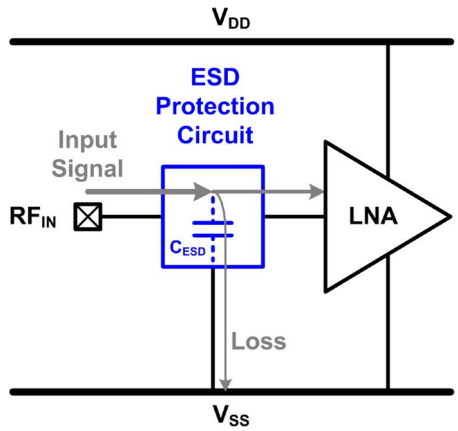

Fig. 1. ESD protection circuit added to the input ($\mathrm{RF_{IN}}$) pad of LNA against ESD damages.

ESD protection devices cause RF performance degradation with several undesired effects [13], [14]. The parasitic capacitance ($\mathrm{C_{ESD}}$) of the ESD protection device is one of the most important design considerations for RF circuits. Conventional ESD protection devices with large dimensions have large parasitic capacitances, which are difficult to be well tolerated in the RF front-end circuits. The parasitic capacitance will cause signal loss from the pad to ground. Moreover, the parasitic capacitance will change the input matching condition. Besides, adding an ESD protection device to the RF receiver will degrade the noise figure. As the operating frequencies of RF circuits are further increased, on-chip ESD protection designs for RF applications are more challenging.

Among the ESD protection devices, such as the diode, MOS, BJT, or field-oxide device, the silicon-controlled rectifier (SCR) device has been reported to be useful for RF ESD protection design due to its higher ESD robustness within a smaller layout area and lower parasitic capacitance [15]. Besides, the SCR device can be safely used without latchup danger in advanced CMOS technologies with low supply voltage [16]. The device structure of the SCR device used in RF input pad is illustrated

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in Fig. 2(a). The $\mathrm{RF_{IN}}$ pad is connected to the first P+, which is formed in the N-well. The $\mathrm{V_{DD}}$ pad is connected to the pickup N+, which is formed in the same N-well. The $\mathrm{V_{SS}}$ pad is connected to the second N+ and the pickup P+, which are formed in the nearby P-well. The trigger port is connected to the third P+, which is formed in the same P-well. The SCR path between $\mathrm{RF_{IN}}$ and $\mathrm{V_{SS}}$ consists of P+, N-well, P-well, and N+. Besides, the parasitic diode path between $\mathrm{RF_{IN}}$ and $\mathrm{V_{DD}}$ consists of P+ and N-well/N+. The equivalent circuit of the SCR consists of a PNP BJT $(\mathrm{Q_{PNP}})$ and an NPN BJT $(\mathrm{Q_{NPN}})$, as shown in Fig. 2(b). The $\mathrm{Q_{PNP}}$ is formed by the P+, N-well, and P-well, and the $\mathrm{Q_{NPN}}$ is formed by the N-well, P-well, and N+. As ESD zapping from $\mathrm{RF_{IN}}$ to $\mathrm{V_{SS}}$, the positive-feedback regenerative mechanism of $\mathrm{Q_{PNP}}$ and $\mathrm{Q_{NPN}}$ results in the SCR device highly conductive to make SCR very robust against ESD stresses. Under RF circuit operating conditions, the diode and SCR paths remain off to prevent from leakage. However, SCR has some drawbacks, such as higher trigger voltage and slower turn-on speed. To reduce the trigger voltage of an SCR device, the trigger signal can be sent into the base terminal of $\mathrm{Q_{NPN}}$ to enhance the turn-on speed. The voltage level of the trigger port is in reverse proportion to the trigger voltage of the SCR device. Therefore, some circuit design techniques are reported to enhance the turn-on efficiency of SCR devices, such as the gate-coupled, substrate-triggered, and gate-grounded-NMOS-triggered (GGNMOS-triggered) techniques [16]. Besides, some SCR devices with lower trigger voltage for RF applications are also presented, such as the diode-triggered SCR (DTSCR) [17]. However, adding a trigger circuit to SCR device also increases the parasitic capacitance seen at the $\mathrm{RF_{IN}}$ pad, which is hard to tolerate for RF circuits, especially in the 60-GHz operating frequency.

In this work, a novel inductor-triggered SCR design is proposed for effective on-chip RF ESD protection for 60-GHz frequency. The inductor acts as a conductive path to trigger the SCR device under ESD stress conditions. Besides, the inductor is used to compensate the parasitic capacitance of ESD protection device under normal RF circuit operating conditions [18], [19]. This design can achieve low trigger voltage, fast turn-on speed, high ESD robustness, and low RF performance degradation. Without additional process modification, this inductor-triggered SCR design is realized by circuit and layout skills in a 65-nm CMOS process.

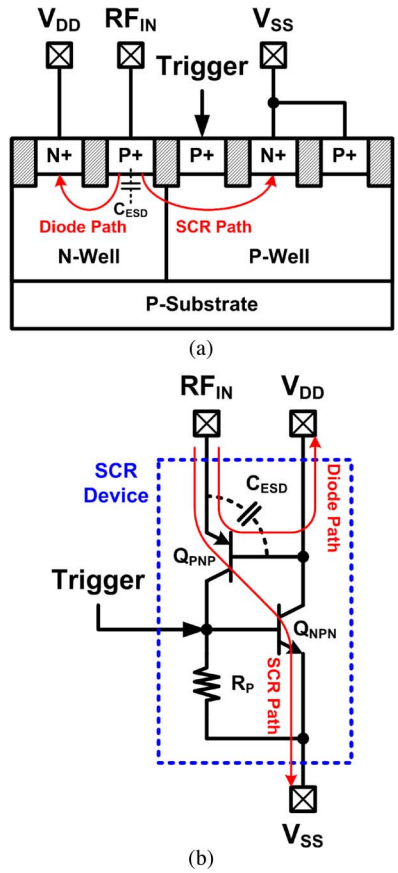


Fig. 2. (a) Device cross-sectional view, and (b) equivalent circuit, of SCR device used in RF input pad.

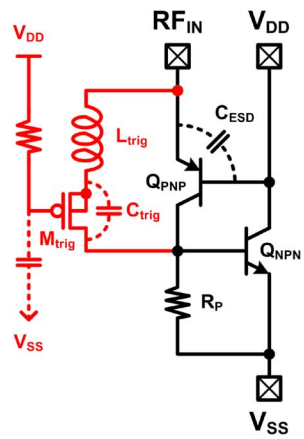


Fig. 3. Proposed inductor-triggered SCR for RF ESD protection.

II. Realization of Inductor-Triggered SCR

A. Implementation of the Inductor-Triggered SCR

The new proposed inductor-triggered SCR is shown in Fig. 3, which consists of an SCR device, an inductor $(\mathrm{L_{trig}})$, a MOS transistor $(\mathrm{M_{trig}})$, and the RC-based ESD detection circuit. The PMOS transistor is selected for $\mathrm{M_{trig}}$ since it exhibits the initial-on function for ESD protection, which can quickly pass the trigger signal to SCR device [20]. The inductor is used to provide the trigger path between the $\mathrm{RF_{IN}}$ pad and the trigger port of the SCR device under ESD stress conditions. The PMOS transistor at the trigger path, which is controlled by the ESD detection circuit, is also turned on under ESD stress conditions. When the trigger signal passes from the $\mathrm{RF_{IN}}$ pad to the trigger port of the SCR device, the SCR device can be quickly turned on to discharge the ESD current. The RC-based ESD detection circuit is used to distinguish the ESD-stress conditions from the normal circuit operating conditions. Therefore, under normal power-on conditions, the PMOS transistor is turned off to block the steady leakage current path from the $\mathrm{RF_{IN}}$ pad to the trigger port of SCR device. Under normal RF circuit operating conditions, the inductor in series with the PMOS is used to compensate the parasitic capacitance of the SCR device $(\mathrm{C_{ESD}})$.

Fig. 4 shows the proposed ESD protection scheme for an RF receiver, including the inductor-triggered SCR, the diode $(\mathrm{D_N})$, and the power-rail ESD clamp circuit. The inductor-triggered

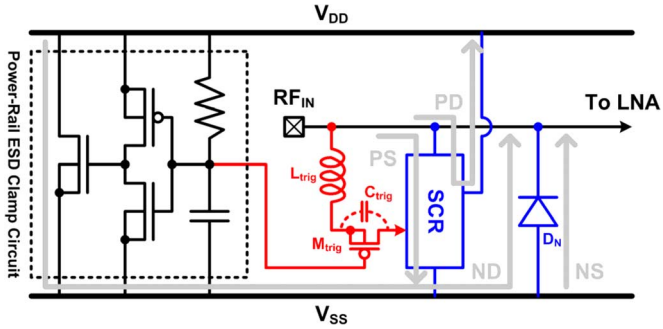


Fig. 4. Proposed ESD protection scheme for $\mathrm{RF_{IN}}$ pad with inductor-triggered SCR, $\mathrm{D_N}$, and power-rail ESD clamp circuit.

SCR assisted with the diode $(\mathrm{D_N})$ and the power-rail ESD clamp circuit is used to provide the ESD current discharging paths for the $\mathrm{RF_{IN}}$ pad. The power-rail ESD clamp circuit, which consists of the RC-inverter-triggered NMOS, is used to provide ESD current paths between $\mathrm{V_{DD}}$ and $\mathrm{V_{SS}}$ under ESD stress conditions. The R ($\sim$ 10 kΩ) and C ($\sim$10 pF) with the time constant of 0.1 μs $\sim$ 1 μs can distinguish the ESD transients from the normal circuit operating conditions. Under normal circuit operating conditions, the node between R and C is charged to the high potential $(\mathrm{V_{DD}})$. Under ESD stress conditions, the ESD voltage at $(\mathrm{V_{DD}})$ has the fast rise time in the order of $\sim$10 ns. With the RC delay, the power-rail ESD clamp circuit is turned on to provide ESD current path from $\mathrm{V_{DD}}$ to $\mathrm{V_{SS}}$. Since the power-rail ESD clamp circuit is placed between $\mathrm{V_{DD}}$ and $\mathrm{V_{SS}}$, the impact on $\mathrm{RF_{IN}}$ pad is minor. The RC used in the power-rail ESD clamp circuit can also be used to control the PMOS in the inductor-triggered SCR. With such a configuration, the resistor for ESD detection circuit in the original inductor-triggered SCR can be merged into the power-rail ESD clamp circuit.

In the ESD protection design with the inductor-triggered SCR, the dimensions of the inductor $(\mathrm{L_{trig}})$, PMOS transistor $(\mathrm{M_{trig}})$, SCR device, and diode $(\mathrm{D_N})$ can be designed to minimize the RF performance degradation. Since the capacitor used in power-rail ESD clamp circuit is large enough ($\sim$10 pF) to keep the node between R and C at ac ground under normal RF circuit operating conditions, the impedance of the trigger path $(\mathrm{Z_{trig}})$ seen at the $\mathrm{RF_{IN}}$ pad to ground can be calculated as

$$Z_{\mathrm{trig}} \approx j\omega L_{trig} + \frac{1}{j\omega C_{trig}} = j\omega\left(L_{trig} - \frac{1}{\omega^2 C_{trig}}\right) \quad (1)$$

where the ω is the angular frequency and the $\mathrm{C_{trig}}$ can be expressed as

$$C_{trig} \approx C_{gs} + C_{gb} + C_{db}. \quad (2)$$

The $\mathrm{C_{gs}}$, $\mathrm{C_{gb}}$, and $\mathrm{C_{db}}$ denote the gate-to-source capacitance, gate-to-body capacitance, and drain-to-body capacitance of the PMOS transistor $(\mathrm{M_{trig}})$, respectively. The resonance angular frequency (ω_{o}), which is designed to be the operating frequency of RF signal, can be obtained by

$$\omega_{\mathrm{o}} = \frac{1}{\sqrt{\left(L_{trig} - \frac{1}{\omega_{\mathrm{o}}^2 C_{trig}}\right) C_{ESD}}} \quad (3)$$

where the $\mathrm{C_{ESD}}$ is the parasitic capacitance contributed by the SCR and diode $(\mathrm{D_N})$. The sizes of SCR and $\mathrm{D_N}$ depend on the required ESD robustness, while the size of $\mathrm{M_{trig}}$ transistor depends on the required trigger current. Once the sizes of $\mathrm{M_{trig}}$ transistor, SCR, and $\mathrm{D_N}$ have been chosen, the required inductance $(\mathrm{L_{trig}})$ can be determined.

Fig. 4 also shows the ESD current paths under positive-to-$\mathrm{V_{SS}}$ (PS), positive-to-$\mathrm{V_{DD}}$ (PD), negative-to-$\mathrm{V_{SS}}$ (NS), and negative-to-$\mathrm{V_{DD}}$ (ND) ESD stress conditions. During positive-to-$\mathrm{V_{SS}}$ ESD stress, ESD current will first pass through the inductor $(\mathrm{L_{trig}})$ and PMOS $(\mathrm{M_{trig}})$ to trigger the SCR device. The major ESD current will be discharged by the SCR device from the $\mathrm{RF_{IN}}$ pad to $\mathrm{V_{SS}}$. Under positive-to-$\mathrm{V_{DD}}$ ESD stress, the ESD current will be discharged by the parasitic diode path embedded in the SCR device from the $\mathrm{RF_{IN}}$ pad to $\mathrm{V_{DD}}$. During negative-to-$\mathrm{V_{SS}}$ ESD stress, the ESD current will be discharged by the forward-biased $\mathrm{D_N}$ from the $\mathrm{V_{SS}}$ to $\mathrm{RF_{IN}}$ pad. Under negative-to-$\mathrm{V_{DD}}$ ESD stress, the ESD current will be discharged by the power-rail ESD clamp circuit and the $\mathrm{D_N}$ from $\mathrm{V_{DD}}$ to $\mathrm{RF_{IN}}$ pad. The proposed ESD protection scheme in Fig. 4 can provide the corresponding current discharging paths with good ESD robustness.

The device dimensions of the test circuits with the inductor-triggered SCR are listed in Table I. A commercial 65-nm CMOS technology is used in this work. The ESD protection circuit with the inductor-triggered SCR is designed for 60-GHz RF applications. The test patterns include the test circuits A, B, C, and D. The size of SCR device used in the test circuits A, B, C, and D are split as 8 μm, 15 μm, 23 μm, and 30 μm, respectively. The size of $\mathrm{D_N}$ in test circuits A, B, C, and D are split as also 8 μm, 15 μm, 23 μm, and 30 μm, respectively. The parasitic capacitance $(\mathrm{C_{ESD}})$ of ESD protection devices in test circuits A, B, C, and D at 60 GHz are estimated as $\sim$25 fF, $\sim$50 fF, $\sim$75 fF, and $\sim$100 fF, respectively. The width/length of PMOS $(\mathrm{M_{trig}})$ in each test circuit is kept at 100 μm/0.2 μm, and the equivalent $\mathrm{C_{trig}}$ is $\sim$50 fF at 60 GHz. Therefore, the required inductors $(\mathrm{L_{trig}})$, including the parasitic inductance of metal connections, are $\sim$0.38 nH, $\sim$0.27 nH, $\sim$0.23 nH, and $\sim$0.2 nH for the test circuits A, B, C, and D.

B. Simulation Under 60-GHz Frequency

The RF characteristics of the test circuits are simulated by using the microwave circuit simulator ADS with the selected device dimensions. Since the SCR model is not provided in the given CMOS process, diodes with P+/N-well, N+/P-well, and N-well/P-well junctions are used to simulate the SCR devices. A signal source with 50-Ω impedance drives the port 1 ($\mathrm{RF_{IN}}$ pad) of the test circuit, and a 50-Ω load is connected to the port 2 to simulate the RF receiver. The voltage supply of $\mathrm{V_{DD}}$ $(\mathrm{V_{SS}})$ is 1 V (0 V), and the dc bias of $\mathrm{RF_{IN}}$ is 0.5 V. The simulated reflection $(\mathrm{S_{11}})$ parameters are shown in Fig. 5(a). These ESD protection circuits exhibit good input matching $(\mathrm{S_{11}} - \mathrm{parameters} < -10\ \mathrm{dB})$ around 60 GHz. The transmission $(\mathrm{S_{21}})$ parameters are compared in Fig. 5(b). At 60-GHz frequency, the test circuits A, B, C, and D have about 0.5-dB, 0.8-dB, 1.2-dB, and 1.5-dB power loss, respectively. Although the parasitic capacitance of the ESD protection devices can be resonated out, the losses are still contributed by the parasitic resistance of the SCR

TABLE I
DEVICE DIMENSIONS AND MEASUREMENTS RESULTS ESD PROTECTION DESIGNS WITH INDUCTOR-TRIGGERRED SCR

		Test Circuits							
		A	A'	B	B'	C	C'	D	D'
Device Dimensions	SCR (μm)	8		15		23		30	
	D_N (μm)	8		15		23		30	
	L_{trig} (nH)	0.38		0.27		0.23		0.2	
	M_{trig} (μm / μm)	100 / 0.2		100 / 0.2		100 / 0.2		100 / 0.2	
	Area (μm x μm)	120 x 150		110 x 140		105 x 135		100 x 130	
	RF-NMOS Emulator	w/o	w/i	w/o	w/i	w/o	w/i	w/o	w/i
Measurement Results	S_{11} at 60 GHz (dB)	-19.1		-18.2		-20.4		-24.6	
	S_{21} at 60 GHz (dB)	-1.24		-1.39		-1.60		-1.84	
	PS HBM ESD Level (kV)		0.75		1.5		2.25		2.75
	PD HBM ESD Level (kV)		1		1.5		2.25		2.75
	NS HBM ESD Level (kV)		0.75		1.5		2.25		3
	ND HBM ESD Level (kV)		0.75		1.5		2.25		3
	PS TLP-Measured It_2 (A)		0.37		0.72		1.39		1.78
	PS VF-TLP-Measured It_2 (A)	1.98	0.96	2.72	1.72	3.08	2.14	3.71	2.21

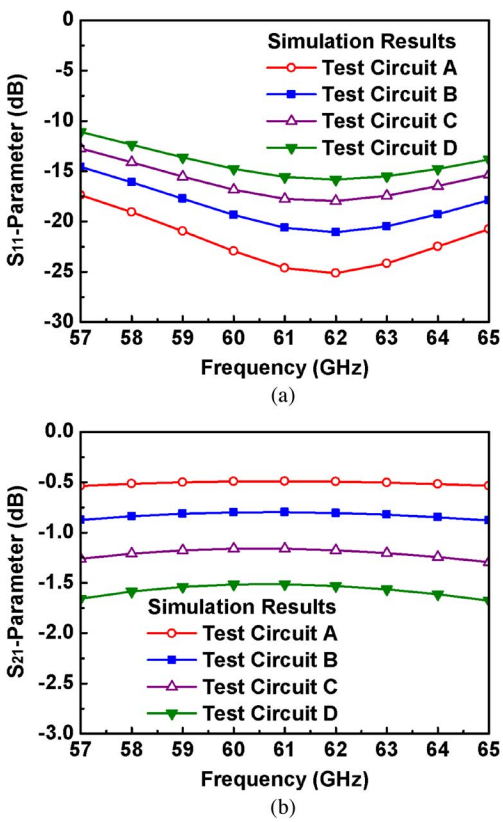


Fig. 5. Simulation results of proposed ESD protection scheme on (a) S_{11}-parameter and (b) S_{21}-parameter.

and D_N. Since these test circuits exhibit good RF performances between 57 ~ 65 GHz, they can be operated at 60 GHz even if some variation happens on device values.

C. Simulation Under Normal Power-On Conditions

The test circuits under normal power-on conditions and ESD transient events are simulated by using HSPICE. Under the normal power-on condition, the dc bias of $\mathrm{RF_{IN}}$ is raised from 0 V to 1 V with 1-ms rise time. The gate voltage of PMOS $(\mathrm{M_{trig}})$ is biased at 1 V through the resistor of power-rail ESD clamp circuit, so $\mathrm{M_{trig}}$ can be kept off and no trigger signal is generated from the $\mathrm{RF_{IN}}$ pad to the SCR device. Fig. 6(a) shows the HSPICE-simulated voltage waveforms of the test circuit D under the normal power-on condition. The trigger signal remains at 0 V, so the SCR device is kept in off state.

D. Simulation Under ESD Transient Events

When a positive fast-transient ESD voltage is applied to $\mathrm{RF_{IN}}$ with $\mathrm{V_{SS}}$ grounded, the RC delay in the ESD detection circuit keeps the gate of $\mathrm{M_{trig}}$ at a relatively low voltage level compared to the fast rising voltage level at $\mathrm{RF_{IN}}$. The $\mathrm{M_{trig}}$ can be quickly turned on by the ESD energy to generate the trigger signal into the trigger port of the SCR device. Finally, the SCR device can be fully turned on to discharge ESD current from $\mathrm{RF_{IN}}$ to $\mathrm{V_{SS}}$. Fig. 6(b) shows the simulated voltage waveforms of the test circuit D under the ESD transition, where a 0-to-5 V voltage pulse with 10-ns rise time is applied to $\mathrm{RF_{IN}}$ to simulate the fast transient voltage of human-body-model (HBM) ESD event [6]. With the limited voltage height of 5 V in the voltage pulse, the simulation results can check the desired trigger function before the RF circuit breakdown.

Fig. 6(c) shows the simulated voltage waveforms of the test circuit D under the other ESD transition, where a 0-to-5 V voltage pulse with 0.1-ns rise time is applied to $\mathrm{RF_{IN}}$ to simulate the faster transient voltage of charged-device-model (CDM) ESD event [6]. With the large enough trigger signal,

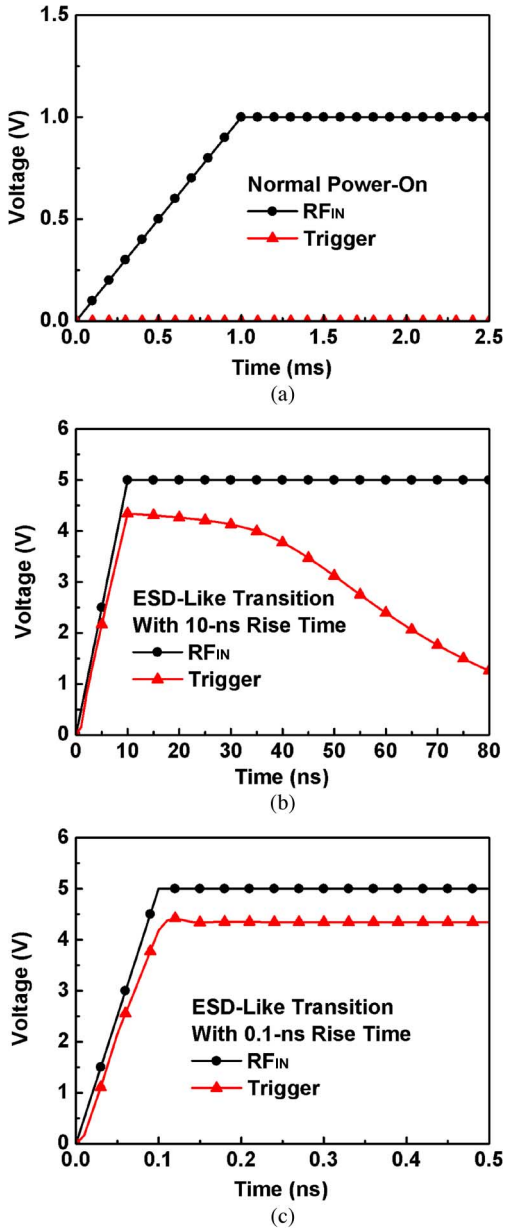


Fig. 6. HSPICE-simulated results of proposed ESD protection scheme under (a) normal power-on condition, (b) ESD-like transition with 10-ns rise time, and (c) ESD-like transition with 0.1-ns rise time.

the SCR device should be triggered on before RF circuit breakdown during ESD stress condition.

III. Experimental Results of Inductor-Triggered SCR

The test circuits of inductor-triggered SCR have been fabricated in a 65-nm salicided CMOS process without using the silicide-blocking mask. One set of the test circuits are implemented with ground-signal-ground (G-S-G) pads to facilitate on-wafer two-port S-parameters measurement, which are labeled as test circuits A, B, C, and D. The other set of the test circuits are implemented with the RF-NMOS emulators [12] for ESD tests, which are labeled as test circuits A′, B′, C′, and D′, as listed in Table I. The RF-NMOS emulator, which consisted of one RF NMOS with gate terminal connected to the $\mathrm{RF_{IN}}$ pad, and the drain, source, and body terminals connected to $\mathrm{V_{SS}}$ pad, is used

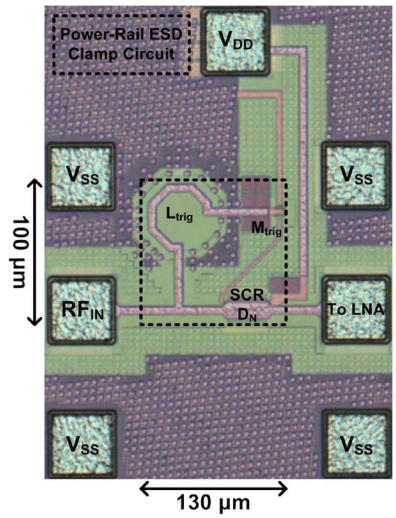


Fig. 7. Chip micrograph of test circuit D.

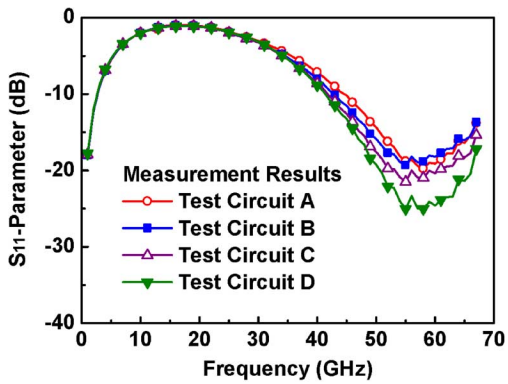
to simulate the RF receiver under ESD stress condition. The ESD robustness of the test circuits can be estimated by the test patterns with the RF-NMOS emulators. Except the RF-NMOS emulator, the device sizes of test circuits A, B, C, and D are equal to those of test circuits A′, B′, C′, and D′, respectively. The chip micrograph of the test circuit D is shown in Fig. 7.

A. RF Performances

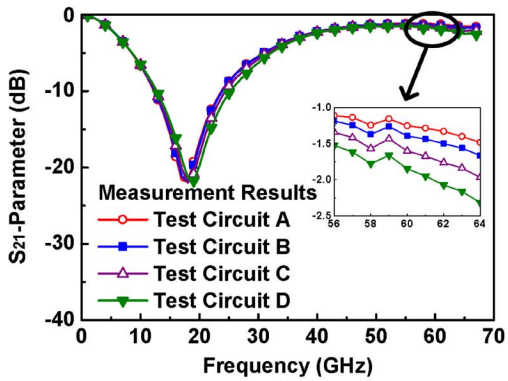
In order to extract the intrinsic characteristics of the test circuits in high frequencies, the parasitic effects of the G-S-G pads have been removed by using the L2L de-embedding technique [21]. With the on-wafer RF measurement, the S-parameters of these four test circuits have been extracted from 0 to 67 GHz. The voltage supply of $\mathrm{V_{DD}}$ ($\mathrm{V_{SS}}$) is 1 V (0 V), and the dc bias of $\mathrm{RF_{IN}}$ is 0.5 V ($\mathrm{V_{DD}}/2$). The source and load resistances to the test circuits are kept at 50 Ω. The measured $\mathrm{S_{11}}$-parameters and $\mathrm{S_{21}}$-parameters versus frequencies among the four test circuits are shown in Fig. 8(a) and (b), respectively. As shown in Fig. 8(a), these ESD protection circuits exhibit good input matching ($\mathrm{S_{11}-parameters} < -15\ \mathrm{dB}$) around 60 GHz. At 60-GHz frequency, the test circuits A, B, C, and D have about 1.2-dB, 1.4-dB, 1.6-dB, and 1.8-dB power loss, respectively.

B. ESD Robustness

The human-body-model (HBM) ESD pulses are stressed to each test circuit under positive-to-$\mathrm{V_{SS}}$ (PS), positive-to-$\mathrm{V_{DD}}$ (PD), negative-to-$\mathrm{V_{SS}}$ (NS), and negative-to-$\mathrm{V_{DD}}$ (ND) ESD stress conditions. The failure criterion is defined as the I-V characteristics seen at $\mathrm{RF_{IN}}$ shifting over 30% from its original curve after ESD stressed at every ESD test level. In other words, the leakage current under 1-V bias at $\mathrm{RF_{IN}}$ will not increase over 30% if the test circuit is not failed after ESD stresses. The HBM ESD robustness among the four test circuits with the proposed ESD protection designs are listed in Table I. The HBM ESD levels of the proposed ESD protection circuits A′, B′, C′, and D′ can achieve 0.75 kV, 1.5 kV, 2.25 kV, and 2.75 kV, respectively, which are obtained from the lowest levels among PS, PD, NS, and ND ESD tests. The HBM ESD robustness of the



(a)



(b)

Fig. 8. Measurement results of (a) S_{11}-parameters and (b) S_{21}-parameters among the four test circuits with the proposed ESD protection scheme under different device dimensions.

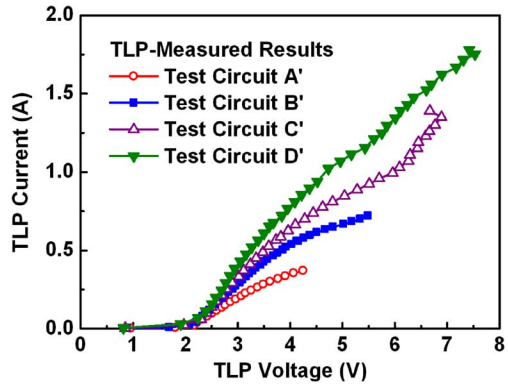


Fig. 9. TLP-measured I-V characteristics among the four test circuits with the proposed ESD protection scheme of different device dimensions under positive-to-V_{SS} tests.

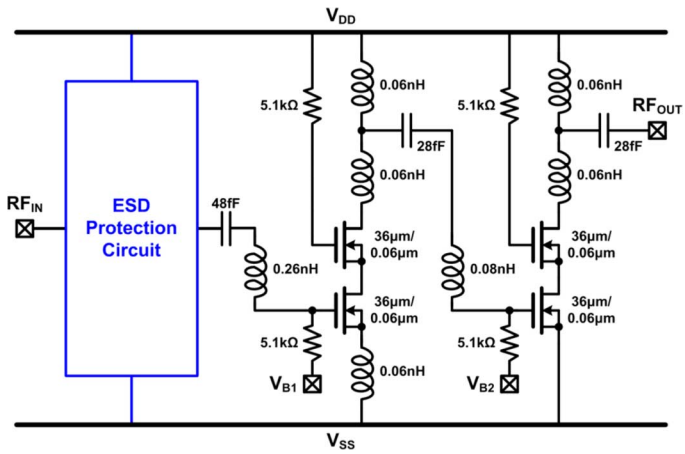


Fig. 10. Circuit schematic of 60-GHz LNA with ESD protection circuit.

test circuits is almost proportional to the sizes of ESD protection devices (SCR and D_N).

To investigate the turn-on behavior and the I-V characteristics in high-current regions of the inductor-triggered SCR, the transmission line pulsing (TLP) system with a 10-ns rise time and a 100-ns pulse width is used [22]. The TLP-measured I-V curves of the ESD protection circuits A′, B′, C′, and D′ under positive-to-V_{SS} stress conditions are shown in Fig. 9. Once ESD pulses stressed to the test circuits, all SCR devices can be quickly triggered on to discharge ESD currents. The secondary breakdown current (I_{t2}), which indicated the current-handling ability of ESD protection circuit, can also be obtained from the TLP-measured I-V curve. The test circuits A′, B′, C′, and D′ can achieve I_{t2} of 0.37 A, 0.72 A, 1.39 A, and 1.78 A, respectively. These second breakdown currents measured by TLP system are summarized in Table I. The turn-on behavior and the I_{t2} values of the ESD protection circuits can ensure the effective ESD protection capability of the proposed inductor-triggered SCR.

To evaluate the effectiveness of the proposed ESD protection circuits in faster ESD-transient events, another very fast TLP (VF-TLP) system with 0.2-ns rise time and 1-ns pulse width is also used in this study. The VF-TLP system can be used to capture the transient behavior of ESD protection circuits in the time domain of charged-device-model (CDM) ESD event [23]. The VF-TLP-measured I_{t2} of the ESD protection circuits are also listed in Table I. The tests circuits A′, B′, C′, and D′ with the RF-NMOS emulator can achieve VF-TLP-measured I_{t2} of 0.96 A, 1.72 A, 2.14 A, and 2.21 A, respectively. For comparison purpose, the tests circuits A, B, C, and D without the RF-NMOS emulator are also tested by VF-TLP system. They can achieve VF-TLP-measured I_{t2} of 1.98 A, 2.72 A, 3.08 A, and 3.71 A, respectively. The proposed inductor-triggered SCR is fast enough to be turned on under such a fast-transient pulse.

IV. Application to 60-GHz LNA

A. 60-GHz LNA Design

One 60-GHz LNA is designed in a commercial 65-nm CMOS technology for verification purpose. The metal-insulator-metal (MIM) capacitors and polysilicon resistors are available in this process.

Fig. 10 shows the schematic of the 60-GHz LNA with ESD protection circuit of inductor-triggered SCR. In the two-stage LNA design, the cascode configuration is utilized to achieve high gain performance. The common-source and common-gate NMOS transistors are all with 36-μm gate width and 0.06-μm gate length. The input matching is designed for the minimum noise figure. The output matching network is conjugately matched for the maximum gain.

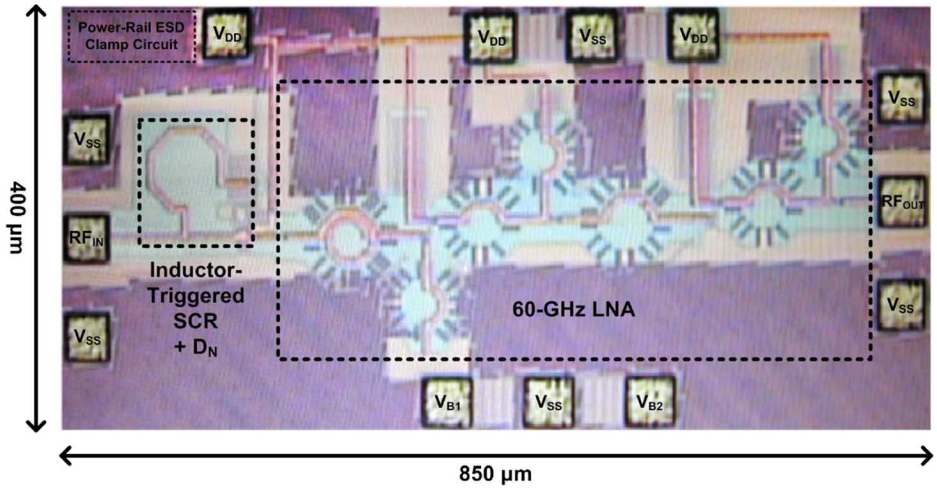


Fig. 11. Chip micrograph of 60-GHz LNA with ESD protection circuit D.

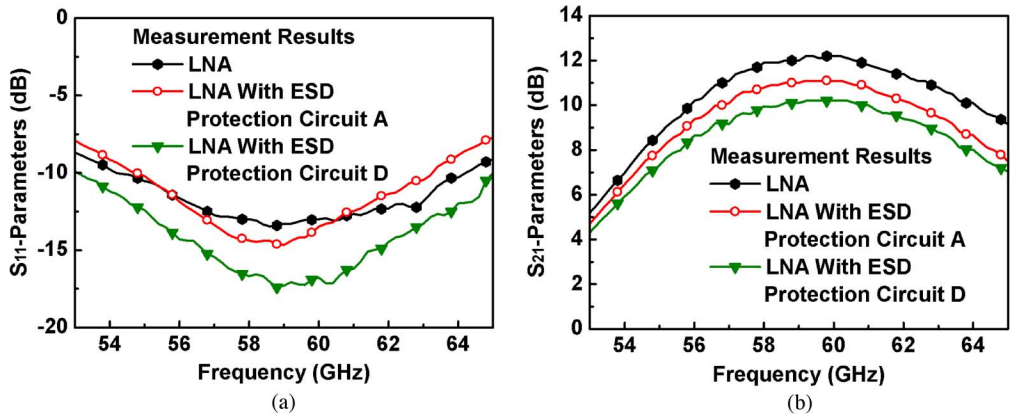


Fig. 12. Measurement results of (a) S_{11}-parameters and (b) S_{21}-parameters on 60-GHz LNA with and without ESD protection circuits.

The 60-GHz LNA circuits with ESD protection circuits A and D are included in silicon chip. Fig. 11 shows a chip photograph of the 60-GHz LNA with the ESD protection circuit D. The layout size of this circuit is $400\ \mu\mathrm{m} \times 850\ \mu\mathrm{m}$, including all testing pads and dummy layers. The dummy layers are kept away from the signal paths, so they will not influence the RF signals.

In order to verify the RF characteristics and ESD robustness, the stand-alone LNA without RF ESD protection is also fabricated for comparison. All the LNA circuits with and without ESD protection circuits are fabricated on the same wafer for comparison.

B. Experimental Results

The RF characteristics are measured on wafer through G-S-G microwave probes with 100-μm pitch. The S-parameters are measured by using the Agilent E8361A PNA network analyzer. The short-open-load-thru calibration has been done before the measurements. Each LNA circuit operates with the 1-V V_{DD} supply and draws a total current of 30 mA. The used bias voltages V_{B1} and V_{B2} are all 0.7 V. The measured S_{11}-parameters and S_{21}-parameters of the LNA circuits are shown in Fig. 12(a) and (b), respectively. With the ESD protection circuits, the peak power-gain frequencies of all LNA circuits are at $\sim$60 GHz. The input return losses for all test circuits are greater than 10 dB at 60 GHz. The power gains at 60 GHz are 11.1 dB and 10.2 dB for two ESD-protected LNA circuits, respectively, which reduced by 1.1 dB and 2 dB, as compared with the stand-alone LNA of 12.2 dB.

Under the same bias condition, the noise figures and the output power versus input power of the LNA with and without ESD protection circuits are shown in Figs. 13 and 14, respectively. The measured noise figures at 60 GHz of two ESD-protected LNA circuits are 7.5 dB and 8.6 dB, respectively, and that of the stand-alone LNA is 6.5 dB, as shown in Table II. The input 1-dB compression point $(P_{1\ \mathrm{dB}})$ of two ESD-protected LNA circuits are -11 dBm, and that of the stand-alone LNA is -12 dBm.

To compare the ESD protection capability among the LNA with and without ESD protection circuits, the RF performances of all LNA circuits after ESD stresses are re-measured. All positive-to-V_{SS}, positive-to-V_{DD}, negative-to-V_{SS}, and negative-to-V_{DD} HBM ESD stresses are zapped to RF_{IN} pad of each test circuit. The S_{21}-parameters of three LNA circuits after various ESD stresses are shown in Fig. 15(a)–(c). The power gain of the stand-alone LNA is severely degraded after 100-V HBM ESD stresses, as seen in Fig. 15(a). In contrast,

TABLE II
COMPARISON AMONG 60-GHz LNA WITH AND WITHOUT ESD PROTECTION DESIGNS IN CMOS TECHNOLOGIES

LNA	Technology	Gain (dB)	Noise Figure (dB)	HBM ESD Level (kV)	ESD Protection Circuit Area (μm x μm)
Without ESD Protection (This Work)	65-nm	12.2	6.5	< 0.1	0
With ESD Protection Circuit A (This Work)	65-nm	11.1	7.5	0.5	120 x 150
With ESD Protection Circuit D (This Work)	65-nm	10.2	8.6	3	100 x 130
With ESD Protection Diodes and Inductors in Series (Ref. [9])	130-nm	20.4	8.6	1.5	400 x 180
With ESD Protection Diodes (Ref. [10])	45-nm	23	8.5	1.25	N/A
With ESD Protection Inductor (Ref. [11])	40-nm	13	8	4.75	N/A

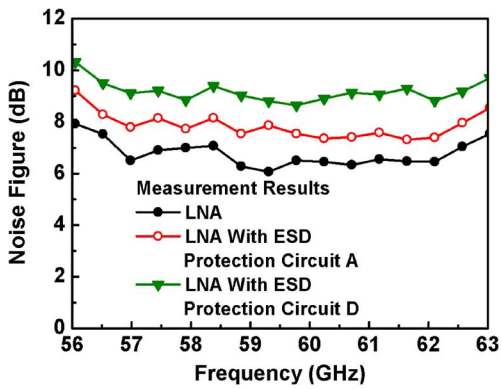


Fig. 13. Measurement results of noise figures on 60-GHz LNA with and without ESD protection circuits.

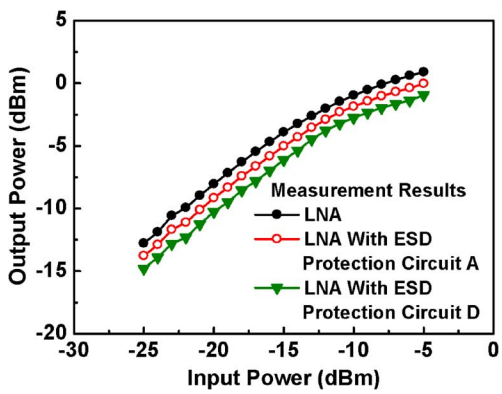


Fig. 14. Measurement results of output power versus input power on 60-GHz LNA with and without ESD protection circuits.

the power gains of the LNA with ESD protection circuit A and that with ESD protection circuit D are still excellent matching after 500-V and 3-kV HBM ESD stresses, respectively, as seen in Fig. 15(b) and (c).

C. Comparison

Table II summarizes and compares the previously reported 60-GHz ESD-protected LNA [9]–[11] and the circuits of this work. The ESD protection circuit D can provide the required

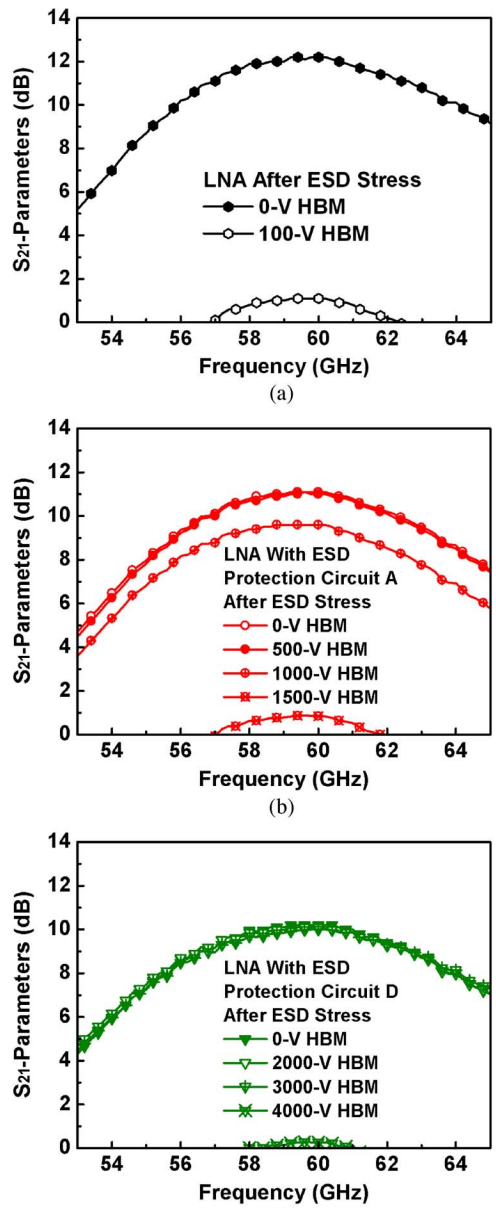


Fig. 15. Measurement results on S_{21}-parameters of (a) LNA without ESD protection, (b) LNA with ESD protection circuit A, and (c) LNA with ESD protection circuit D, after PS, PD, NS, and ND HBM ESD stresses.

2-kV HBM ESD robustness with $100 \times 130 - \mu m^2$ layout area and little RF performance degradation. Moreover, the proposed design has been implemented in cell configuration, which can be directly applied to the 60-GHz RF LNA. Therefore, the proposed ESD protection design in this paper is more suitable for RF circuit designer for them to easily apply ESD protection in the 60-GHz RF LNA.

V. Conclusion

The new ESD protection scheme with inductor-triggered SCR has been designed, fabricated, and characterized in a 65-nm CMOS process. The inductor-triggered SCR is designed to achieve low trigger voltage and high turn-on speed. Moreover, these inductor-triggered SCR can reach the input/output matching with low S_{11}-parameters and high S_{21}-parameters. These ESD protection circuits are developed to support RF circuit designers for them to easily apply ESD protection in the 60-GHz RF receiver circuits. Verified in a commercial 65-nm CMOS process, the test circuits A, B, C, and D have about 1.2-dB, 1.4-dB, 1.6-dB, and 1.8-dB power loss at 60-GHz frequency, respectively. Besides, they can sustain 0.75-kV, 1.5-kV, 2.25-kV, and 2.75-kV HBM ESD tests, respectively. The VF-TLP-measured It_2 of these test circuits are also provided, which are 0.96 A, 1.72 A, 2.14 A, and 2.21 A, respectively. The test circuits with inductor-triggered SCR have been applied to the 60-GHz LNA to confirm the ESD protection ability and to verify the RF performances. The RF performances of the LNA with ESD protection circuit A and that with ESD protection circuit D are still maintained after 500-V and 3-kV HBM ESD tests are performed, respectively. The inductor-triggered SCR can be further applied to other circuit blocks in the RF transceiver without dc blocking capacitor. Therefore, the proposed ESD protection scheme can be widely used to achieve good RF performance and high ESD robustness simultaneously.

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