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Investigation of Hot-Carrier Stress Effect on High-Frequency Performance of Laterally Diffused Metal–Oxide–Semiconductor Transistors

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The hot-carrier stress effects on the high-frequency performance characteristics of laterally diffused metal–oxide–semiconductor (LDMOS) transistors were investigated. A constant bias channel hot-carrier stress was applied at room temperature. After applying 3 h of hot-carrier stress, the on-resistance and saturation drain current degradations are 18 and 9%, respectively. However, the degradations of the cutoff frequency and maximum oscillation frequency were less than 2% when the devices were biased before the onset of quasi-saturation. In addition, we found that the degradations of high-frequency parameters are not related to the change in transconductance but to the changes in gate capacitances. Finally, *S*-parameter variations under hot-carrier stress were also examined in this study. The observations of *S*-parameter variations are important for RF power amplifier design.

1. Introduction

The rapid growth of wireless communication product markets has created a huge demand for low-cost, high-efficiency, and good-linearity RF power amplifiers. Among power devices, laterally diffused metal–oxide–semiconductor (LDMOS) transistors are the most attractive in cost and potential for improvements in performance and integration. LDMOS transistors have been widely used in RF power amplifier modules for a high frequency range up to 3.8 GHz.[1–3] Because the LDMOS used in power amplifiers is operated at a high drain voltage while carrying a high current, it could be vulnerable to hot carrier injection and trapping. Therefore, hot-carrier instability is one of the major reliability issues in an LDMOS and has widely attracted attention in recent years.[4–7] Owing to the existence of a drift region, the mechanisms of hot-carrier-induced degradation in LDMOS transistors differ substantially from that in standard complementary metal–oxide–semiconductor (CMOS) transistors. The degradation mechanism depends on the device structure and stress condition. Generally, the hot-carrier degradation is associated with the effects of hot hole/electron injection in the channel region and/or the drift region of LDMOS transistors.

For RF power circuit design, it is important to evaluate the hot-carrier stress effects on the high-frequency characteristics of power transistors to predict stress-induced circuit performance drifts. Although the hot-carrier reliability of LDMOS transistors has been investigated in many studies, there are only a few reports that address the hot-carrier stress effects on RF behaviors,[8–10] particularly on the degradation of *S*-parameters and the RF figures of merit, such as cutoff frequency (f_T) and maximum oscillation frequency (f_{max}). Previously, hot-carrier-induced f_T or *S*-parameter degradations were shown only to verify the reliability improvement of a new device structure[8,9] or compare the measurement results of different aging test methods.[10] However, the mechanisms of high-frequency parameter degradations were not discussed in detail. In this paper, we present the experimental results of the high-frequency characteristics of LDMOS transistors under hot-carrier stress. It was observed that f_T decreases and f_{max} remains almost unchanged after applying stress under the bias conditions of RF-power-amplifying applications. The degradation mechanisms of the high-frequency parameters are discussed in detail by analyzing the changes in gate capacitances. Finally, *S*-parameter variations under hot-carrier stress are also shown in this paper.

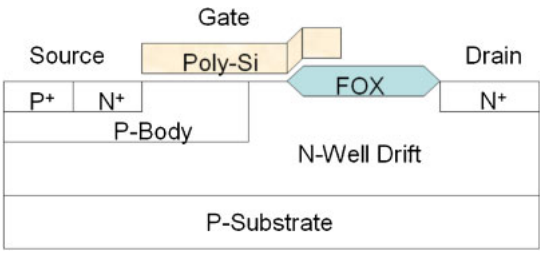

Fig. 1. (Color online) Schematic cross section of an LDMOS transistor.

2. Experiments

The n-channel LDMOS transistors used in this study were fabricated by a 0.5 μm CMOS-DMOS process with a gate oxide thickness of 135 Å.[11] The off-state breakdown voltage is about 41 V. As illustrated in Fig. 1, the devices have a lightly doped N-well drift region under the field oxide (FOX). The effective channel length and drift length are 1.1 and 2 μm, respectively. The source and p-body contacts are tied together to eliminate extra surface bond wires to reduce the source inductance and improve the RF performance in a power amplifier configuration.[12] To monitor the body current, devices with separate source and p-body contacts were also fabricated. The devices under test have a multifinger gate configuration featuring eight fingers with a total width of 80 μm.

A constant bias hot-carrier stress was applied with a gate voltage of 2.5 V and a drain voltage of 28 V at room temperature. The applied gate voltage corresponds to the maximum body current. The stress tests were interrupted periodically to measure the degradation of device electrical parameters. The *S*-parameters were measured on chip using

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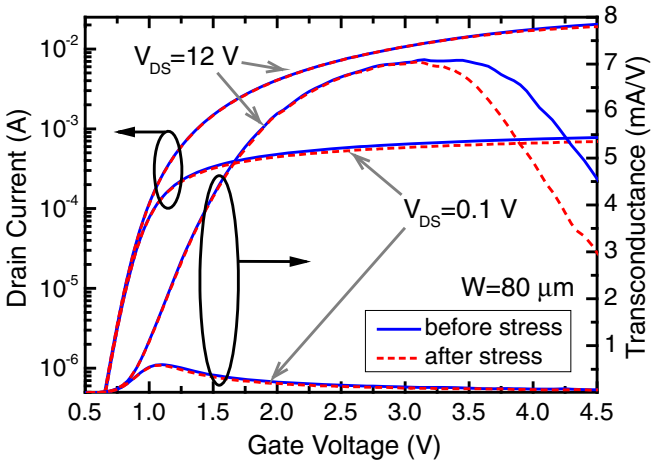
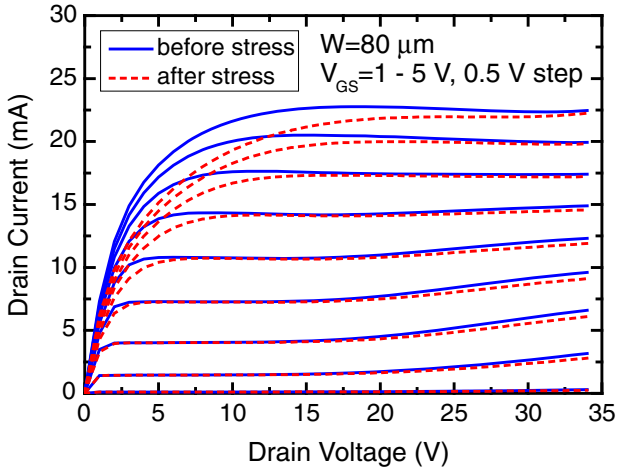


(a)



(b)

Fig. 2. (Color online) (a) I_D–V_{GS} and (b) I_D–V_{DS} characteristics of an LDMOS measured before and after applying 3 h of hot-carrier stress.

an Agilent 8510 network analyzer from 100 MHz to 15 GHz. After de-embedding the parasitic pad effects, the ac current gain (H_{21}) and unilateral power gain (U) were calculated to extract f_T and f_{max}, respectively.

3. Results and Discussion

3.1 DC characteristics

Figure 2 shows the effects of hot-carrier stress on the dc characteristics of an LDMOS. In Fig. 2(a), the threshold voltage is found to exhibit no degradation after applying stress (<0.5 mV), which means that there is no damage on the source side of the channel. When the device operates in the linear region (drain voltage $V_{DS} = 0.1$ V), the maximum value of linear transconductance ($g_{m,lin}$) shows an approximately 3% degradation, probably owing to the interface trap generation near the drain side of the channel. When the device operates in the saturation region ($V_{DS} = 12$ V), the drain current (I_D) and transconductance (g_m) degradations are not observed (<0.2%) before the quasi-saturation effect occurs ($V_{GS} < 3$ V). In this bias range, the drain current is dominated by the channel current. In addition, the pinch-off region on the drain side of the channel is created; thus, the generated interface traps in the channel would only slightly affect the carrier mobility. At high gate voltages, the device operation enters the quasi-saturation region, and I_D and g_m decrease significantly after applying stress. In this operation region, N-well drift resistivity has a large impact on the device characteristics. During hot-carrier stress, the generated interface traps in the drift region may capture the electrons and thus increase the surface scattering, leading to the reduction in carrier mobility.[4–6)]

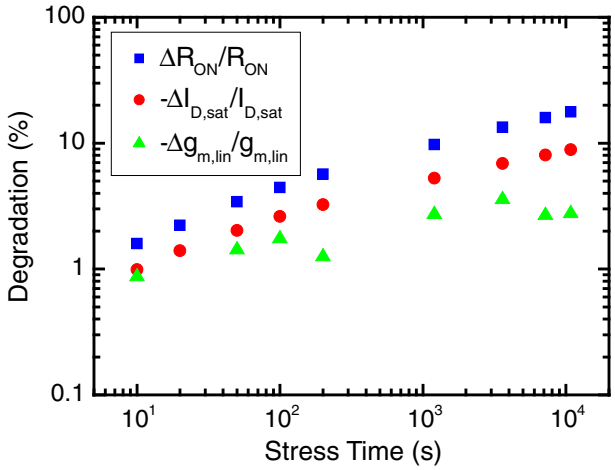


Fig. 3. (Color online) Degradations of R_{ON}, $I_{D,sat}$, and $g_{m,lin}$ with hot-carrier stress time. R_{ON} and $I_{D,sat}$ are extracted at $V_{DS} = 0.5$ and 12 V, respectively, under $V_{GS} = 5$ V. $g_{m,lin}$ is the maximum transconductance at $V_{DS} = 0.1$ V.

The severe hot-carrier-induced current degradation in the quasi-saturation region can also be observed in the device output characteristics, as depicted in Fig. 2(b). At high drain voltages, I_D degradation decreases as the current is pushed deeper in the silicon; hence, the trap-induced surface scattering also decreases. From Fig. 2(b), we extracted the on resistance (R_{ON}) and saturation drain current ($I_{D,sat}$) at $V_{DS} = 0.5$ and 12 V, respectively, under the gate voltage condition $V_{GS} = 5$ V. We found that R_{ON} increases and $I_{D,sat}$ decreases upon applying hot-carrier stress. As shown in Fig. 3, the degradations of R_{ON} and $I_{D,sat}$ are about 18 and 9%, respectively, after applying 3 h of stress; they are higher than the degradation of $g_{m,lin}$, suggesting that the stress-induced damage in the drift region is more serious than that in the channel region. In addition, the slopes of the R_{ON} and $I_{D,sat}$ curves in Fig. 3 are in the 0.3–0.4 range, which is close to that reported in ref. 4. Moens *et al.* pointed out that the hot-carrier-induced interface traps in the drift region are produced at the source-side bird's beak of the FOX when the stress condition corresponds to the maximum body current.[4)] Since the hot carriers affect the dc characteristics of an LDMOS transistor, they may also result in the degradation of high-frequency performance.

3.2 f_T and f_{max}

The gate voltage dependence of f_T under hot-carrier stress is shown in Fig. 4. The degradation of the maximum value of f_T is ~1.9% after applying 3 h of stress. This degradation is much lower than those of R_{ON} and $I_{D,sat}$, owing to the different measurement biases. This result indicates that hot-carrier instability would be less serious when the LDMOS is used in RF power amplifiers than when the LDMOS is used in power switching circuits. In addition, we found that although g_m is unchanged by the stress at the peak f_T [see

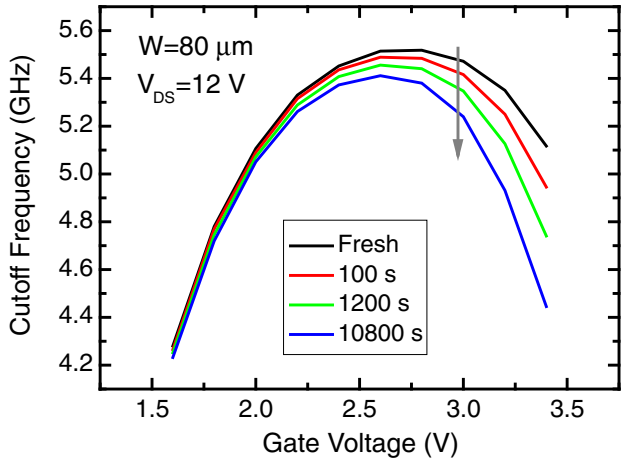


Fig. 4. (Color online) Measured cutoff frequency as a function of gate voltage for LDMOS under hot-carrier stress.

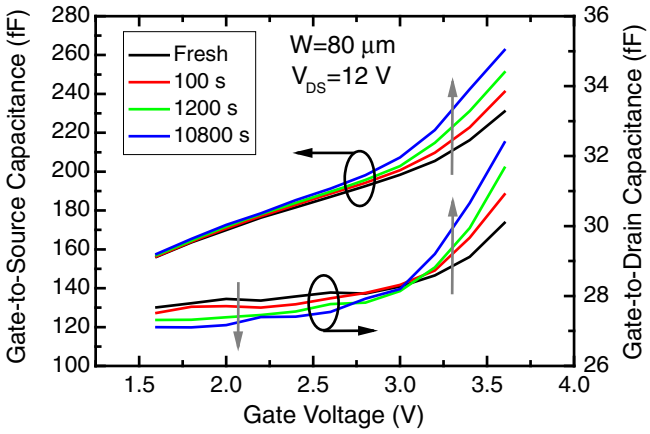


Fig. 5. (Color online) Extracted gate capacitances as a function of gate voltage for LDMOS under hot-carrier stress.

Fig. 2(a)], f_T still exhibits a small degradation. This observation is different from that in metal–oxide–semiconductor field-effect transistors (MOSFETs), where g_m plays an important role in f_T degradation.[13] The cutoff frequency can be expressed as a function of g_m and gate capacitances, that is,

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}, \quad (1)$$

where C_{gs} is the gate-to-source capacitance and C_{gd} is the gate-to-drain capacitance. Because g_m is unchanged by the stress, the degradation of f_T may be attributed to the changes in gate capacitances.

The changes in C_{gs} and C_{gd} under hot-carrier stress are shown in Fig. 5. The values of the gate capacitances are extracted from the Y-parameters at low frequencies. Before quasi-saturation ($V_{GS} < 3$ V), C_{gs} increases with increasing stress time, whereas C_{gd} decreases. The increase in C_{gs} under hot-carrier stress was also observed in MOSFET devices,[14] and this phenomenon can be explained by the change in channel surface potential owing to the negative trap charges appearing near the drain side of the channel. However, in MOSFETs, C_{gd} was nearly unchanged under hot-carrier stress as the device was operated in the saturation

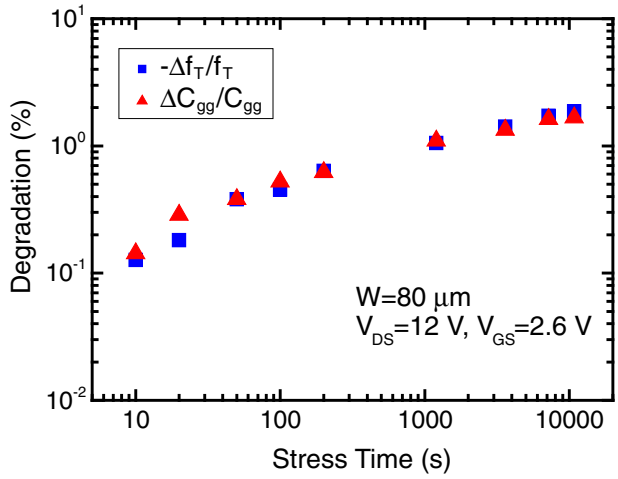


Fig. 6. (Color online) Degradations of cutoff frequency and total gate capacitance under hot-carrier stress.

region.[13,14] The different results between MOSFETs and our device are due to the existence of a drift region. In LDMOS transistors, a large part of C_{gd} comes from the drift region. The stress-induced negative interface charges in the drift region lead to positive mirror charges in the silicon, thus reducing the effective top N-well concentration. As such, the depletion layer width in the drift region increases and thus C_{gd} decreases. By plotting the degradations of cutoff frequency and total gate capacitance ($C_{gg} = C_{gs} + C_{gd}$) as functions of stress time (see Fig. 6), we found that the changes in f_T and C_{gg} are similar. This result confirms that the f_T degradation is dominated by the change in gate capacitance.

When the gate voltage increases and reaches the quasi-saturation region, both the transconductance and gate capacitance markedly change [see Figs. 2(a) and 5] owing to the increased drain resistance after stress. As a result, f_T exhibits a large stress-induced degradation at high gate voltages. It was also noted that both C_{gs} and C_{gd} increase with stress time in this bias range. In LDMOS transistors, because the inversion charges may be injected from the intrinsic MOSFET to the depleted area of the drift region, C_{gs} and C_{gd} increase with increasing gate voltage, and C_{gs} even increases over the limit of inversion.[15] The increase in gate capacitance with gate voltage may become more apparent as the drain resistance increases. Therefore, the increases in C_{gs} and C_{gd} under stress might be mainly attributed to the increased drain resistance.

Figure 7 shows the degradation of maximum oscillation frequency under hot-carrier stress. The maximum value of f_{max} is nearly unchanged with stress time (<0.5%). f_{max} can be expressed as[16]

$$f_{max} \cong \sqrt{\frac{f_T}{8\pi R_g C_{gd}}}, \quad (2)$$

where R_g is the gate resistance. Because the gate resistance is not affected by the hot carriers, we only consider the effects of f_T and C_{gd} on f_{max}, and the f_{max} degradation ($\Delta f_{max}/f_{max}$) is now written as

$$\frac{\Delta f_{max}}{f_{max}} \cong \frac{1}{2}\left(\frac{\Delta f_T}{f_T}\right) - \frac{1}{2}\left(\frac{\Delta C_{gd}}{C_{gd}}\right). \quad (3)$$

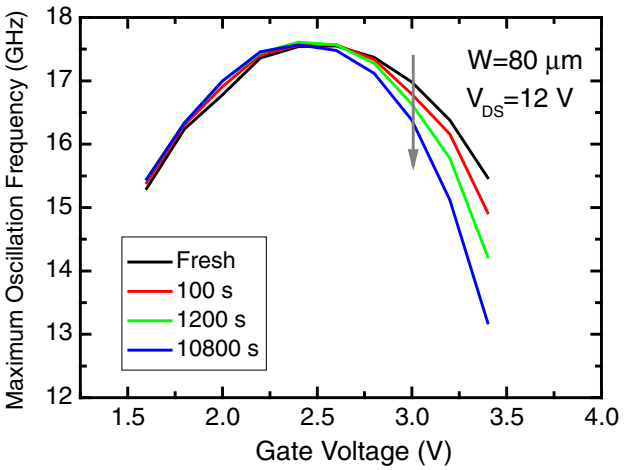


Fig. 7. (Color online) Measured maximum oscillation frequency as a function of gate voltage for LDMOS under hot-carrier stress.

After 3 h of stress, the degradations of f_T and C_{gd} are 1.9 and 2.0%, respectively, at $V_{GS} = 2.6$ V and $V_{DS} = 12$ V. Owing to the similar degradations of f_T and C_{gd}, f_{max} would not be changed by the hot carriers. At high gate voltages, large f_{max} degradations are observed owing to the obvious f_T reduction and C_{gd} enhancement.

3.3 *S*-parameters

Figure 8 shows the *S*-parameters measured before and after hot-carrier stress versus frequency. The transistor was measured at $V_{GS} = 2.6$ V and $V_{DS} = 12$ V for the maximum value of f_T. Although all *S*-parameters are affected by the hot carriers, their degradations (1.1–1.3% at 15 GHz) are not as significant as those of R_{ON} and $I_{D,sat}$. As shown in Fig. 8, the stress-induced deviations of the four *S*-parameters are similar and increase with increasing frequency. These findings differ from the results for MOSFET devices.[17,18] In the case of MOSFETs, S_{21} and S_{22} change more than S_{11} and S_{12} after applying stress. Moreover, the stress-induced deviations of S_{21} and S_{22} decrease with increasing frequency. This is because the changes in *S*-parameters are mainly attributed to the changes in the tranconductance and channel conductance of MOSFETs. In our devices, the degradations of *S*-parameters are due to the changes in C_{gs} and C_{gd}.

The observations in hot-carrier-induced *S*-parameter degradations are very important for power amplifier design. In Fig. 8(a), the reduction in S_{12} implies that the isolation of transistors is improved. Therefore, the degradation of f_{max} is less than that discussed previously. It is worthwhile to pay attention to the measured results of S_{21} and S_{22}. At low frequencies, S_{21} and S_{22} are almost unchanged. This suggests that the tranconductance and channel conductance are not affected by the stress, which is consistent with the measured dc characteristics. As the frequency increases, S_{21} and thus the voltage gain decrease gradually. Moreover, the increase in S_{22} is observed at high frequencies; this is due to not only the reduction in C_{gd} but also the increase in drain resistance. Since S_{11} and S_{22} change after applying stress, we know that the hot carriers also affect the input and output reflection coefficients of the transistors.

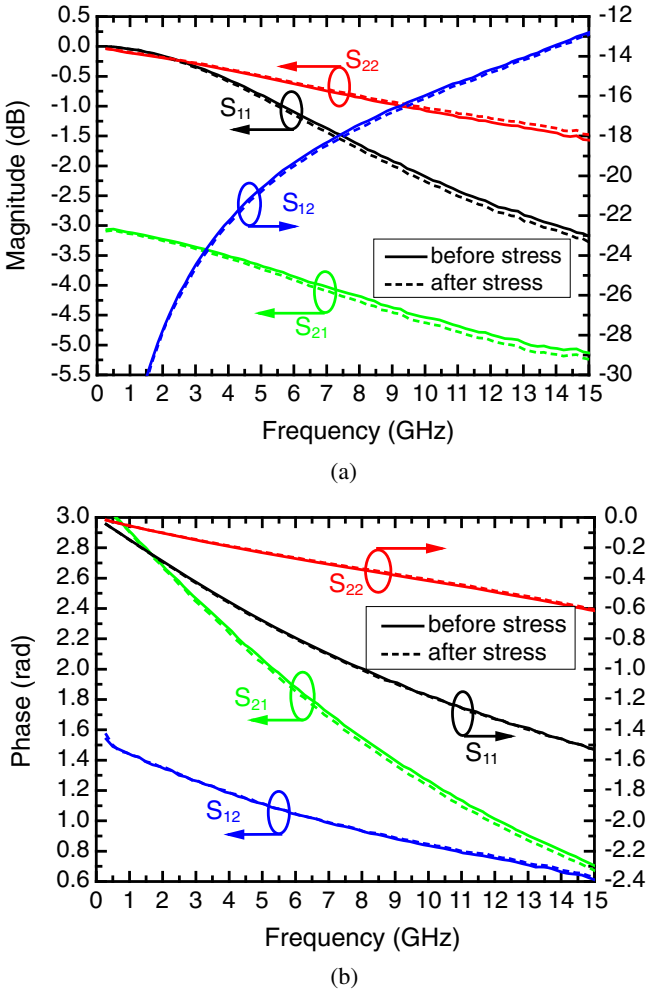


Fig. 8. (Color online) (a) Magnitudes and (b) phases of *S*-parameters before and after applying 3 h of hot-carrier stress. The measurement conditions were $V_{GS} = 2.6$ V and $V_{DS} = 12$ V.

4. Conclusions

In this work, we investigated the hot-carrier stress effects on the high-frequency performance characteristics of LDMOS transistors. After applying stress, the cutoff frequency decreases, while the maximum oscillation frequency remains almost the same when the device operates before the quasi-saturation effect occurs. This observation can be explained by the changes in C_{gs} and C_{gd} owing to the generated trap charges in the channel and drift regions, respectively. In addition, we also examined *S*-parameter variations under hot-carrier stress. Our experimental results showed that the hot carriers affect the voltage gain as well as the input and output reflection coefficients of the LDMOS transistors. However, these degradations are less than those of on-resistance and saturation drain current, indicating that the hot-carrier effect is less serious when the devices are used in RF power amplifying applications.

Acknowledgements

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