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Analytical Model of Subthreshold Current and Threshold Voltage for Fully Depleted Double-Gated Junctionless Transistor

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In this study, we derive an analytical model of an electric potential of a double-gated (DG) fully depleted (FD) junctionless (J-less) transistor by solving the two-dimensional Poisson's equation. On the basis of this two-dimensional electric potential model, subthreshold current and swing can be calculated. Threshold voltage roll-off can also be estimated with analytical forms derived using the above model. The calculated results of electric potential, subthreshold current and threshold voltage roll-off are all in good agreement with the results of technology computer aided design (TCAD) simulation. The model proposed in this paper may help in the development of a compact model for simulation program with integrated circuit emphasis (SPICE) simulation and in providing deeper insights into the characteristics of short-channel J-less transistors.
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1. Introduction

The scaling of traditional planar metal–oxide–semiconductor field-effect transistors (MOSFETs) often encounters difficult challenges owing to aggravated short-channel effects (SCEs).[1] Several types of nonplanar structure with a multiple-gated (MG) configuration have been proposed and demonstrated to be beneficial for improving immunity to SCEs.[2–4] Nonetheless, for conventional MOSFETs, ultra-shallow and abrupt junctions are still indispensable to prevent severe SCEs,[5] which in turn impose a serious issue on parasitic series resistance.[6] Recently, a novel concept of junctionless (J-less) transistors that eliminates the formation of source and drain p–n junctions altogether and has heavy doping concentration ranging from 10^{19} to 8×10^{19} cm^{-3} in the channel has been proposed to address the above dilemma.[7–10] With the scheme, superior driving performance can be achieved owing to the marked reduction in series resistance. In addition, using the ultrathin silicon body and MG device structure, J-less transistors can also be effectively turned off with comparable scaling capability to traditional MG transistors.[7] J-less transistors have also been proposed for applications in three-dimensional (3D) stacked NAND flash memories.[11,12] The n-type channel of J-less transistors can serve as a buried bit line that connects series transistors together.[11,12] A buried bit line can also prevent the complicated self-boosting program-inhibit method.[11]

Considering the great potential of J-less transistors stated above, studies of theoretical modeling are urgently needed. The purpose of this study is to provide an analytical model of subthreshold current and threshold voltage (V_{th}) for double-gated (DG) fully depleted (FD) J-less transistors. For simplicity, quantum effects arising from ultrathin channels are not taken into account in this work. The organization of this paper is as follows. In §2, we derive an analytical model of electric potential by solving two-dimensional (2D) Poisson's equation. In §3, we calculate subthreshold current and subthreshold swing using 2D electric potential. In §4, we discuss the characteristics of V_{th} roll-off. Finally, we present the conclusions drawn in this study in §5.

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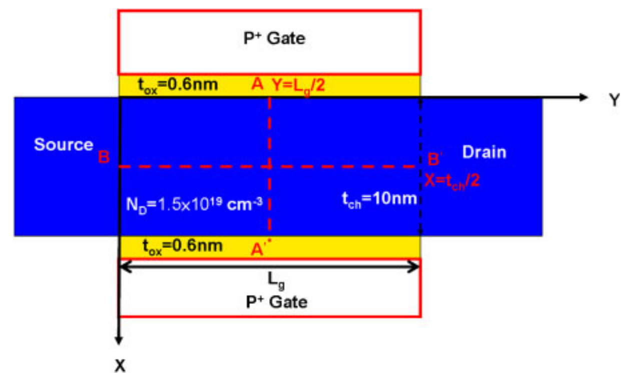

Fig. 1. (Color online) Schematic diagram of the DG FD J-less transistor with P$^+$ poly-gate investigated in this work. t_{ch}, t_{ox}, and L_g are the silicon channel thickness, effective gate oxide thickness, and channel length, respectively. $N_D = 1.5 \times 10^{19}$ cm^{-3} is the homogeneous doping concentration across the source/drain and channel.

2. Solution of 2D Poisson's Equation

Figure 1 shows a schematic diagram of a DG FD J-less transistor. A P$^+$ polycrystalline silicon (poly-Si) gate is used in our calculation of a suitable V_{th}. The X- and Y-axes indicating the gate-to-gate and source-to-drain directions, respectively, are also shown in the figure with the origin set at the intersection of the source and front-gate oxide/channel interface. In the subthreshold region, the silicon film is fully depleted and 2D Poisson's equation can be written as

$$\frac{\partial^2 \Phi(x,y)}{\partial x^2} + \frac{\partial^2 \Phi(x,y)}{\partial y^2} = \frac{-qN_D}{\varepsilon_{si}}, \tag{1}$$

where Φ is the electric potential, ε_{si} is the dielectric constant of silicon, q is the electric charge, and N_D is the homogeneous doping concentration across the source, drain, and channel regions. N_D is fixed at 1.5×10^{19} cm^{-3} in this work. The boundary conditions necessary to solve 2D Poisson's equation are listed below:

$$\Phi(t_{ch}, y) + t_{ox}\frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{\partial \Phi(x,y)}{\partial x}\bigg|_{x=t_{ch}} = V_g - V_{fb}, \tag{2}$$

$$\Phi(0, y) - t_{ox}\frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{\partial \Phi(x,y)}{\partial x}\bigg|_{x=t_{ch}} = V_g - V_{fb}, \tag{3}$$

$$\Phi(x, 0) = V_s, \tag{4}$$

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$$\Phi(x, L_g) = V_s + V_D. \tag{5}$$

In this study, fixed oxide charges at oxide/silicon interfaces are neglected. In eqs. (2)–(5), ε_{ox} is the dielectric constant of the oxide. L_g, t_{ch}, and t_{ox} are the effective gate length, silicon channel film thickness, and gate oxide thickness, respectively. V_g, V_D, and V_s are the applied voltages for the gate, drain, and source, respectively. V_{fb} is the flatband voltage. To simplify the situation, we treat the gate oxide region as an equivalent Si region[13–15] by multiplying the gate oxide thickness by $(\varepsilon_{si}/\varepsilon_{ox})$. Then, eqs. (2) and (3) are respectively converted into

$$\Phi(x,y)|_{x=t_{ch}+\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox}} = V_g - V_{fb}, \tag{6}$$

$$\Phi(x,y)|_{x=-\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox}} = V_g - V_{fb}. \tag{7}$$

Next, to solve eq. (1), 2D Poisson's equation is separated into the 1D Poisson's equation and 2D Laplace's equation as

$$\frac{\partial^2 \Phi_1(x)}{\partial x^2} = \frac{-qN_D}{\varepsilon_{si}}, \tag{8}$$

$$\frac{\partial^2 \Phi_2(x,y)}{\partial x^2} + \frac{\partial^2 \Phi_2(x,y)}{\partial y^2} = 0, \tag{9}$$

$$\Phi(x,y) = \Phi_1(x) + \Phi_2(x,y), \tag{10}$$

where Φ_1 and Φ_2 are the solutions of the 1D Poisson's and 2D Laplace's equations, respectively.

The 1D solution Φ_1, which satisfies the boundary conditions eqs. (6) and (7), can be expressed as

$$\Phi_1(x) = \frac{-qN_D}{2\varepsilon_{si}}x^2 + a_1 x + a_2, \tag{11}$$

$$a_1 = \frac{-2V_{FB} + \dfrac{N_D q t_{ox}^2 \varepsilon_{si}}{2\varepsilon_{ox}^2} + \dfrac{N_D q\left(t_{ch} + \dfrac{t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}\right)^2}{2\varepsilon_{si}}}{t_{ch} + \dfrac{2t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}}, \tag{11a}$$

$$a_2 = \frac{\left(-V_{FB} + V_g + \dfrac{N_D q t_{ox}^2 \varepsilon_{si}}{2\varepsilon_{ox}^2}\right)\left(t_{ch} + \dfrac{t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}\right)}{t_{ch} + \dfrac{2t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}} + \frac{t_{ox}\varepsilon_{si}\left(-V_{FB} + V_g + \dfrac{N_D q\left(t_{ch} + \dfrac{t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}\right)^2}{2\varepsilon_{si}}\right)}{\varepsilon_{ox}\left(t_{ch} + \dfrac{2t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}\right)} = V_g + a_3,$$

$$a_3 = \frac{\left(-V_{FB} + \dfrac{N_D q t_{ox}^2 \varepsilon_{si}}{2\varepsilon_{ox}^2}\right)\left(t_{ch} + \dfrac{t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}\right)}{t_{ch} + \dfrac{2t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}} + \frac{t_{ox}\varepsilon_{si}\left(-V_{FB} + \dfrac{N_D q\left(t_{ch} + \dfrac{t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}\right)^2}{2\varepsilon_{si}}\right)}{\varepsilon_{ox}\left(t_{ch} + \dfrac{2t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}\right)}. \tag{11b}$$

By using the separation method,[16] the solution of the 2D Laplace's equation Φ_2 can be expressed as

$$\Phi_2(x,y) = \sum_{n=1}^{\infty}\left\{G_n \sinh\left(\frac{n\pi}{t_{eff}}y\right) + H_n \sinh\left[\frac{n\pi}{t_{eff}}(L_g - y)\right]\right\} \times \sin\left[\frac{n\pi}{t_{eff}}\left(x + \frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox}\right)\right], \tag{12}$$

$$\begin{aligned} G_n = {} & \frac{2}{n\pi}\operatorname{csch}\left(\frac{L_g n\pi}{t_{eff}}y\right)\Bigg\{(a_2 - V_D) \times [-1 + \cos(n\pi)] \\ & + \frac{2a}{(n\pi)^2\varepsilon_{ox}}\operatorname{csch}\left(\frac{L_g n\pi}{t_{eff}}y\right)\{[n\pi t_{ox}\varepsilon_{si} + n\pi(t_{eff}\varepsilon_{ox} - t_{ox}\varepsilon_{si})\cos(n\pi) - t_{eff}\varepsilon_{ox}\sin(n\pi)]\} \\ & + \frac{2qN_D}{(n\pi)^3 t_{eff}\varepsilon_{si}}\operatorname{csch}\left(\frac{L_g n\pi}{t_{eff}}y\right)\left\{\frac{(n\pi t_{ox}\varepsilon_{si})^2 t_{eff}}{\varepsilon_{ox}^2}[1 - \cos(n\pi)] + \frac{2n\pi t_{eff}^2 t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}[n\pi\cos(n\pi) - \sin(n\pi)]\right\} \\ & + t_{eff}^3[-2 + (2 - (n\pi)^2)\cos(n\pi) + 2n\pi\sin(n\pi)]\Bigg\}, \end{aligned} \tag{12a}$$

$$\begin{aligned} H_n = {} & \frac{2}{n\pi}\operatorname{csch}\left(\frac{L_g n\pi}{t_{eff}}y\right)\Bigg\{a_2 \times [-1 + \cos(n\pi)] \\ & + \frac{2a}{(n\pi)^2\varepsilon_{ox}}\operatorname{csch}\left(\frac{L_g n\pi}{t_{eff}}y\right)[n\pi t_{ox}\varepsilon_{si} + n\pi(t_{eff}\varepsilon_{ox} - t_{ox}\varepsilon_{si})\cos(n\pi) - t_{eff}\varepsilon_{ox}\sin(n\pi)] \\ & + \frac{2qN_D}{(n\pi)^3 t_{eff}\varepsilon_{si}}\operatorname{csch}\left(\frac{L_g n\pi}{t_{eff}}y\right)\left\{\frac{(n\pi t_{ox}\varepsilon_{si})^2 t_{eff}}{\varepsilon_{ox}^2}[1 - \cos(n\pi)] + \frac{2n\pi t_{eff}^2 t_{ox}\varepsilon_{si}}{\varepsilon_{ox}}[n\pi\cos(n\pi) - \sin(n\pi)]\right\} \\ & + t_{eff}^3[-2 + (2 - (n\pi)^2)\cos(n\pi) + 2n\pi\sin(n\pi)]\Bigg\}, \end{aligned} \tag{12b}$$

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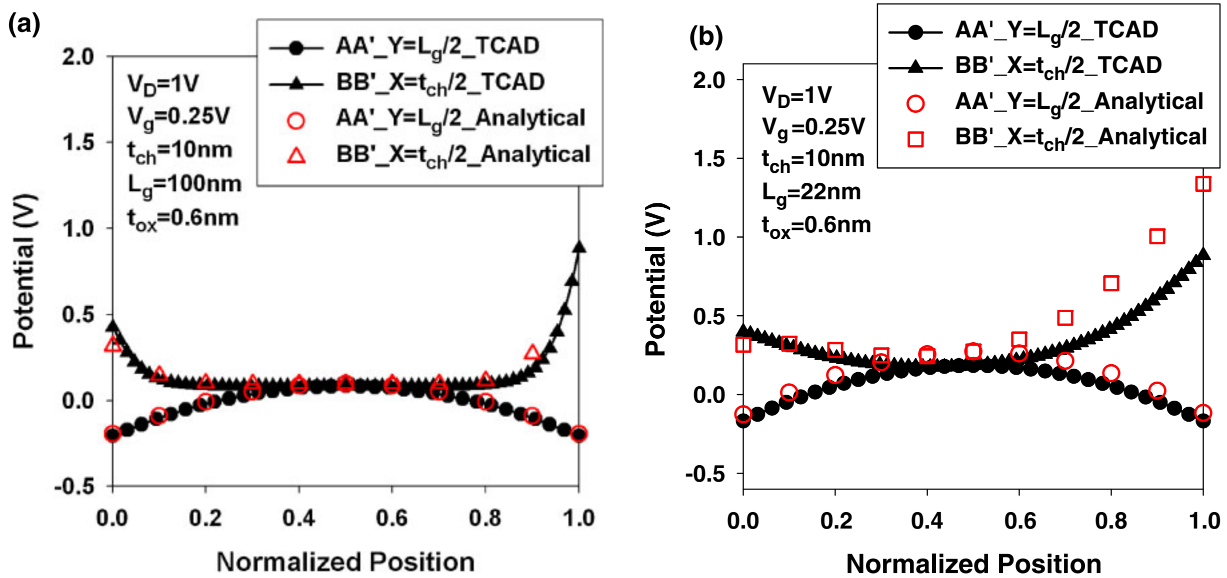

Fig. 2. (Color online) Comparison of analytical electric potentials and TCAD simulation results for (a) long ($L_g = 100$ nm)- and (b) short ($L_g = 22$ nm)-channel devices.

$$t_{\rm eff} = t_{\rm ch} + 2\frac{\varepsilon_{\rm si}}{\varepsilon_{\rm ox}} t_{\rm ox}, \tag{12c}$$

where G_n and H_n are respectively determined by the boundary conditions eqs. (4) and (5), and Φ_2 is equal to zero at the top and bottom boundaries.

To verify the above-mentioned forms, we compare the calculated results with the results of the technology computer aided design (TCAD) simulation. With focus on the electrostatic characteristics of DG FD J-less transistors, basic models, such as the Poisson's equation, continuity equation, drift-diffusion model, and constant mobility models, are applied to the 2D TCAD simulation tool "ISE TCAD Rel. 10.0 DESSIS".[17] Figures 2(a) and 2(b) show such comparisons on the device with L_g values of 100 and 22 nm, respectively. Note that A–A′ and B–B′ (see Fig. 1) refer to the perpendicular and parallel lines, respectively, with respect to the source-to-drain direction. Good agreements between the TCAD numerical simulation results[17] and the analytical solutions of the electric potential along the two lines A–A′ and B–B′ are obtained. Note that, in the long-channel case ($L_g = 100$ nm) shown in Fig. 2(a), in the middle of the channel (along the y-direction), the potential is nearly constant and close to its minimum at $x = t_{\rm ch}/2$. Results of the calculation indicate that $\Phi_2(x, y)$ is small and can be neglected in the middle region of a long-channel device and that the potential is mainly determined by $\Phi_1(x)$ in eq. (10).

3. Subthreshold Current and Swing

With the analytical electric potential solution, subthreshold current can be written as[13,14]

$$I_{\rm ds} = \frac{q\mu W(kT/q)[1-\exp(-V_{\rm ds}/kT)]}{\displaystyle\int_0^{L_g} dy \Big/ \int_0^{t_{\rm ch}} n_{\rm i}\exp[q\Phi(x,y)/kT]\,dx}, \tag{13}$$

where μ, W, and kT/q are the effective carrier mobility, channel width, and thermal voltage, respectively. Subthreshold current is mainly limited by the potential minimum along the transport direction,[16] which is assumed to be $\Phi(x, y_{\rm min})$ located at $y = y_{\rm min}$. It can then be simplified to

$$I_{\rm ds} = \frac{q\mu W(kT/q)[1-\exp(-V_{\rm ds}/kT)]}{\displaystyle\int_0^{L_g} \frac{dy}{\displaystyle\int_0^{t_{\rm ch}} n_{\rm i}\exp[q\Phi(x,y_{\rm min})/kT]\,dx}}. \tag{14}$$

According to a previous work,[16] two assumptions are made in our calculation. First, the first Fourier series term of eq. (12) is sufficient to predict the electric potential at $y = y_{\rm min}$. Second, $\sinh(x) \approx 0.5 \times \exp(x)$ can be used if $L_g\pi > t_{\rm ch}$. On the basis of these two approximations, eq. (12) can be simplified to

$$\Phi_2(x,y) = \sin\left[\frac{\pi}{t_{\rm ch}}\left(x + \frac{\varepsilon_{\rm si}}{\varepsilon_{\rm ox}} t_{\rm ox}\right)\right] \times \left\{G_1' \exp\left[\frac{(y-L_g)\pi}{t_{\rm ch}}\right] + H_1' \exp\left(\frac{-y\pi}{t_{\rm ch}}\right)\right\}, \tag{15}$$

$$G_1' = \sinh\left(\frac{\pi}{t_{\rm ch}} L_g\right) \times G_1, \tag{15a}$$

$$H_1' = \sinh\left(\frac{\pi}{t_{\rm ch}} L_g\right) \times H_1. \tag{15b}$$

Furthermore, by setting $\partial\Phi_2(x, y)/\partial y = 0$, the location of channel potential minimum, $y_{\rm min}$, can be expressed as

$$y_{\rm min} = \frac{L_g}{2} - \frac{t_{\rm ch}}{2\pi}\ln\left(\frac{G_1}{H_1}\right). \tag{16}$$

Combining eqs. (10), (14), and (16), the calculated subthreshold currents at $L_g = 22$ and 100 nm at $V_D = 0.1$ and 1 V are plotted in Figs. 3(a)–3(d). Again, the calculated results are quite close to the results of TCAD simulation. Figure 4 shows subthreshold swing as a function of L_g, ranging from 100 to 22 nm. The results are quite close to the theoretical limit of 60 mV/decade, owing to the ultrathin silicon film ($t_{\rm ch} = 10$ nm), and are also in good agreement with the results of TCAD simulation.

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Fig. 3. (Color online) Comparison of analytical subthreshold currents and TCAD simulation results for long-channel device ($L_g = 100$ nm) measured at V_D values of (a) 0.1 and (b) 1 V and short-channel device ($L_g = 22$ nm) measured at V_D values of (c) 0.1 and (d) 1 V.

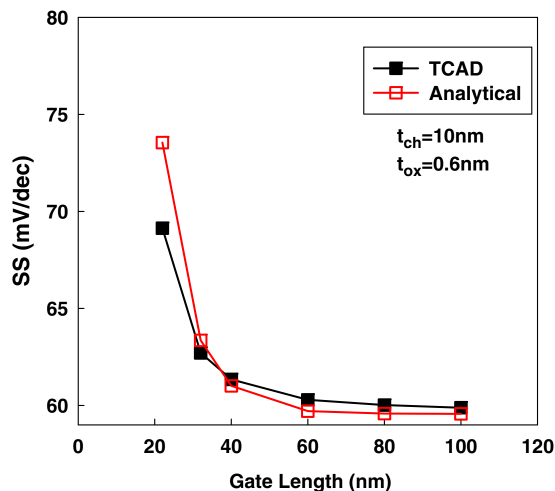

Fig. 4. (Color online) Comparison of analytical subthreshold swings for different channel lengths with TCAD simulation results.

4. Threshold Voltage Roll-Off

Although V_{th} can be directly extracted from the subthreshold current in eq. (14) by the constant-current method, this approach cannot provide much physical insight into DG FD J-less transistors. Therefore, a simple analytical V_{th} model is addressed here. As discussed above, subthreshold current is dominated by the electric potential minimum $\Phi(x, y_{min})$. Moreover, along the direction normal to the carrier transport direction, subthreshold current is determined by the location of the maximum amount of conduction electrons, and its electric potential is denoted as $\Phi(x_{max}, y_{min})$, where x_{max} is the depth from the front-gate oxide. Different from that of the traditional inversion-mode DG device in which $\Phi(x_{max}, y_{min})$ is situated close to the interface of the gate oxide and the silicon channel, the $\Phi(x_{max}, y_{min})$ of a DG FD J-less transistor device is located in the middle of a silicon channel, as shown in Fig. 2. Therefore, in the following derivation, $\Phi(x_{max}, y_{min})$ is replaced with $\Phi(0.5 \times t_{ch}, y_{min})$.

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Moreover, the electron density at $\Phi = \Phi(0.5 \times t_{ch}, y_{min})$ is equal to

$$n_i \exp\left[\frac{q\Phi(0.5 \times t_{ch}, y_{min})}{kT}\right], \tag{17}$$

where n_i is the intrinsic carrier concentration. The V_{th} of a DG FD J-less transistor can be defined as

$$V_{th} \equiv V_g \quad \text{when } \Phi(0.5 \times t_{ch}, y_{min}) = \left(\frac{kT}{q}\right)\ln\left(\frac{1}{M_{cri}}\frac{N_D}{n_i}\right), \tag{18}$$

where $M_{cri} \times n_i$ is the critical value of electron density which could be determined by comparing V_{th} in eq. (17) with that obtained by the constant-current method for a long-channel device. Later, we will show that $M_{cri} \times n_i$ is typically about one or two orders in magnitude lower than the doping density (N_D). In the long-channel case, as has been pointed out at the end of §2, $\Phi_2(x, y)$ in eq. (10) can be neglected in the middle of a channel; therefore, solving the 1D Poisson's equation is sufficient to predict subthreshold current. On the basis of eqs. (10) and (11), $\Phi(x_{max}, y_{min})$ can be simplified to

$$\Phi(0.5 \times t_{ch}, y_{min}) = \Phi_1\left(\frac{t_{ch}}{2}\right) = \frac{-qN_D}{2\varepsilon_{si}}\left(\frac{t_{ch}}{2}\right)^2 + a_1\frac{t_{ch}}{2} + a_2. \tag{19}$$

Combining eqs. (11), (18), and (19), the V_{th} of a long-channel device can be expressed as

$$V_{th,long} = \left(\frac{kT}{q}\right)\ln\left(\frac{1}{M_{cri}}\frac{N_D}{n_i}\right) - \text{con1} - \text{con2} - \text{con3}, \tag{20}$$

$$\text{con1} = \frac{-qN_D}{2\varepsilon_{si}}\left(\frac{t_{ch}}{2}\right)^2, \tag{20a}$$

$$\text{con2} = a_1 \times \frac{t_{ch}}{2}, \tag{20b}$$

$$\text{con3} = a_3. \tag{20c}$$

For short-channel devices, only solving the 1D Poisson's equation is not sufficient. Therefore, combined with eqs. (16)–(18), and (20), the V_{th} of short-channel devices can be expressed as

$$V_{th,short} = \frac{V_{th,long}}{1 - \frac{\pi}{8}\sin\left[\frac{\pi}{t_{ch}}\left(\frac{t_{ch}}{2} + \frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox}\right)\right] \times \exp\left(-\frac{\pi L_g}{2t_{ch}}\right)} + \frac{-\frac{\pi}{8}\text{con3} + \left[2(\text{con4} + \text{con5} + \text{con6}) - \frac{4V_D}{\pi}\right]\sin\left[\frac{\pi}{t_{ch}}\left(\frac{t_{ch}}{2} + \frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox}\right)\right] \times \exp\left(-\frac{\pi L_g}{2t_{ch}}\right)}{1 - \frac{\pi}{8}\sin\left[\frac{\pi}{t_{ch}}\left(\frac{t_{ch}}{2} + \frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox}\right)\right] \times \exp\left(-\frac{\pi L_g}{2t_{ch}}\right)}, \tag{21}$$

$$\text{con4} = \frac{2a(2t_{ox}\varepsilon_{si} - t_{eff}\varepsilon_{si})}{\pi\varepsilon_{ox}}, \tag{21a}$$

$$\text{con5} = \frac{2N_D q\left[(-4 + \pi^2)t_{eff}^2 - \frac{2\pi^2 t_{eff}t_{ox}\varepsilon_{si}}{\varepsilon_{ox}} + \frac{2\pi^2 t_{eff}^2\varepsilon_{si}^2}{\varepsilon_{ox}^2}\right]}{\pi^3\varepsilon_{si}}, \tag{21b}$$

$$\text{con6} = \frac{-4(V_{bi} - V_D)}{\pi}. \tag{21c}$$

Results of V_{th} estimated using eqs. (20) (for $L_g = 100$ nm) and (21) (for $L_g < 100$ nm) are shown in Fig. 5. By the constant-current method in which V_{th} is defined as the gate voltage at a drain current of $300\,\text{nA} \times W/L_g$,[13,14] a set of V_{th} values are also extracted by TCAD simulation and put into the same figure for comparison. Note that, in the figure, the V_{th} of the transistor with $L_g = 100$ nm estimated with eq. (20) is assumed to be the same as that extracted by the constant-current method, and $M_{cri} \times n_i$ in eq. (20) is consequently found to be equal to $(1/60)N_D$. It is seen that the simulated data actually coincide well with our analytical predictions. From eq. (21), it is understood that V_{th} roll-off can be significantly improved by increasing the ratio of L_g/t_{ch} considering the $\exp(-\pi L_g/2t_{ch})$ term in the denominators of the first and second terms of the equation. The V_{th} roll-off characteristics of the transistors with $t_{ch} = 8$, 10, 12, and 15 nm measured at $V_D = 0.1$ and 1 V are shown in Figs. 6(a) and 6(b), respectively, in which delta V_{th} is defined as the V_{th} difference between the short-channel transistors and that with $L_g = 100$ nm. As can be seen in the figures, the analytical model can well describe the trend of the enhanced V_{th} roll-off with increasing t_{ch}. Nonetheless, the difference

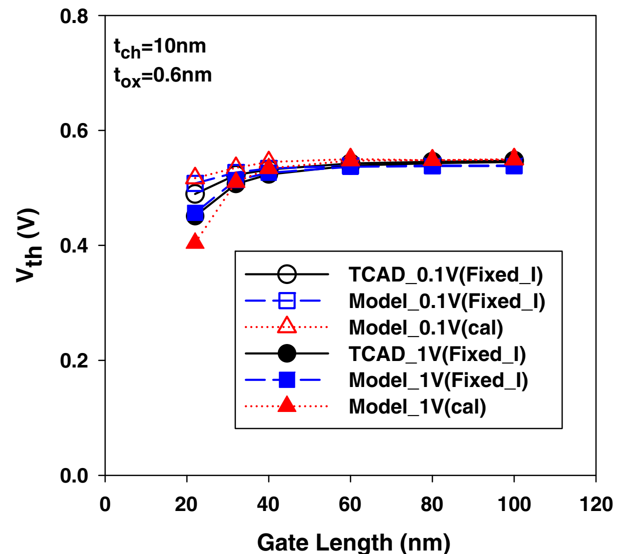

Fig. 5. (Color online) Comparison of analytical threshold voltages for different channel lengths with TCAD simulation results.

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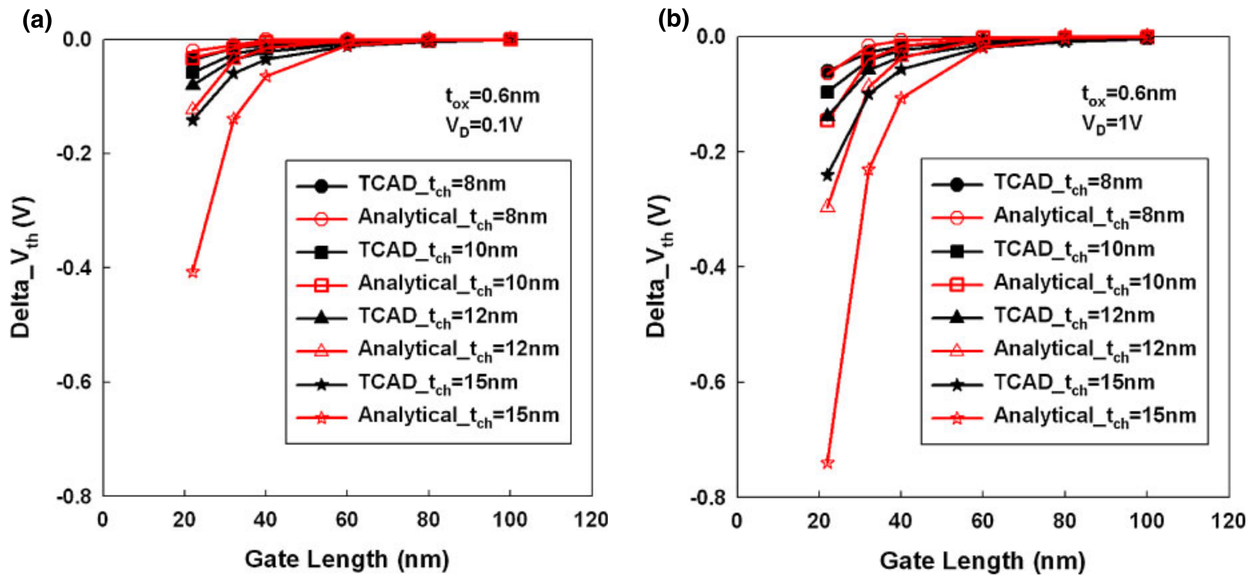

Fig. 6. (Color online) Comparison of analytical V_{th} roll-off for $t_{ch} = 8$, 10, 12, and 15 nm with TCAD simulation results at V_D values of (a) 0.1 and (b) 1 V.

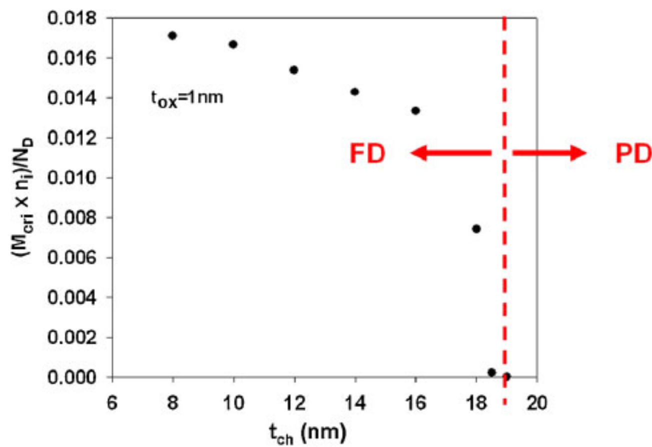

Fig. 7. (Color online) $M_{cri} \times n_i/N_D$ versus t_{ch}. As t_{ch} is larger than 19 nm, the DG device becomes PD.

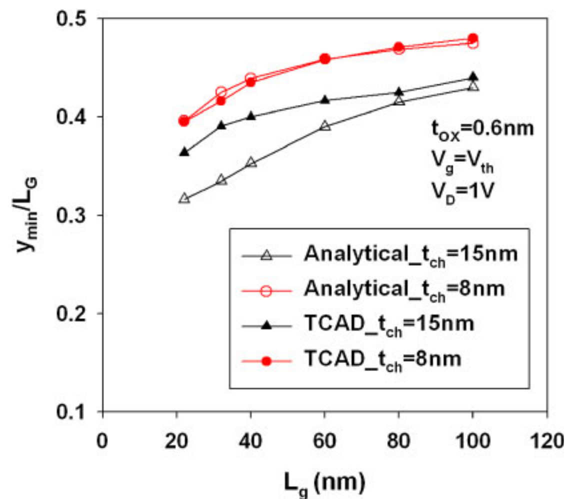

Fig. 8. (Color online) Location of y_{min} estimated with eq. (16) and TCAD simulation for devices with $t_{ch} = 8$ and 15 nm. Smaller y_{min} means a location closer to the source.

between the analytical and simulation results in the short-channel regime becomes significant as t_{ch} increases. The reason for such deviation will be discussed later on.

Next, it is worth commenting on $M_{cri} \times n_i$, which is actually the carrier concentration at $x = 0.5\,t_{ch}$ in the long-channel device at $V_g = V_{th}$. This value is typically much smaller than N_D, an indication of the fully depleted condition of the channel. However, it is not constant and is mainly dependent on t_{ch}, t_{ox}, and N_D. Since V_{th} is usually determined by the constant-current method, theoretically $M_{cri} \times n_i$ would decrease with increasing t_{ch}, thereby turning off the additional contribution of current components conducted in the middle of the channel. Such a trend is shown in Fig. 7. $M_{cri} \times n_i$ is about $(1/60)N_D$ for $t_{ch} = 10$ nm and $(1/58)N_D$ for $t_{ch} = 8$ nm. Nonetheless, as t_{ch} is increased, the middle portion of the channel becomes difficult to deplete and eventually the device becomes partially depleted (PD) because t_{ch} is sufficiently large. In the case shown in Fig. 7, the maximum t_{ch} under the FD condition is 19 nm. When devices become PD, the quasi-neutral region in the channel would conduct an extremely high current that cannot be turned off by adjusting gate bias. In other words, the current level used to define V_{th} is screened out by the substantial leakage and loses its significance in defining V_{th}. The essential role played by t_{ch} for the successful operation of J-less transistors is evident.

Figures 4 and 6 indicate that the differences in SS and delta V_{th} between the results calculated using the analytical model and TCAD simulation become significant at a small L_g because t_{ch} is large. Such observation is attributed to the error in determining y_{min} using eq. (16). In Fig. 8, the y_{min} values in the middle channel at $V_g = V_{th}$ and $V_D = 1$ V calculated using the analytical model and TCAD simulation are shown as functions of L_g. It is seen that y_{min} becomes closer to the source as the device becomes shorter, primarily owing to the penetration of electric field with the applied drain voltage. At t_{ch} of 8 nm, the results obtained using the analytical model are quite consistent with those of TCAD

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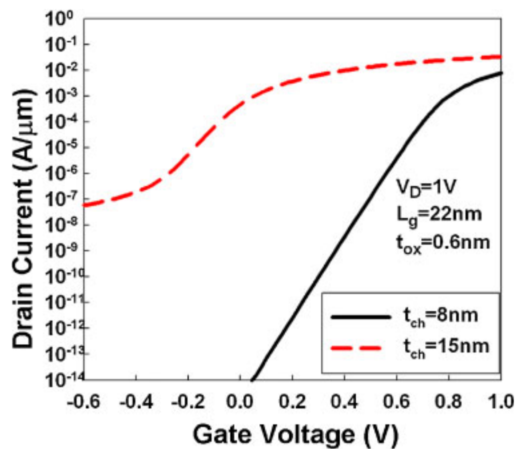

Fig. 9. (Color online) Comparison of transfer characteristics of transistors with t_{ch} values of 8 and 15 nm and L_g of 22 nm, operating at $V_D = 1$ V. Note that the transistor with t_{ch} of 15 nm suffers from high leakage current.

simulation. Nonetheless, the location of the y_{min} predicted using the analytical model is much closer to the source than that estimated by the TCAD simulation, implying that a much higher subthreshold leakage would conduct through the middle channel and thus a lower SS and a higher V_{th} roll-off resulted. Such disparity indicates that the assumption made in acquiring eq. (16) is not sufficient because t_{ch} is large. As mentioned in §3, only the first terms of the Fourier series in eq. (12), i.e., G_1 and H_1, are considered. This could greatly simplify the form of y_{min} but is not satisfactory because t_{ch} is large. Fortunately, for practical applications, t_{ch} should not be so large considering the poor subthreshold characteristics (Fig. 9). The analytical model developed in this work is still useful for probing and designing J-less devices.

5. Conclusions

We have investigated and analytically modeled the subthreshold current and V_{th} roll-off characteristics of DG FD J-less transistors by solving 2D Poisson's equation. The results of the derived analytical forms show good agreement with results of the numerical analysis by TCAD. With an ultrathin silicon film ($t_{ch} \leqq 10$ nm) and strong DG control, the subthreshold swing of the DG FD J-less transistors is quite close to the theoretical limit of 60 mV/decade. The analytical forms in both long- and short-channel cases of V_{th} with useful physical insights are also derived. The V_{th} data estimated using these analytical forms also coincide well with those extracted by the constant-current method. The results of V_{th} as a function of L_g with various silicon channel thicknesses, shown in Figs. 6(a) and 6(b) also unambiguously points out that V_{th} roll-off can be significantly suppressed by increasing the ratio of L_g/t_{ch}.

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1) C. H. Wann, K. Noda, T. Tanaka, M. Yoshida, and C. Hu: IEEE Trans. Electron Devices **43** (1996) 1742.
2) F. L. Yang, H. Y. Chen, F. C. Chen, C. C. Huang, C. Y. Chang, H. K. Chiu, C. C. Lee, C. C. Chen, H. T. Huang, C. J. Chen, H. J. Tao, Y. C. Yeo, M. S. Liang, and C. Hu: IEDM Tech. Dig., 2002, p. 255.
3) B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C. Y. Yang, C. Tabery, C. Ho, Q. Xiang, T. J. King, J. Bokor, C. Hu, M. R. Lin, and D. Kyser: IEDM Tech. Dig., 2002, p. 251.
4) S. Kobayashi, M. Saitoh, and K. Uchida: J. Appl. Phys. **106** (2009) 024511.
5) H.-J. L. Gossmann, A. Agarwal, T. Parrill, L. M. Rubin, and J. M. Poate: IEEE Trans. Nanotechnol. **2** (2003) 285.
6) D. Lenoble, K. G. Anil, A. De Keersgieter, P. Eybens, N. Collaert, R. Rooyackers, S. Brus, P. Zimmerman, M. Goodwin, D. Vanhaeren, W. Vandervorst, S. Radovanov, L. Godet, C. Cardinaud, S. Biesemans, T. Skotnicki, and M. Jurczak: VLSI Symp. Tech. Dig., 2006, p. 168.
7) C. W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J. P. Colinge: Solid-State Electron. **54** (2010) 97.
8) J. P. Colinge, C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A. M. Kelleher, B. McCarthy, and R. Murphy: Nat. Nanotechnol. **5** (2010) 225.
9) C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J. P. Colinge: Appl. Phys. Lett. **94** (2009) 053511.
10) C. J. Su, T. I. Tsai, Y. L. Liou, Z. M. Lin, H. C. Lin, and T. S. Chao: IEEE Electron Device Lett. **32** (2011) 521.
11) H. T. Lue, T. H. Hsu, Y. H. Hsiao, S. P. Hong, M. T. Wu, F. H. Hsu, N. Z. Lien, S. Y. Wang, J. Y. Hsieh, L. W. Yang, T. Yang, K. C. Chen, K. Y. Hsieh, and C. Y. Lu: VLSI Symp. Tech. Dig., 2010, p. 131.
12) H. T. Lue, Y. H. Hsiao, P. Y. Du, S. C. Lai, T. H. Hsu, S. P. Hong, M. T. Wu, F. H. Hsu, N. Z. Lien, C. P. Lu, J. Y. Hsieh, L. W. Yang, T. Yang, K. C. Chen, K. Y. Hsieh, R. Liu, and C. Y. Lu: VLSI Symp. Tech. Dig., 2009, p. 224.
13) Y. S. Wu and P. Su: IEEE Trans. Nanotechnol. **7** (2008) 299.
14) V. P. H. Hu, Y. S. Wu, and P. Su: Semicond. Sci. Technol. **24** (2009) 045017.
15) G. Pei, V. Narayannan, Z. Liu, and E. C. Kan: IEDM Tech. Dig., 2001, p. 5.3.1.
16) J. D. Marshall and J. D. Meindl: IEEE Trans. Electron Devices **35** (1988) 373.
17) DESSIS software manual (Synopsys International, 2004).

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