

Thermal stability of AlSiCu/W/n⁺p diodes with and without TiN barrier layer

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Abstract

Thermal stability of AlSiCu/W/n⁺p diodes with two different W contact structures prepared by selective W chemical vapour deposition (W-CVD), was first investigated. The diodes with the self-aligned W-contacted structure were able to sustain a 30 min furnace annealing up to 500 °C without degradation of electrical characteristics. The diodes with the contact-hole W-contacted structure were thermally less stable than the diodes with the self-aligned W-contacted structure, presumably because the sidewall of the W-filled contact hole provided a path for diffusion of Al into the Si substrate, leading to junction spiking. The insertion of a 400 Å TiN barrier layer between the AlSiCu and W films blocked the Al diffusion path; thus, the AlSiCu/TiN/W/n⁺p diode was able to retain its integrity up to 550 °C furnace annealing.

Keywords: Titanium nitride; Tungsten; Chemical vapour deposition; Annealing

1. Introduction

One of the main concerns of very large scale integrated (VLSI) process technology is to fabricate reliable, low-resistivity contacts to shallow junctions. Thus, the introduction of barrier layers between the aluminum metallization and the silicon substrate is becoming important in order to avoid junction spiking and contact degradation caused by the transport of substrate silicon into the aluminum overlayer. [1] Selective W chemical vapour deposition (W-CVD) is an attractive technique of depositing a W film which can be used as a diffusion barrier in the AlSiCu/W/Si contact structures. [2–4] The applications of selective W-CVD include contact-hole filling [5] and self-aligned gate and source/drain cladding of metal-oxide semiconductor field effect transistors (MOSFETs). [6] The diffusion barrier properties of W films have been extensively studied. [7,8] However, most of the studies were limited to material analysis, though there were reports of thermal stability with respect to leakage current on the AlSiCu/W/Si junction diodes having a conventional W-filled contact hole structure. [9–11] In this work, thermal stability of the AlSiCu/W/n⁺p diodes with the self-aligned W contact structures, as well as the contact-hole W contact structures was investigated with respect to the electrical characteristics. We show that the thermal stability of AlSiCu/W/n⁺p is related to the diffusion behaviour of Al and the barrier

capability of tungsten. The study was then extended to investigate the effect of a TiN diffusion barrier.

2. Experimental details

Three different diode structures were used in this study, as illustrated in Fig. 1. To fabricate the AlSiCu/W/n⁺p and AlSiCu/TiN/W/n⁺p diodes, the starting material was <100>-oriented p-type Si wafers with 8–12 Ω cm nominal resistivity. After RCA standard cleaning, the wafers were thermally oxidized to grow an oxide layer 4000 Å thick. Diffusion areas with a size of 1200 × 1200 μm² were defined on the oxide-covered wafers using the conventional photolithographic technique and reactive ion etching. The junction implantation was carried out by As⁺ implantation on the p-type substrate at 50 keV to a dose of 5 × 10¹⁵ cm⁻² followed by furnace annealing at 950 °C for 30 min in a N₂ ambient. The wafers were split into two groups. For the fabrication of diodes with a self-aligned W structure (structure I, as shown in Fig. 1(a)), W films of 3000 Å thickness were deposited on the diffusion areas of a group of wafers using the selective W-CVD technique. This was followed by the deposition of a 4000 Å TEOS oxide layer. Finally, Al alloy (AlSiCu) metallization was applied after contact holes 500 × 500 μm² in size were opened. For the fabrication of diodes with a contact-hole W structure (structure II, as shown in Fig. 1(b) and

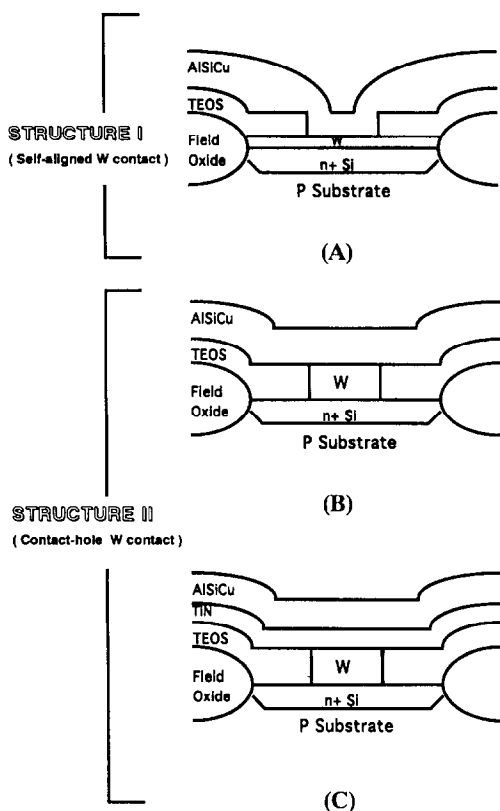


Fig. 1. Schematic cross-section of n^+p junction diodes' metallization structures. (a) AlSiCu/W/ n^+p (self-aligned W contact of structure I), (b) AlSiCu/W/ n^+p (contact-hole W contact of structure II), and (c) AlSiCu/TiN/W/ n^+p (contact-hole W contact of structure II with a TiN barrier).

1(c)), a second group of wafers were deposited with a 4000 Å TEOS oxide layer. Contact holes with a size of $500 \times 500 \mu\text{m}^2$ were defined on the oxide layer using the conventional photolithographic technique and reactive ion etching. The contact holes were then filled with tungsten using selective W-CVD. After the W deposition, this group of wafers was further split into two batches. For one batch of wafers, Al alloy metallization was applied to each diode (Fig. 1(b)). For the other batch of wafers, a 400 Å TiN layer was first sputter deposited and then Al alloy metallization was performed (Fig. 1(c)). Finally, post metallization sintering was performed at 400 °C for 30 min to all of the wafers.

In all of the aforementioned W depositions, the wafers were dipped in dilute HF (2%) for 30 s followed by a rinse in deionized water for 2 min prior to conducting the selective W-CVD. The wafers were then loaded into the load-locked cold wall W-CVD system within 5 min. An in-situ predeposition plasma etching was conducted with 30 W r.f. power, 100 mTorr gas pressure, 12 sccm flow rate of NF_3 , and 72 sccm flow rate N_2 . After the plasma etching, the wafers were transferred to the tungsten deposition chamber without being exposed to the atmosphere. The base pressure of the CVD chamber was 10^{-6} torr. The selective W-CVD was conducted at a substrate temperature of 300 °C with a total gas pressure of 100 mTorr, WF_6 flow rate of 20 sccm, SiH_4 flow rate of 10 sccm, and H_2 carrier gas flow rate of 1000 sccm.

Barrier effects of the CVD-W interlayer were evaluated using cumulative failure analysis. Thermal treatments of the diodes were carried out by conventional furnace annealing at 300–600 °C for 30 min. The sheet resistances of the Al/W/Si and Al/TiN/W/Si multilayer structures were measured by a four-point probe. Contact resistance was measured using the four-terminal Kelvin structure prepared by the conventional VLSI process as follows. After the diffusion areas were defined and the n^+p junctions were formed, the samples were subsequently covered with a dielectric layer of 4000 Å TEOS oxide. Contact holes with sizes ranging from 1 to 2 μm were defined using the conventional photolithographic and reactive ion etching technique. Finally, Al alloy metallization and/or sputter deposition of a 400 Å TiN layer was applied to form the four-terminal Kelvin structure of the AlSiCu/W/ n^+p and AlSiCu/TiN/W/ n^+p contacts.

3. Results and discussion

Current–voltage characteristics were investigated on the AlSiCu/W/ n^+p and AlSiCu/TiN/W/ n^+p junction diodes with the self-aligned W-contacted and the contact-hole W-contacted structures. Fig. 2 illustrates the histograms showing

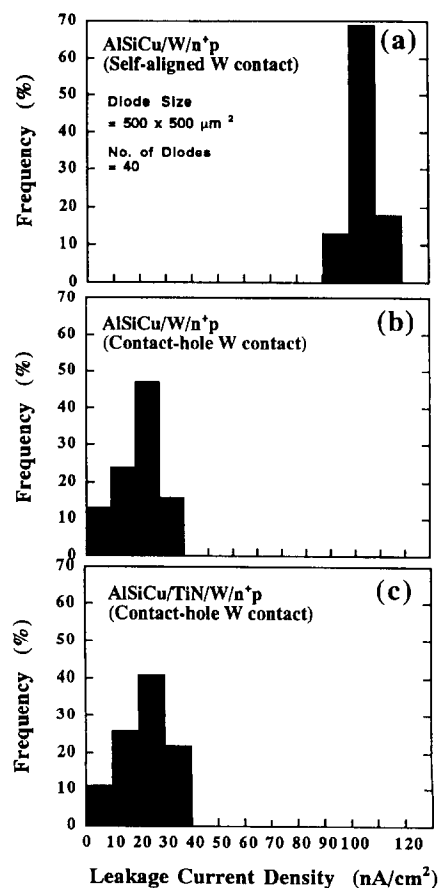


Fig. 2. Histograms showing the distribution of reverse leakage current density measured at 5 V for (a) AlSiCu/W/ n^+p diodes (self-aligned W contact), (b) AlSiCu/W/ n^+p diodes (contact-hole W contact), and (c) AlSiCu/TiN/W/ n^+p diodes (contact-hole W contact).

the distribution of the reverse leakage current density measured at 5 V; the measured diodes had an area of $500 \times 500 \mu\text{m}^2$, and at least 40 randomly chosen diodes were measured in each case. Large leakage current was observed for the self-aligned W-contacted diodes; this is presumably due to the W encroachment at the sidewall of the field oxide where a shallower junction was formed. [12] For the diodes with the contact-hole W-contacted structure, the W encroachment effect on the junction characteristics is apparently alleviated because the CVD-W was deposited on the centre region of a diffusion area where a uniform junction was formed, thus less leakage occurred. Fig. 3 shows the cumulative failure as a function of annealing temperature for the three differently W-contacted diodes. Diodes with the average reverse leakage current density higher than 700 nA cm^{-2} at 5 V were regarded as failure and at least 20 randomly chosen diodes were measured in each case. For the AlSiCu/W/n⁺p diodes, it was found that the diodes with the contact-hole W-contacted structure are thermally less stable than the diodes with the self-aligned W-contacted structure. Presumably, during the annealing treatment at a temperature of 500 °C, aluminum diffusion started to occur along the sidewall of the W-filled contact hole, leading to the failure of the diodes having the contact-hole W-contacted structure. [13] Nonetheless, the W film failed as a diffusion barrier at temperatures above 500 °C due to the massive transport of Al and Si across the CVD-W film. [14] With the insertion of a TiN barrier layer between the aluminum alloy and the W contact, the thermal stability of the diodes was remarkably improved. The AlSiCu/TiN/W/n⁺p diodes were able to retain their characteristic integrity up to a 550 °C anneal for 30 min. It is clear that TiN is an effective diffusion barrier against Al and Si interdiffusion.

Contact resistance was measured for the AlSiCu/W/n⁺p and AlSiCu/TiN/W/n⁺p diodes with the contact-hole W-contacted structure. Fig. 4 shows the measured contact resistance versus contact size using the four-terminal Kelvin structure. For the AlSiCu/W/n⁺p diode structure with a contact area of $2 \times 2 \mu\text{m}^2$, the measured contact resistance was about 25 Ω, which corresponds to a contact resistivity of

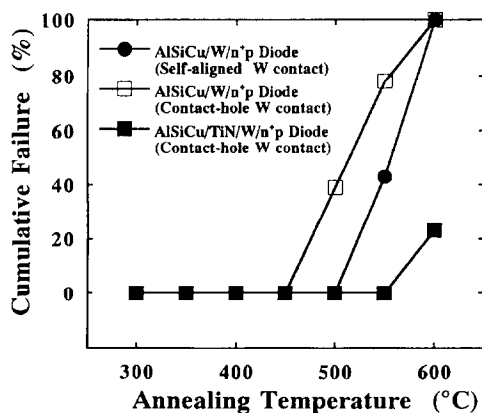


Fig. 3. Cumulative failure of AlSiCu/W/n⁺p (self-aligned W contact as well as contact-hole W contact structure) and AlSiCu/TiN/W/n⁺p (contact-hole W contact structure) diodes as a function of annealing temperature.

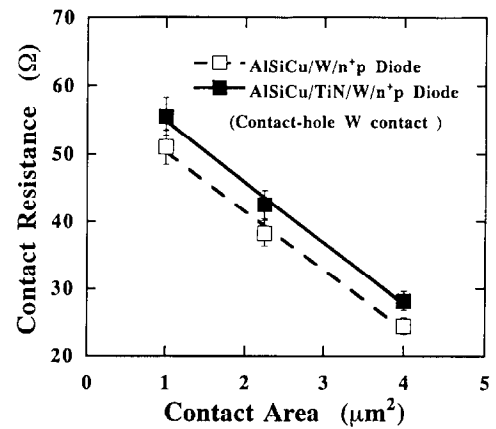


Fig. 4. Contact resistance versus contact size for the AlSiCu/W/n⁺p and AlSiCu/TiN/W/n⁺p diodes with the contact-hole W contact structure.

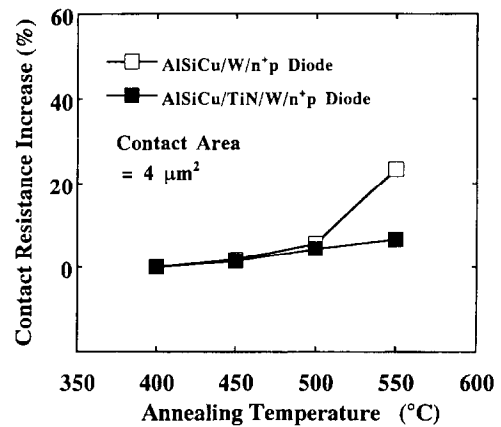


Fig. 5. Contact resistance versus annealing temperature for the AlSiCu/W/n⁺p and AlSiCu/TiN/W/n⁺p diodes with the contact-hole W contact structure.

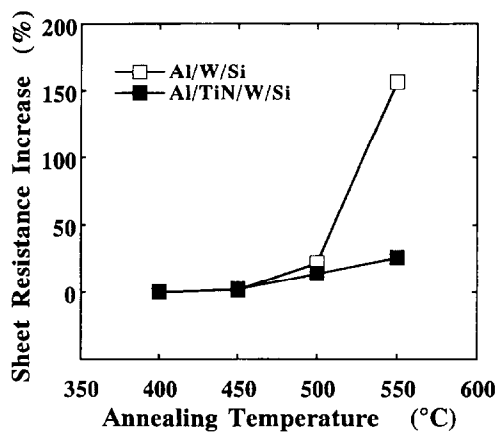


Fig. 6. Increase of sheet resistance versus annealing temperature for the AlSiCu/W/Si and AlSiCu/TiN/W/Si structures.

$1 \times 10^{-6} \Omega \text{ cm}^2$. The contact resistance measured on the AlSiCu/TiN/W/n⁺p diodes is only slightly higher than that of the AlSiCu/W/n⁺p diodes. The thermal stability of contact resistance for the AlSiCu/W/n⁺p and AlSiCu/TiN/W/n⁺p diodes was also investigated, and the result is illustrated in Fig. 5. Contact resistance of the AlSiCu/W/n⁺p diodes started to show degradation after annealing at temperatures above 450 °C. Presumably, some interfacial reaction had

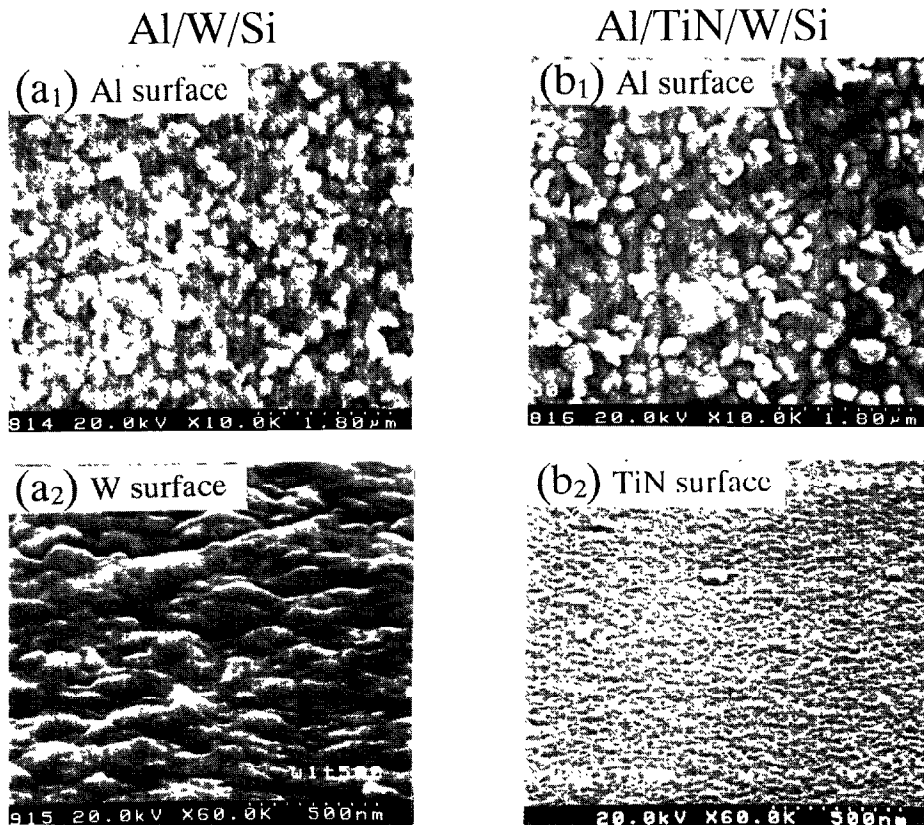


Fig. 7. SEM micrographs for the 500 °C-annealed Al/W/Si and Al/TiN/W/Si samples: (a₁) Al surface of the Al/W/Si sample, (a₂) W surface of the Al/W/Si sample after removal of the Al layer, (b₁) Al surface of the Al/TiN/W/Si sample, and (b₂) TiN surface of the Al/TiN/W/Si sample after removal of the Al layer.

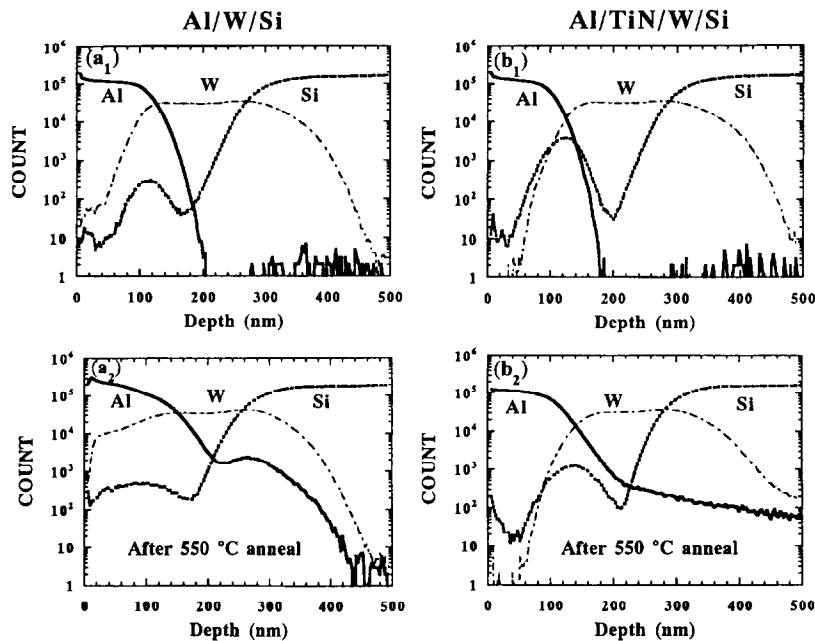


Fig. 8. SIMS depth profiles of (a₁) Al/W/Si sample, (a₂) 550 °C-annealed Al/W/Si sample, (b₁) Al/TiN/W/Si sample, and (b₂) 550 °C-annealed Al/TiN/W/Si sample.

occurred between the metal layers. In the Al/W/Si system, Pauleau et al. [15] reported the formation of a W–Al alloy (WAl¹²) at 450 °C; Harada et al. [16] also showed that W will diffuse into Al and reach the Al surface after 500 °C annealing. In contrast, the contact resistance of the AlSiCu/

TiN/W/n⁺p diodes remained stable up to annealing at 550 °C. Apparently, the 400 Å TiN layer played a role of an effective diffusion barrier against W diffusion into AlSiCu and suppressed the reaction between W and Al. To further investigate the barrier capability of the W film, the sheet

resistance change as a function of annealing temperature was measured for the Al/W/Si and Al/TiN/W/Si multilayer samples, and the result is illustrated in Fig. 6. No change in sheet resistance was observed for annealing at temperatures below 400 °C. Above 450 °C, however, an increase of sheet resistance was observed. Apparently, the 3000 Å W layer was not able to prevent Al and Si from interpenetration at 550 °C, leading to a sharp increase in the sheet resistivity of the structure [17]. The increase of sheet resistance for the Al/TiN/W/Si multilayer was mild compared with that of the Al/W/Si multilayer, apparently due to the diffusion barrier effect of TiN layer. The SEM micrographs shown in Fig. 7 reveal the morphology of the Al and W and TiN surfaces, respectively, in the 500 °C-annealed Al/W/Si and Al/TiN/W/Si multilayer samples before (Fig. 7(a₁) and 7(b₁)) and after (Fig. 7(a₂) and 7(b₂)) removal of the Al overlayer. Compared with the rough morphology and large grain size of the W film, the TiN film with its dense looking surface morphology presumably played a role of barrier against Al diffusion. Fig. 8 shows the SIMS depth profiles measured on the Al/W/Si and Al/TiN/W/Si multilayer samples before and after a 550 °C anneal. The diffusion of Al through the W film into Si substrate was clearly observed in the annealed Al/W/Si sample. For the annealed Al/TiN/W/Si sample, diffusion of Al still existed, but has been greatly alleviated. We believe that a tighter optimization control on the deposition process of TiN film is necessary to achieve an optimal diffusion barrier effect.

4. Conclusion

The AlSiCu/W/n⁺p diodes of the self-aligned W-contacted structure, with the W inter-layer deposited by selective W-CVD, were able to sustain a 30 min furnace annealing up to 500 °C without causing electrical characteristics degradation. However, the AlSiCu/W/n⁺p diodes with the contact-hole W-contacted structure were thermally less stable, presumably because the sidewall of the W-filled contact hole provided diffusion paths for the interdiffusion between Al

and the Si substrate. The insertion of a 400° TiN barrier layer between the AlSiCu and W films blocked the Al diffusion path. Thus, the AlSiCu/TiN/W/n⁺p diode was able to retain its integrity up to 550 °C furnace annealing.

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