



# The Deterioration of a-IGZO TFTs Owing to the Copper Diffusion after the Process of the Source/Drain Metal Formation

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In this work, the influence of copper on amorphous type Indium-Gallium-Zinc-Oxide (a-IGZO) thin-film transistor's (TFTs) transfer curve is studied. The  $I_D$ - $V_G$  curves of a-IGZO TFTs with source/drain in the structures of Cu/Ti and Ti/Al/Ti are compared. The results show that the copper greatly deteriorates the performance of the TFTs. The presence of the copper in the channel region of the device is verified by SIMS analysis. A Cu-dipping experiment is conducted by dipping devices into the solution of  $\text{CuSO}_4$  to confirm the role of copper in the deterioration of the  $I_D$ - $V_G$  curves. The hypothesis is also verified through ATLAS device simulator. © 2012 The Electrochemical Society. [DOI: 10.1149/2.025206jes] All rights reserved.

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Indium-Gallium-Zinc-Oxide (a-IGZO) thin-film transistors (TFTs) have attracted great attention for the impressive transparent and high carrier mobility characteristics. They can serve in switching pixel or peripheral circuit application for active-matrix liquid crystal displays (AMLCDs) in the next generation.<sup>1,2</sup> With the increase of display size, resolution, and the operating frequency in television and 3D display, Cu is applied to replace Al for the reduction of resistance loading in the signal metal bus. Many attempts have been made to incorporate Cu into the amorphous silicon TFT array fabrication.<sup>3-5</sup> The process implementation of using Cu as the source/drain (S/D) metal of a-IGZO TFT is also an interesting topic to study. However, most of the previous papers about a-IGZO TFT with the application of Cu emphasized on the contact resistance and the quality of the surface between Cu and a-IGZO.<sup>6-10</sup> In the present work, the influence of Cu diffusion to the electrical properties of a-IGZO TFT is observed and studied.

## Device and Experiment

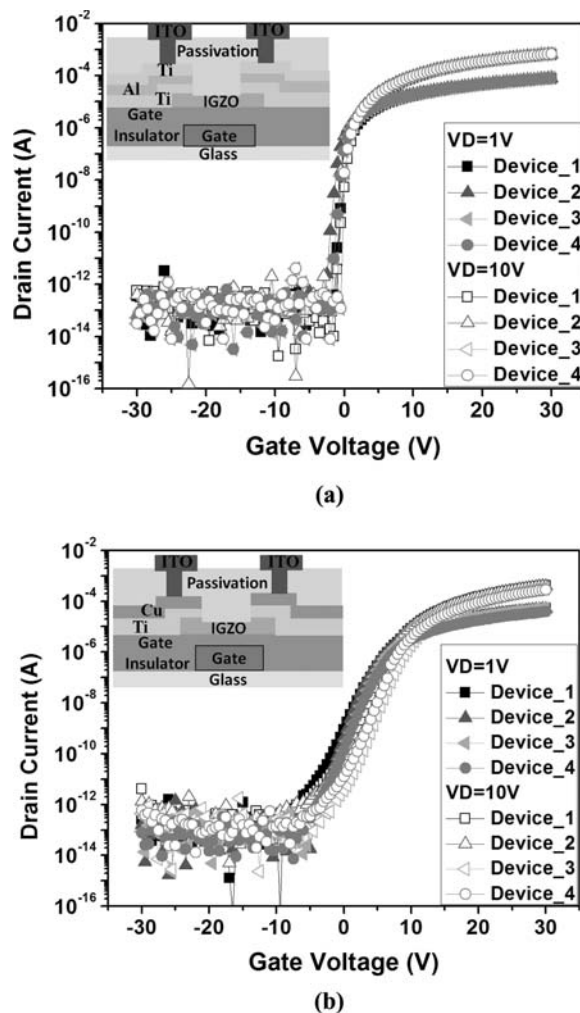
The experimental work was based on the bottom-gate TFT devices of back-channel-etch (BCE) structure with symmetrical S/D fabricated on the glass substrate. Shaped Ti/Al/Ti (50/200/50 nm) gate electrodes were capped with 400-nm-thick  $\text{SiN}_x$  gate dielectric, which was deposited by plasma enhanced chemical vapor deposition (PECVD) at 370°C. The active layer of 60-nm-thick a-IGZO film was deposited by DC magnetron sputtering system using a target of In:Ga:Zn = 1:1:1 in atomic ratio with the  $\text{O}_2/\text{Ar}$  ratio about 6%. For the S/D metals, both samples of Ti/Al/Ti (50/200/50 nm) and Cu/Ti (200/50 nm) were prepared by DC sputtering at room temperature. Then, the devices are capped with passivation at 280°C as protection layer to avoid the disturbance of outside surrounding. After that, via holes and ITO were patterned and shaped for device measurement. The final annealing step was conducted at 280°C for 1 hour in the oven. In this study, the electrical characteristics are measured by Agilent 4156-C system at 25°C in dark under 1 atmosphere pressure. The threshold voltage ( $V_T$ ) is defined by the gate voltage ( $V_G$ ) when the size-normalized drain current  $I_D$  reaches  $10^{-9}$  A. The subthreshold swing (S.S) and effective field mobility ( $\mu$ ) are extracted at drain voltage  $V_D = 1$  V.

## Transfer Characteristics

Figure 1a and 1b show the electrical characteristics of a-IGZO TFTs with S/D metal of Ti/Al/Ti and Cu/Ti with their cross-section schematics in the insets, respectively. The average values of the  $V_T$ ,  $\mu$  and S.S for the Ti/Al/Ti samples at distant sites on the glass substrate are -0.78 V, 10.13  $\text{cm}^2/\text{V s}$ , and 0.48 V/dec, accordingly, while those

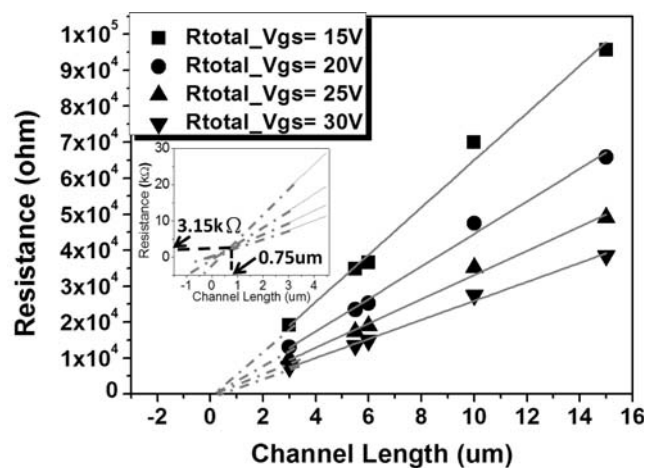
for the Cu/Ti samples are 5.27 V, 8.12  $\text{cm}^2/\text{V s}$ , and 1.58 V/dec, correspondingly. The performance of the devices fabricated with Cu/Ti S/D metal is apparently worse than that of Ti/Al/Ti samples.

In Figure 2, the parasitic contact resistances for these devices are extracted to check whether the deterioration is owing to the quality of the S/D contact by measuring the TFTs with different channel

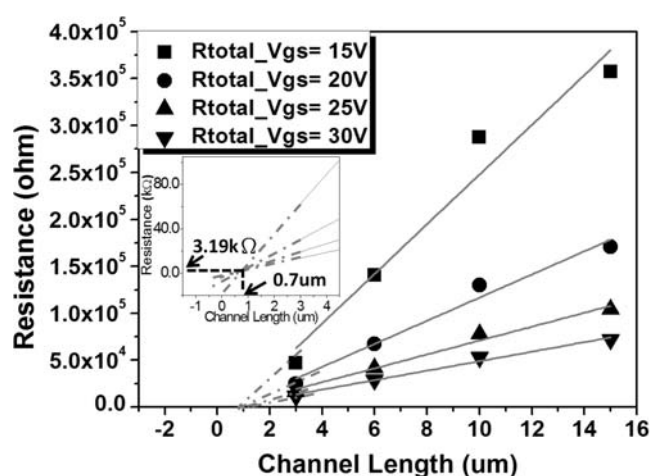


**Figure 1.** (a) The  $I_D$ - $V_G$  transfer characteristics of a-IGZO TFTs with S/D metal of (a) Ti/Al/Ti and (b) Cu/Ti and their correspondent cross-section schematics.

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(a)



(b)

**Figure 2.** The parasitic resistance extracted from a-IGZO TFTs of (a) Cu/Ti and (b) Ti/Al/Ti S/D with different channel lengths.

length.<sup>11-13</sup> With the measurement of  $I_D$ - $V_G$  curve at  $V_{DS} = 0.1V$ , the total ON resistance of TFT ( $R_{total}$ ) is represented as Eq. 1:

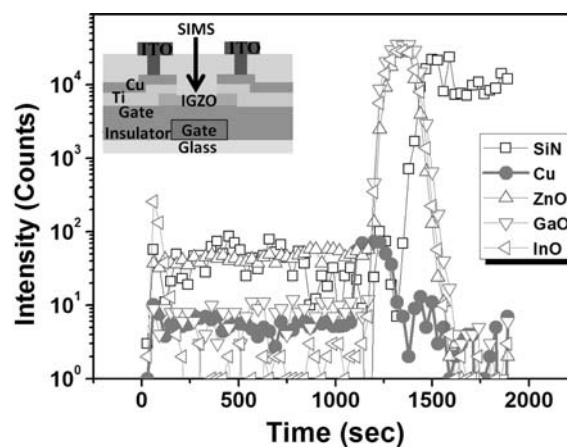
$$R_{total} = \frac{V_{DS}}{I_{DS}} = R_D + R_S + R_{ch} \cdot L \quad [1]$$

where  $R_{ch}$  is the channel resistance per unit channel length,  $R_s$  and  $R_d$  denote the source and drain resistance, respectively. With the use of intrinsic mobility field-effect mobility  $\mu_i$ , the gate insulator unit capacitor  $C_{ox}$ , and the threshold voltage  $V_{th}$ ,  $R_{ch}$  can be represented as Eq. 2:

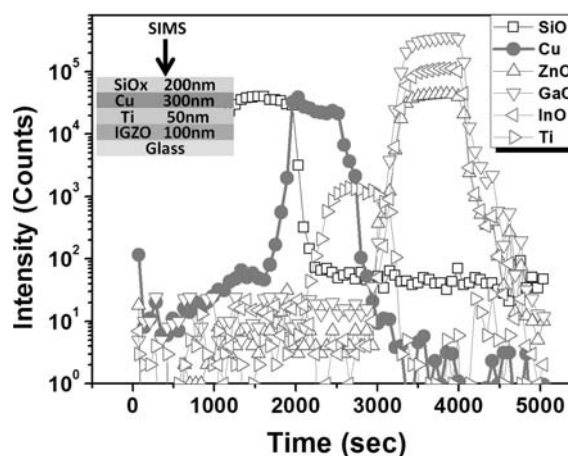
$$R_{ch} = \frac{1}{\mu_i C_{ox} W (V_G - V_{th} - \frac{1}{2} V_D)} \quad [2]$$

By substituting Eq. 2 into Eq. 1, the extraction result of TFTs with Ti/Al/Ti and Cu/Ti as S/D metal, are 3.15 K $\Omega$  and 3.19 K $\Omega$ , respectively. The extraction result excludes the possible reason that it is the quality of the metal contact to influence the device characteristics. Therefore, the factor that affects the device transfer curve should be in the region of device channel.

Because of the high diffusivity,<sup>14</sup> Cu can deeply incorporate with the IGZO film. We then come to the hypothesis that Cu in the device channel region is the reason of the deterioration in the characteristics of a-IGZO TFTs. Secondary ion mass spectrometry (SIMS) is applied to trace the existence of Cu in depth in the channel region for the



(a)



(b)

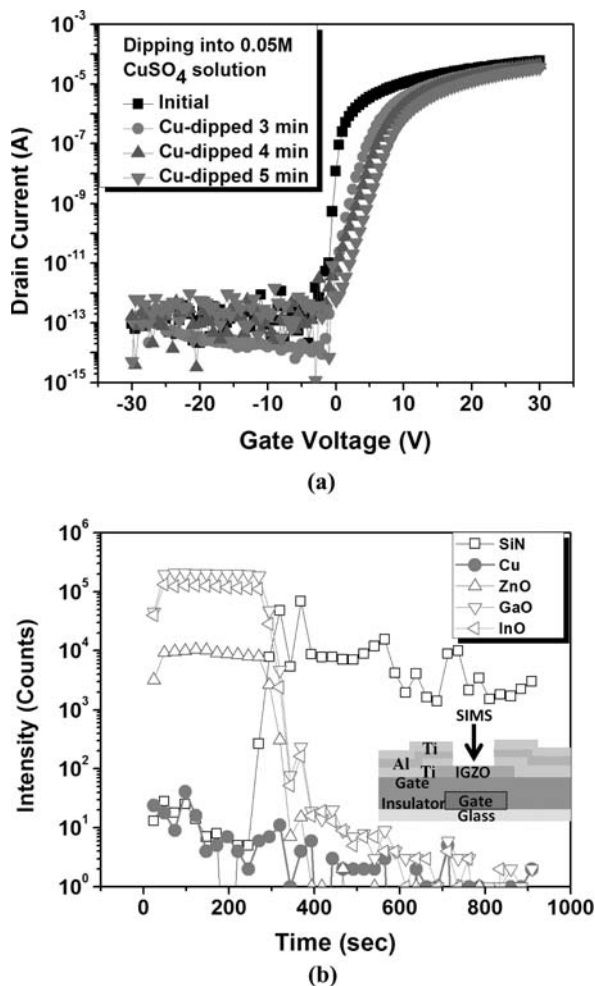
**Figure 3.** (a) The SIMS result of the channel region for the device using Cu/Ti as the S/D metal. (b) SIMS result of SiO<sub>2</sub>/Cu/Ti/IGZO stacked film with no pattern.

TFTs with Cu/Ti S/D, as shown in Fig. 3a. The profile of Cu signal distributing from the passivation to the gate insulator proves the existence of Cu. In order to check whether Cu can penetrate through Ti or not, stacked films of IGZO, Ti, Cu, SiOx deposited on glass was also analyzed by SIMS. As shown in Figure 3b, the signal of Cu is untraceable. It reveals that Cu of S/D in the contact region can hardly degrade the IGZO film with Ti as buffer metal between active layer and S/D metal.

To further examine the Cu diffusion, non-passivated a-IGZO TFTs with S/D metal of Ti/Al/Ti were dipped into the CuSO<sub>4</sub> solution. After the dipping process, these devices were annealed at 280°C to imitate the deposition environment of passivation. The  $I_D$ - $V_G$  curves of the a-IGZO TFTs without Cu in the S/D metal dipped in the CuSO<sub>4</sub> solution of the same concentration (0.05M) for various dipping time are shown in Fig. 4a. The deterioration of the  $I_D$ - $V_G$  curve becomes more and more serious with the increasing dipping time. The SIMS result of device with S/D metal of Ti/Al/Ti dipped into the CuSO<sub>4</sub> solution indicates the existence of Cu, even though the SIMS signal is not very strong. We conclude that the a-IGZO TFT is quite sensitive to the existence of Cu in the channel.

### Defects Induced by Copper

In the previous report, the Cu element has been regarded as an acceptor in ZnO.<sup>15</sup> The formation mechanism of wide bandgap p-type



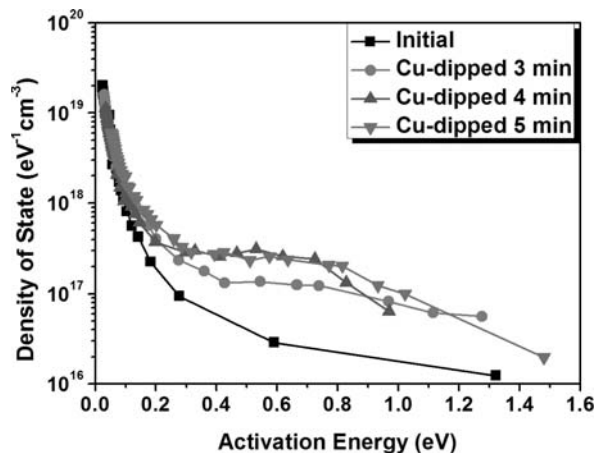
**Figure 4.** The  $I_D$ - $V_G$  transfer curves of a-IGZO TFT with Ti/Al/Ti S/D metal dipped in  $\text{CuSO}_4$  solution (a) for different dipping times (b) the SIMS result of the device after dipping.

conduction oxide is proposed based on the concept that the chemical bonds of Cu–O form a covalent hybridized band between the O 2p<sup>6</sup> and Cu 3d orbitals at the top of the valence band.<sup>16–18</sup> For a p-type oxide semiconductor, the TFT is turned on when it is biased at negative voltage. In other words, if it is the case, a significant hole current should be observed for the TFTs with negative  $V_G$ . However, as shown in Fig. 1, the leakage current in the devices fabricated with Cu/Ti as S/D metal is almost the same as that of conventional device. It depicts that the role of Cu can be different and needs to be discussed in more detail.

Assuming the current in the IGZO thin film distributed uniformly in the film of IGZO about several hundred angstroms in thickness, the density of states (DOS) of the IGZO TFT can be extracted from the  $I_D$ - $V_G$  characteristics for further discussions.<sup>19</sup> According to the method proposed by Globus et al.,<sup>20</sup> measuring the activation energy  $E_a$  at different gate voltages  $V_G$ , the DOS can be calculated based on the following equation

$$g(E_a) = -\frac{\varepsilon_i}{qd_i t \frac{d(E_a)}{d(V_G)}} \quad [3]$$

where  $\varepsilon_i$  and  $d_i$  are respectively the permittivity and the thickness of the gate dielectric,  $q$  is the electron charge, and  $t$  is the thickness of the active layer.<sup>20</sup> Fig. 5 shows the DOS of the Cu-dipped devices extracted through the measurement of  $I_D$ - $V_G$  under different temperatures. The magnitude of DOS increases from  $10^{16} \text{cm}^{-3}$  to  $10^{18} \text{cm}^{-3}$  with respect to the dipping time. We come to a hypothesis that the role



**Figure 5.** The DOS of the devices shown in Figure 4a extracted through the measurement of  $I_D$ - $V_G$  under different temperatures.

of Cu in IGZO is more like being a defect diffused among the atoms than an acceptor taking the substitutive sites to provide hole.

A commercial ATLAS device simulator produced by Silvaco, Inc., was used to study the possible defects that Cu can form in IGZO TFT. Several parameterized components were used to express the subgap density of states (DOS), such as the acceptor-like exponential and Gaussian functions and the donor-like exponential and Gaussian functions.<sup>21</sup> In this work, we introduce an exponential function  $g_{\text{exp}}(E)$  expressed by:

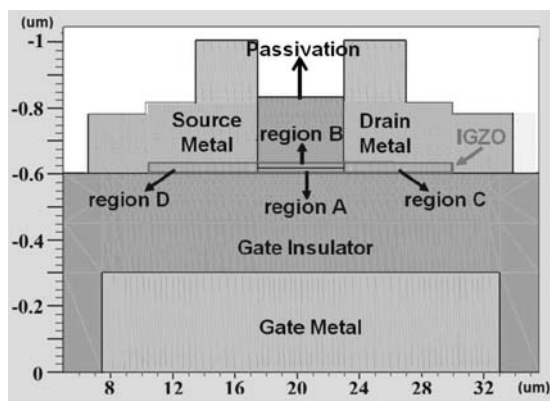
$$g_{\text{exp}}(E) = N_{\text{TA}} \cdot \exp\left[-\frac{E-E_C}{W_{\text{TA}}}\right] \quad [4]$$

to describe the DOS near the conduction band, where  $N_{\text{TA}}$  is the conduction band edge intercept energy,  $E$  is the state energy,  $E_C$  is the conduction band edge, and  $W_{\text{TA}}$  is the characteristic decay energy of the exponential distribution. The sub-gap DOS function  $g_G(E)$  that Cu forms in IGZO film is modeled by:

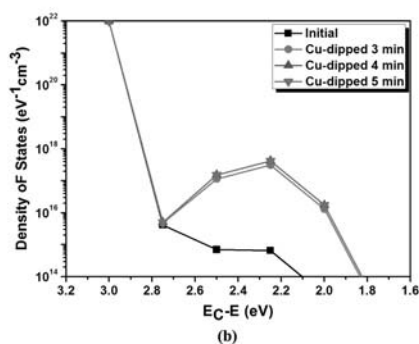
$$g_G(E) = N_{\text{GA}} \cdot \exp\left\{-\left[\frac{E_{\text{GA}}-E}{W_{\text{GA}}}\right]^2\right\} + N_{\text{GD}} \cdot \exp\left\{-\left[\frac{E-E_{\text{GD}}}{W_{\text{GD}}}\right]^2\right\} \quad [5]$$

where  $N_{\text{GA}}$  and  $N_{\text{GD}}$  are the densities at the peak of Gaussian distribution,  $E_{\text{GA}}$  and  $E_{\text{GD}}$  are the centers of the distribution,  $W_{\text{GA}}$  and  $W_{\text{GD}}$  are the characteristic decay energies of Gaussian distribution for the acceptor-like and donor-like states, respectively. Since the diffusion of Cu is from the back channel of device, the defect density in the active layer near the back channel surface (region B) is set to be larger than those in the region near the front gate (region A) and the S/D contact regions (region C and D) in our simulation, as shown in Fig. 6a. The DOS of region B used in the simulation for the different times of  $\text{CuSO}_4$  dipping are shown in Fig. 6b. The subgap states of acceptor-like and donor-like are both simulated.

Fig. 7a shows the simulation results with the increasing of acceptor-like Gaussian distribution subgap DOS and the measurement data of the  $\text{CuSO}_4$ -dipping experiment shown in Fig. 4a. The simulation results fairly fit the measured curves. However, the results by increasing of donor-like Gaussian distribution subgap DOS in the same manner do not match the measurement data, as shown in Fig. 7b. These simulation results suggest that the role of Cu in a-IGZO film to be an acceptor-like defect near conduction band. The proposed role of Cu is further supported by two arguments. Firstly, according to the percolation conduction model,<sup>22</sup> the worse subthreshold swing and larger  $V_{\text{th}}$  indicate the increase of deep states. In addition, Cu distributed in the IGZO film may act as acceptor-like trap states in the cases of silicon devices.<sup>23–25</sup>

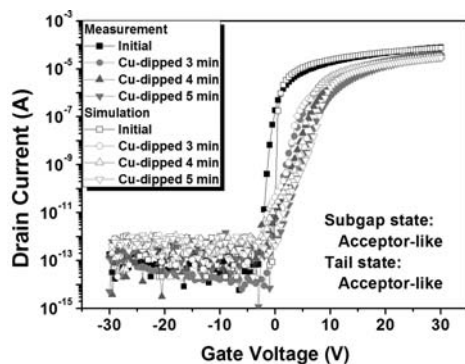


(a)

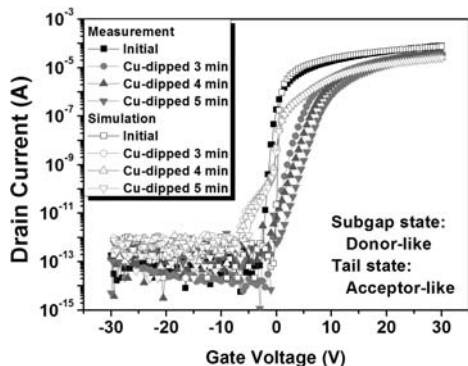


(b)

**Figure 6.** (a) The structure and IGZO regions of the device and (b) the DOS of region B used in the ATLAS simulation for the different times of CuSiO<sub>4</sub> dipping.



(a)



(b)

**Figure 7.** The ATLAS simulation results for the cases of (a) acceptor-like subgap states and (b) donor-like subgap states in IGZO along with the measurement results shown in Fig. 4a.

## Conclusions

In summary, the performances of a-IGZO TFTs with and without Cu in the S/D electrodes are compared. The application of Cu/Ti as the S/D metal of the a-IGZO TFT does not affect the parasitic contact resistance. Instead, the existence of Cu in the channel is verified by SIMS analysis and is realized to be the reason that deteriorated the  $I_D$ - $V_G$  curves. The defects that form by Cu diffusion in IGZO film are proposed to be the acceptor-like trap states below the conduction band, which explains the increased DOS and the unchanged leakage current of the TFT. The results of the CuSO<sub>4</sub>-dipping experiment are consistent with the proposed mechanism. Considering the impact of Cu to the electrical properties of a-IGZO TFTs is so tremendous, the fabrication process of device with Cu electrode should be designed carefully.

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