Structural Effect on Band-Trap-Band Tunneling Induced Drain Leakage in n-MOSFET's

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***Abstract*—The structural dependence of the hot carrier stress incurred drain leakage current via band-trap-band tunneling in off-state has been modeled and characterized in conventional S/D, DDD, and LDD n-MOSFET structures. The results shows that lateral field enhanced band-trap-band tunneling is primarily responsible for an increased drain leakage current after hot carrier stress in LDD structures while vertical field induced tunneling is dominant in conventional S/D and DDD structures.**

I. Introduction

Gate induced drain leakage (GIDL) current attributed to band-to-band tunneling has been found to be a major reliability issue in off-state MOSFET's [1], [2]. Recently, much research interest has been attracted to the study of hot carrier stress effects on the GIDL [3]–[5]. In our earlier work, an interface trap-assisted tunneling and thermionic emission model [6] has been developed to evaluate an increased drain leakage current after hot carrier stress. In the model, a complete band-trap-band leakage path is formed at the Si/SiO_2 interface by hole emission from interface traps to a valance band and electron emission from interface traps to a conduction band. It has been shown that, at a sufficiently large V_{dg}, both electron and hole transitions are made through quantum tunneling. The two-step band-trap-band tunneling becomes increasingly important as the device dimension is further reduced since the vertical and the lateral electrical fields are continually increased in each generation of device scaling according to the generalized MOSFET scaling theory [7]. The trap-assisted leakage mechanism can be further divided into vertical field dominant tunneling and lateral field dominant tunneling. The features of these two tunneling processes are quite different. In this letter, the drain leakage currents via these two processes are characterized and modeled in a variety of MOSFET structures.

II. Experiment

To investigate the structural dependence of the band-trap-band tunneling process, three types of MOSFET structures, a 0.5 μm LDD with 120 Å gate oxide, a 2.0 μm conventional S/D with 90 Å gate oxide, and a 2.0 μm DDD with 90 Å gate oxide, were fabricated. In the LDD MOSFET, the n^- implant dose is 1.5×10^{13} cm^{-2} phosphorus. The spacer width is 0.1 μm. An arsenic dose of 4.0×10^{15} cm^{-2} was implanted in the n^+ source/drain regions. The n^- length and the overlap between the gate and the n^- region are about 0.08 μm and 0.03 μm, respectively. Both of the conventional S/D and the DDD MOSFET's have a n^+ arsenic implant dose of 2.5×10^{15} cm^{-2}. The n^- phosphorus implant is 1×10^{14} cm^{-2} in the DDD structure. The n^- length and the gate/n^+ drain overlap are 0.08 μm and 0.19 μm, respectively. A maximum substrate current stress method was adopted to obtain maximum interface trap generation and to minimize the oxide charge effects [8]. The stress conditions in the LDD, conventional S/D, and DDD MOSFET's were 1) $V_{gs} = 2.5$ V, $V_{ds} = 6$ V, 2) $V_{gs} = 2.5$ V, $V_{ds} = 5.5$ V, and 3) $V_{gs} = 2.5$ V, $V_{ds} = 6.5$ V, respectively. It should be mentioned that both of the S/D and DDD devices were stressed under approximately the same substrate current.

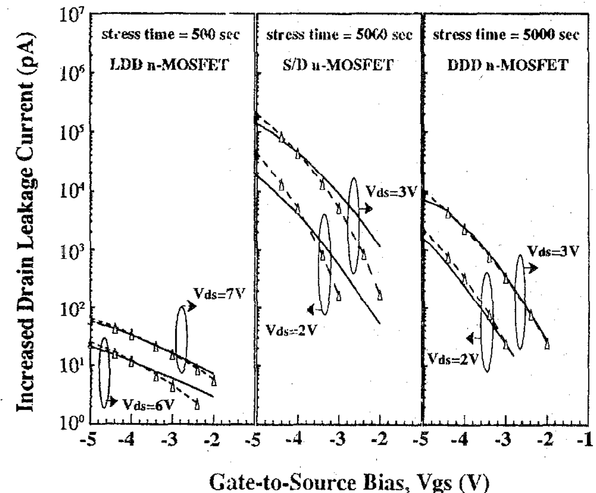

Fig. 1. Measured (solid lines) and calculated (dashed lines) additional drain leakage currents due to interface traps in LDD, S/D, and DDD MOSFET's.

III. Results and Discussions

Under a trap-assisted tunneling dominant condition, the increased drain leakage current can be derived as follows [6]:

$$\Delta I_d = A \exp\left(-B_{it}/F\right) \quad (1)$$

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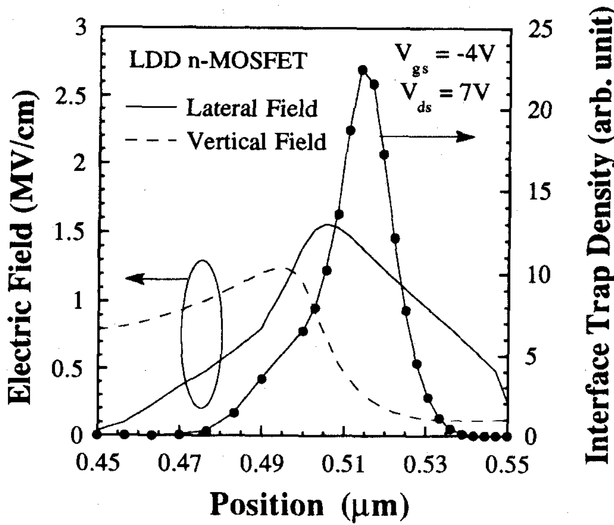
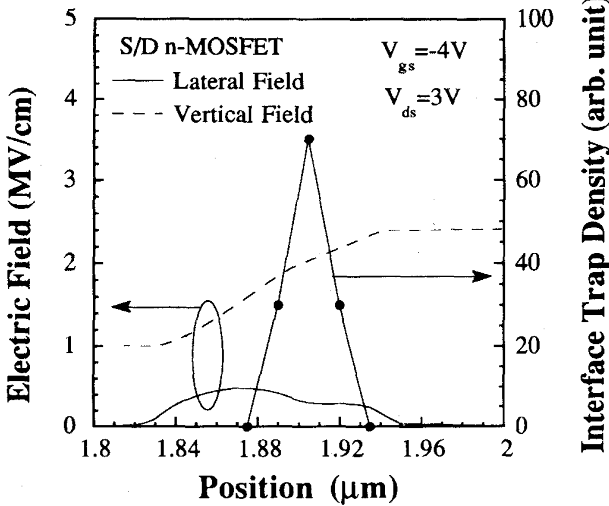


(a)



(b)

Fig. 2. Vertical and lateral field distributions in (a) LDD and (b) S/D MOSFET's. The gate edge is at 0.5 μm in the LDD device and at 2.0 μm in the S/D device.

$$B_{it} = \frac{4}{\hbar}(2m_n)^{1/2}\frac{(E_c - E_t)^{3/2}}{3q} \tag{2}$$

$$E_t = \frac{E_v + (F_1/F)^{2/3}E_c}{1 + (F_1/F)^{2/3}} \tag{3}$$

where A is proportional to the interface trap density, F_1 is a lateral field, F is a total field, and E_t is the energy level of interface traps which are most effective in the band-trap-band tunneling process. Other variables have their usual definitions. It should be pointed out that if the lateral field is much greater than the vertical field, a theoretically lower limit of B_{it} about 13 MV/cm is obtained and the corresponding E_t is 0.5 $(E_c + E_v)$. In the other extreme, if the vertical field is much larger than the lateral field, B_{it} has a maximum value of 36 MV/cm which is the same as the GIDL [9]. Thus, the value

Device Structures (× : interface traps)	Pre-stress	Post-stress	
	B (MV/cm)	B_{it} (MV/cm)	Dominant field in tunneling
LDD (Gate, n⁻, n⁺)	28	13 ~ 15	lateral field
S/D (Gate, n⁺)	31	23 ~ 25	vertical field
DDD (Gate, n⁺, n⁻)	35	21 ~ 25	vertical field

Fig. 3. Comparison of the band-trap-band tunneling characteristics in various MOSFET structures.

of B_{it} may vary significantly in different MOSFET structures depending on the relative strength of the vertical and lateral fields.

Fig. 1 shows the hot carrier stress induced drain leakage currents in the three structures. The solid lines are from measurement and the dashed lines are from calculation (1). In the calculation, the field distributions are obtained from a two-dimensional device simulation. The vertical and the lateral field distributions in the LDD and the S/D devices are plotted in Fig. 2. The gate edge is at 0.5 μm in Fig. 2(a) and at 2.0 μm in Fig. 2(b). The spatial distributions of the interface traps in the figure are evaluated from a numerical simulation [10]. The schematic cross-sections of the structures, together with some important results, are compared in Fig. 3. In the LDD MOSFET, the interface traps are generated in the spacer region (i.e., outside the gate), where the lateral field is much larger than the vertical field. Thus, the lateral field induced tunneling is dominant and the obtained B_{it} is close to its theoretically lower limit 13 MV/cm. This value is much lower than the pre-stress result. In the S/D MOSFET, however, the generated traps are located under the gate where the vertical field is stronger. As a result, the vertical field induced tunneling plays a more important role. The B_{it} reaches a higher value about 23~25 MV/cm. In the DDD MOSFET, the interface traps are also generated under the gate during stress. The vertical field enhanced tunneling is dominant and the B_{it} value is again about 21 ~ 25 MV/cm. Furthermore, our study reveals that the interface traps in the DDD structure are located farther away from the maximum electric field than in the S/D structure in a measurement bias condition. This fact explains why the increased drain leakage current in the DDD MOSFET is much lower than that of the S/D MOSFET in Fig. 1 even though both devices were stressed under the same substrate current.

In addition, the oxide charge effect on the drain leakage is evaluated through a device simulation. In the simulation, a certain amount of negative oxide charge (2×10^{12} cm^{-2}) is placed in the LDD spacer region. The simulation shows that the enhancement of the drain leakage current due to the oxide charge only is no more than 15% in the current structure. This

quantity is much smaller than the band-trap-band tunneling induced drain leakage current.

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