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Size-Dependent Trapping Effect in Nano-Dot Non-Volatile Memory

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We report a flash memory using deep traps nano-dot formed in ZrON charge trapping layers by As^+ implantation to improve the device performance of MONOS CTF device. The TaN-[SiO_2-$LaAlO_3$]-[As^+-implanted ZrON]-[$LaAlO_3$-SiO_2]-Si device shows a 6 nm ENT, a large initial memory window of 9.8 V, a 10-year extrapolated retention window of 3.6 V at 85°C, and an endurance window of 5.1 V after 10^5 cycles under fast 100 μs and low ±16 V program/erase. The performance of As^+-implanted ZrON is significantly better than that of stacked Si_3N_4/Ir-dot/HfON device with poor thickness scaling due to excess Ir metal dot.

Introduction

As listed in *International Technology Roadmap for Semiconductors* (1), the metal-oxide-nitride-oxide-Si (MONOS) charge-trapping flash (CTF) devices (1)-(15) have the high potential to replace the poly-Si floating-gate flash memory for future generation non-volatile memory (NVM) due to their discrete charge-trapping property and simple planar process. Nevertheless, the fundamental drawback of the CTF device is the distributed trap energy in Si_3N_4 (11) compared to the deep energy of 3.15 eV in poly-Si floating-gate memory, where charges stored in shallower traps may leak out and hence degrade the retention characteristics(12)-(15). Such degraded retention is one of the major challenges in highly scaled NVM device with fewer electrons (1). Although the retention can be improved by the increase of tunnel oxide thickness, the small electric field across tunnel oxide suffers from the long erase time (10~100 ms) and large P/E voltages, which are unacceptable for NVM devices. To improve the high temperature retention, the usage of deep-trapping metal-nitride trapping layer, with large conduction band offset (ΔE_C), is necessary (12)-(16). Significant improvement on retention has been realized in the CTF device with high-κ Al(Ga)N trapping layer (13). To lower the program/erase (P/E) voltages, the using higher-κ HfON trapping layer is required for CTF device (14)-(15). However, this HfON has a lower trapping efficiency than that of Si_3N_4 with a smaller memory window (14).

To further improve the memory window and retention, the double trapping-layer HfON-Si_3N_4 CTF was developed (15). However, dual trapping-layer HfON-Si_3N_4 also suffers a penalty in down-scaling limit of equivalent-nitride thickness (ENT) due to adding a lower-κ Si_3N_4. Recently, nano-dot memory using ion implantation to form deep levels in high-κ trapping layer has been proposed and offers good control ability on the distributed traps (17). Thus, we focused on size-dependent effect in nano-dot memory and also investigate the memory characteristics as shrinking the nano-dot size.

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In this paper, both higher-κ deep-E_C ZrON and As^+ implantation are used to improve the CTF performance. With a 6 nm ENT trapping layer, a small As-dot, the device demonstrates an initial 5.5 V memory window and a good 3.6 V extrapolated 10-year retention window at 85°C, under a fast 100 μs and low ±16 V P/E.

Experimental Procedure

The CTF with nano-dot devices were fabricated on standard 6-in p-type Si wafers. The double tunnel oxide layers of 2.8-nm-thick thermal SiO_2 was grown on Si substrates and 3.0-nm-thick $LaAlO_3$ was deposited by physical vapor deposition (PVD). Then the charge trapping layers of 20-nm-thick Si_3N_4/Ir-dot/HfON and 30-nm-thick arsenic-implanted ZrON (As^+-implanted ZrON) were performed by using high-temperature forming step and low-energy ion implantation, respectively. Sequentially, the 4.5-nm-thick $LaAlO_3$ and 8.0-nm-thick SiO_2 as double blocking layers were deposited by PVD and chemical vapor deposition (CVD) through Tetraethyl orthosilicate gas (TEOS, $Si(C_2H_5O)_4$), respectively. Finally, the 200-nm-thick TaN gate was deposited by PVD to form the CTF structure. After standard lithography and gate patterning by reactive ion etching (RIE), self-aligned 25 keV As^+ implantation at 5×10^{15} cm^{-2} dose was applied and followed by 900°C RTA to activate the dopant at source-drain region. The fabricated devices were characterized by P/E, cycling and retention measurements.

Result and Discussion

Fig. 1 shows schematic band diagram of the Si_3N_4/Ir-dot/HfON and arsenic-implanted ZrON CTF devices. The double tunnel layers employing $LaAlO_3/SiO_2$ with thicker physical thickness allows fast P/E speeds, which can improve the memory characteristics of retention and endurance. The double blocking layers using high-κ $LaAlO_3$ and SiO_2 have the merit of lower voltage operation, which in turn improves the erase saturation due to the higher electric field across the tunnel oxide. Here the TEOS SiO_2 layer in double blocking layer has a large energy bandgap and small trap densities that are important to reach good retention characteristics at high temperatures. However, the high work-function metals including As (5.1 eV) and Ir (5.27 eV) are used to form metal dots in metal-oxynitride trapping layers, respectively, which may generate deep trapping levels and thereby obtain better trapping efficiency in a scaled ENT. The overall ENT was calculated from the $\kappa_{Si3N4}/\kappa_{trapping\ layer}\times t_{trapping\ layer}$, where the κ_{Si3N4}, $\kappa_{trapping\ layer}$ and $t_{trapping\ layer}$ are the dielectric constants of Si_3N_4, high-κ trapping layer, and the thickness of high-κ trapping layer, respectively. However, the unconfined metal dot in or near trapping layers may affect the trapping efficiency due to process- or temperature-dependent size effect. To obtain uniform dot size and density, we investigate the size effect on control Si_3N_4/Ir-dot/HfON with high-temperature annealed Ir dot and single-layer ZrON with low-energy As^+ implantation.

In Fig. 2(a), we compare C-V hysteresis of the Si_3N_4/HfON CTF devices with and without Ir dot. A larger C-V hysteresis window of 8V is obtained in Ir-dot memory than that of control device under ±14 V sweep, which is evidence of more electron trapping in Si_3N_4/Ir-dot/HfON due to the formation of deep energy levels of Ir dots (~5.27 eV). However, the thick ENT of 10.5 nm and excess dot size shown in Fig. 2(b) imply that the size control of metal dot becomes more difficult as ENT downscaling continues. In Fig.3,

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the *C-V* hysteresis of As^+-implanted ZrON CTF device increases with applied voltage, indicating the good trapping property in As^+-implanted ZrON with a reduced ENT of 6 nm. Also, even larger *C-V* hysteresis window of 9.8 V is obtained under ±16 V sweep. The scaled 6 nm ENT in As^+-implanted ZrON is because of small-size As dot formation via low-energy implantation, but high-temperature annealing such as control Ir dot. All the frequency-dependent *C-V* measurements were performed in the range of 10 to 700 kHz (not shown). The measured results present that the flatband voltage shift (ΔV_{FB}) is independent to the different frequencies (small frequency dispersion). Thus, the hysteresis memory window should be due to the trapping effect in As^+-implanted ZrON trapping layer rather than the interface states between tunnel oxide and Si.

The program and erase behaviors are important for device switching, which can be dominated by the Fowler-Nordheim (FN) tunneling mechanism through thin tunneling oxide. Thinning tunneling oxide allows low P/E voltages and fast P/E speeds, but compromises with charge retention. Fortunately, both good retention and low voltage operation can be achieved using high-κ based tunneling layer. The Figs. 4(a) and 4(b) show the P/E characteristics at various P/E times for the Si_3N_4/Ir-dot/HfON and As^+-implanted ZrON CTF devices, respectively. We can found that the V_{th} increases with increasing time. The large ΔV_{th} memory windows of 5.3 V and 5.5 V are obtained at ±16 V and fast 100 μs P/E for the Si_3N_4/Ir-dot/HfON and As^+-implanted ZrON CTF devices, respectively. The large memory window with the increase of switched speed in Si_3N_4/Ir-dot/HfON CTF memory is clearly contributed by Ir dot in HfON, but the dot uniformity is still a concern. The fast 100 μs P/E speed can be ascribed to the large conduction and valance band discontinuity (ΔE_C and ΔE_V) in $LaAlO_3$ and SiO_2 for easier tunneling during program and erase.

Data retention is one of the most important parameters for NVM device. Fig. 5(a) shows the retention characteristics of the Si_3N_4/Ir-dot/HfON CTF devices at 25 °C. Under ±16 V and 100 μs P/E, the charge retention for Ir-dot memory is poor since the large dot size would lead to weaker quantum confinement. To improve the degraded retention caused by dot-size effect, we employ higher-κ As^+-implanted ZrON (κ~35) (18) with small-size and uniform As-dot to improve retention characteristic. The retention characteristics at 25°C and 85°C of As^+-implanted ZrON are shown in Fig. 5(b). Under ±16 V and 100 μs P/E, the As^+-implanted ZrON devices have a large extrapolated 10-year memory window of of 4.1 V and 3.6 V at 25 and 85°C, respectively, suggesting the higher electron trap density in ZrON with small As-dot. The large extrapolated 10-year memory window of the As^+-implanted ZrON CTF devices is much better than that of the Si_3N_4/Ir-dot/HfON CTF. It is conceivable that the good confined barrier of double $LaAlO_3$-SiO_2 layer and higher trap density in the As^+-implanted ZrON retain better charge retention ability. The large 10-year retention window with a small 6-nm-ENT trapping layer allows multi-level cells (MLC) storage even at 85°C. As shown in Fig. 6, the excellent 5.1V endurance window was measured after 10^5 cycles under a fast 100 μs speed and low P/E voltages of ±16 V. The excellent 10^5 cycling is vital to allow further endurance improvement in highly scaled CTF device with fewer electrons. Such good endurance is due to the fast 100 μs P/E speed and the existing ΔE_C and ΔE_V for easy tunneling that lead to less stress to $LaAlO_3$-SiO_2 tunnel oxide.

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Table 1 summarizes and compares the memory device characteristics with published data in the literature (5)-(7), (13)-(15). The As^+-implanted ZrON CTF device compares well with other devices, with additional merits of larger memory window, good 85^oC retention, the largest 10^5 endurance window, and fast 100 μs P/E speed.

Conclusion

In summary, the size-dependent trapping effect in nano-dot CTF has been investigated. The better trapping efficiency in As^+-implanted ZrON can be partly attributed to the improved dot size, which is very critical for both ensuring good retention characteristic and providing the feasibility of scaling the ENT.

Acknowledgments

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TABLE I. Comparison of important memory device characteristics for the As^+-implanted ZrON CTF devices (this work) and other MONOS devices.

	P/E condition for retention & cycling	Initial ΔV_{th} (V)	ΔV_{th} (V) for 10-year retention @ 85°C	ΔV_{th} (V) @Cycles
This Work (As-implanted ZrON)	**16V 100μs/ -16V 100μs**	**5.5**	**3.6**	**5.1@10^5**
This Work (Si_3N_4/Ir-dot/HfON)	**16 100μs/ -16V 100μs**	**5.3**	**-**	**-**
TANOS $SiO_2/Si_3N_4/Al_2O_3$/TaN (5)	13.5V 100μs/ -13V 10ms	4.4	2.07	4@10^5
$SiO_2/Si_3N_4/SiO_2$ (6)	13V 10μs/ -12V 1ms	4.5	2.4	3.5@10^4
$SiO_2/Si_3N_4/SiO_2$ (7)	11.5V 3ms/ -11.5V 100ms	1.2	1.1 (@25°C)	1.5@10^4
SiO_2/AlGaN/ $AlLaO_3$/TaN (13)	11V100μs/ -11V 100μs	3.0	1.6	2.3@10^5
SiO_2/HfON/ AlHfO/TaN (14)	8V 100μs/ -8V 100μs	2.5	1.45	2.1@10^5
$SiO_2/LaAlO_3$/HfON/$Si_3N_4/LaAlO_3$/TaN (15)	16V 100μs/ -16V 100μs	5.6	4.1	4.9@10^5

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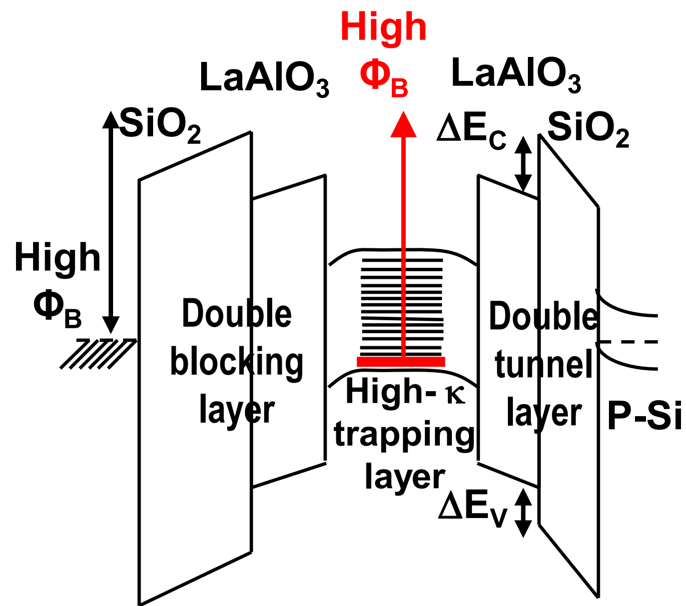

Figure 1. Schematic energy band diagram of the Si_3N_4/Ir-dot/HfON and As^+-implanted ZrON CTF devices.

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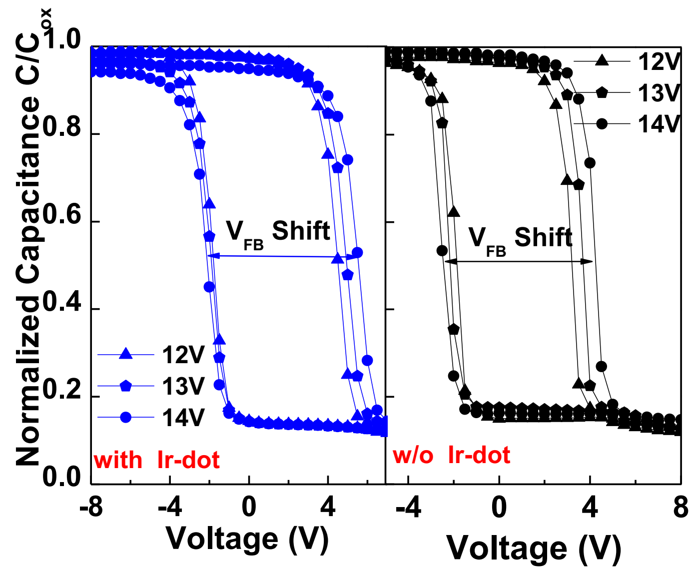
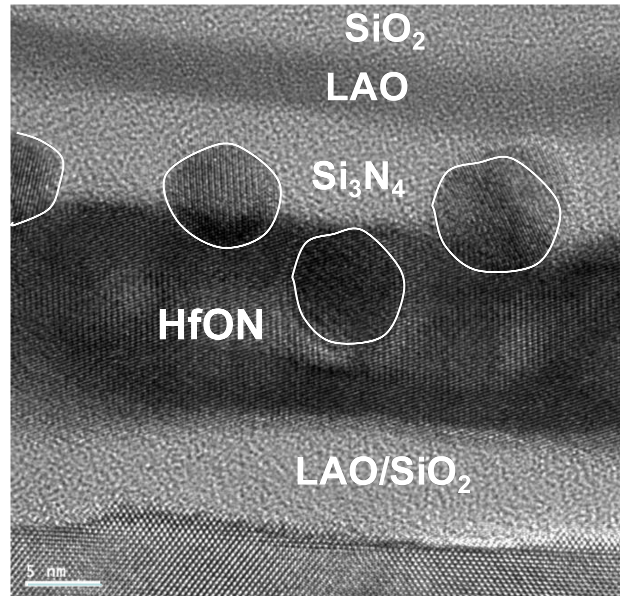


(a)



(b)

Figure 2. (a) *C-V* hysteresis and (b) cross-sectional TEM image of of the Si_3N_4/HfON CT Flash devices with and without Ir-dot.

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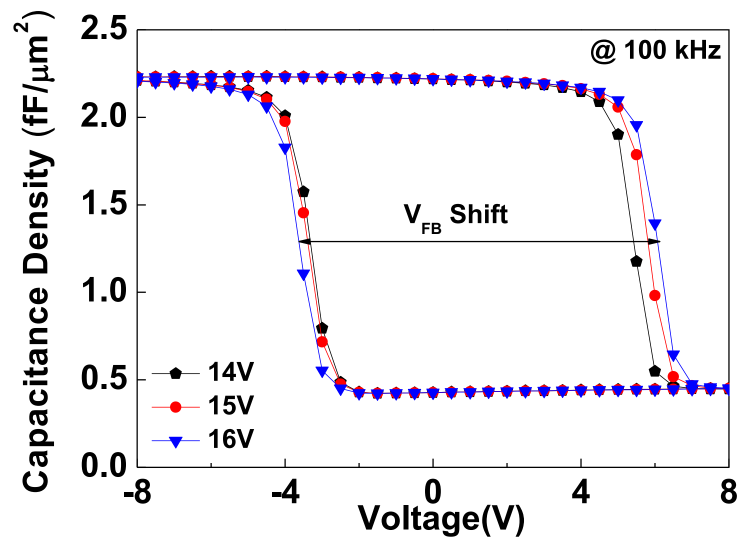

Figure 3. *C-V* hysteresis of As^+-implanted ZrON memory devices.

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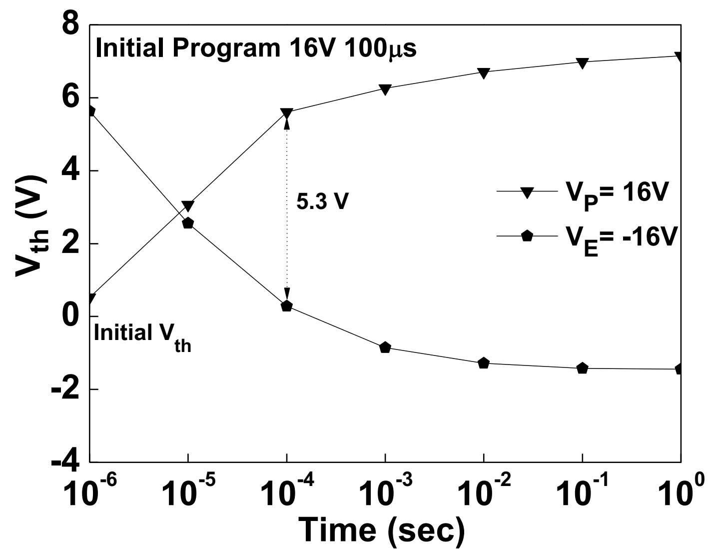
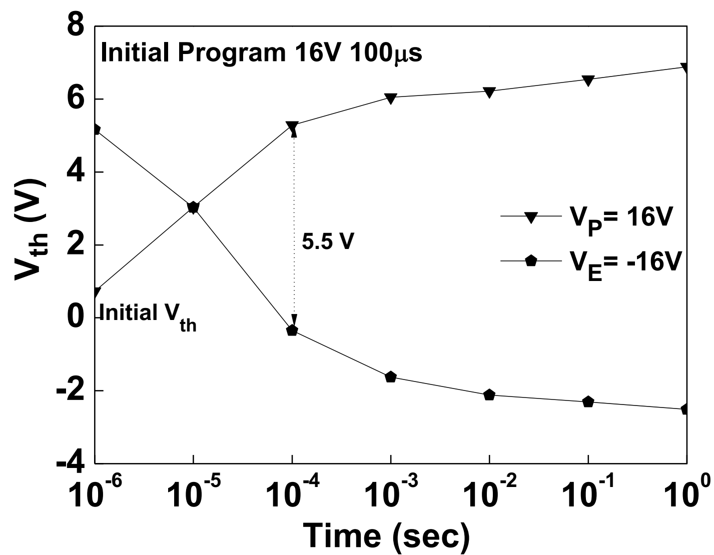


(a)



(b)

Figure 4. V_{th}-P/E characteristics of (a) Si_3N_4/Ir-dot/HfON CT Flash devices and (b) As^+-implanted ZrON CT Flash devices for different times.

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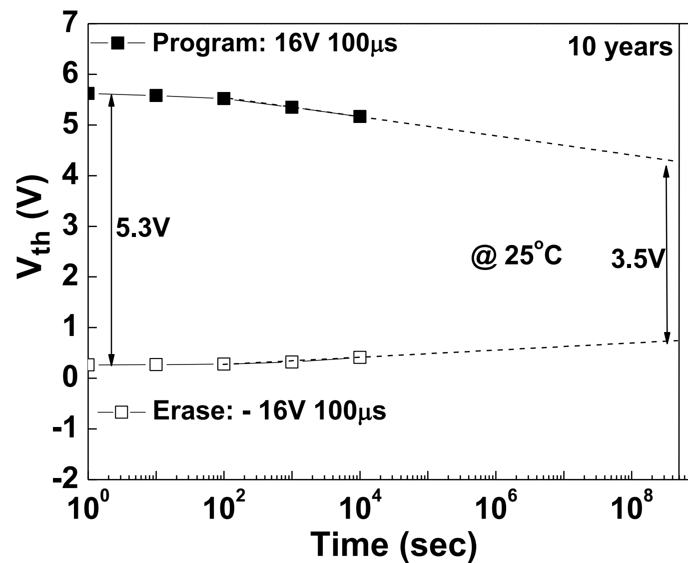
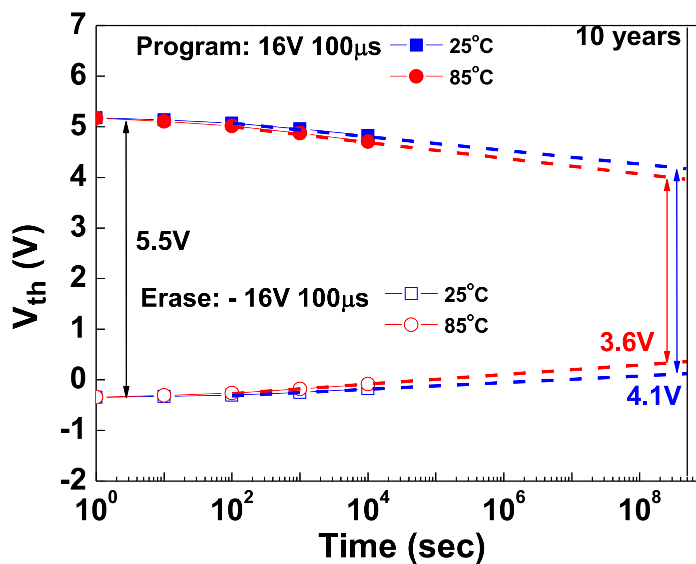


(a)



(b)

Figure 5. Retention characteristics of (a) Si_3N_4/Ir-dot/HfON CT Flash devices and (b) As^+-implanted ZrON CT Flash devices at 25°C and 85°C.

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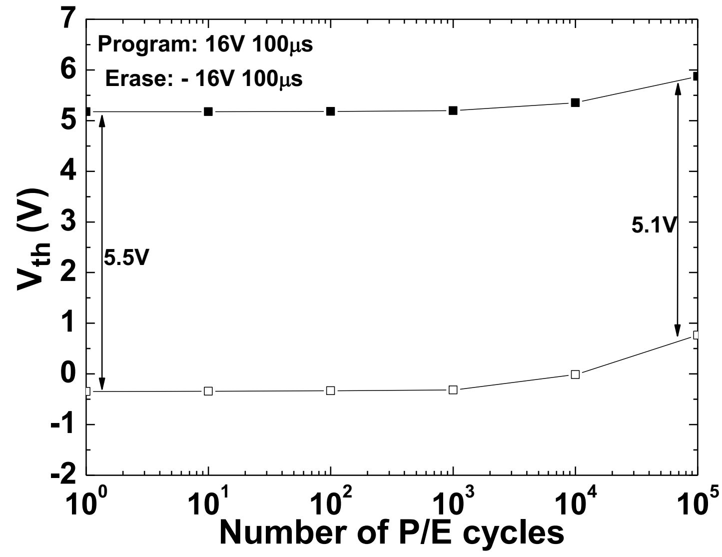

Figure 6. Endurance characteristics of As^{+}-implanted ZrON MONOS NVM devices.

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