Time-Multiplexing Current Balance Interleaved Current-Mode Boost DC-DC Converter for Alleviating the Effects of Right-half-plane Zero

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***Abstract*—In the present study, a time-multiplexing current balance (TMCB) current-mode boost converter is proposed to improve the transient performance. Generally, the crossover frequency of a conventional boost converter is limited to half or less than the right-half-plane (RHP) zero to ensure the system stability. The transient performance of a conventional boost converter is degraded due to its limited bandwidth. The proposed TMCB boost converter extends its bandwidth and moves the RHP zero to a higher frequency to improve the transient performance using two inductors in one channel. Besides, the small signal model of dual phase system which considers cross-couple effect and offset correction is presented. The proposed converter requires an extra inductor and a slight increase in the size of the printed circuit board layout and die size. Using time multiplexing, two inductors were operated in an interleaved phase at a switching frequency of 5 MHz rather than a single inductor system operated at a switching of 10 MHz for the same ripple required. Experimental results show that the TMCB technique is effective in correcting the mismatch in the current of the inductors even if the difference between the inductors is large. Furthermore, the proposed converter can improve the settling time from 52 to 22 μs due to an extended bandwidth.**

***Index Terms*—Boost converter, dc–dc power converter, dual inductor single output boost converter, right-half-plane (RHP) zero, time-multiplexing current balance (TMCB).**

I. Introduction

In recent years, various dc–dc converters, such as the buck, boost, and buck–boost converters, among others, have been used in power systems due to their high efficiency and ease of control. The boost converter, as shown in Fig. 1(a), is a commonly used converter used to convert a low input voltage to a higher output voltage. Especially for harvesting systems, such a low input voltage must be boosted to a higher voltage level for driving a complex next-stage.

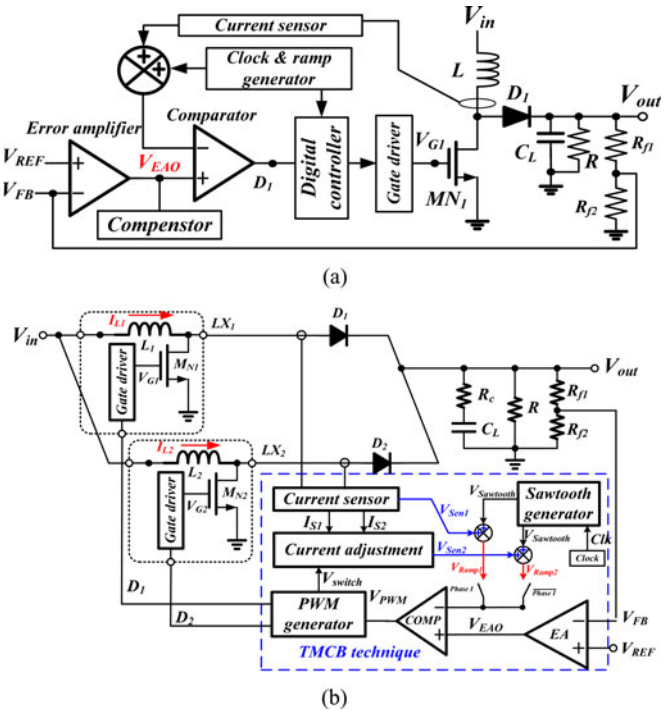

Fig. 1. (a) Conventional current-mode boost converter. (b) Proposed TMCB interleaved current-mode boost converter.

In theory, the maximum bandwidth of a boost converter can be set to 1/10th or 1/15th of the switching frequency to obtain the best transient performance and stability [1]. However, when the output load, duty ratio, and inductor value are increased, the right-half-plane (RHP) zero moves toward low frequencies, and thus toward the crossover frequency ω_T. The phase margin (PM) and the system stability are greatly influenced by the low-frequency RHP zero given by

$$\omega_{z(\mathrm{RHP})} = \frac{D'^2 R}{L}, \text{where } D' = 1 - D, R = \frac{V_{\mathrm{out}}}{I_{\mathrm{load}}} \quad (1)$$

where V_{out} is the output voltage, I_{load} is the output load current, R is the output load resistance, and D is the duty cycle of the pulsewidth modulation control.

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A number of studies have been made on eliminating or reducing the effects of the RHP zero [2]–[8]. Cho *et al.* [2] presented a method to eliminate the RHP zero by selecting the passive component value and satisfying the equation as follows:

$$R_C \cdot C > \frac{L}{R \cdot (1 - D)} \tag{2}$$

where R_C is the equivalent series resistance (ESR) of the output capacitance, C is the output capacitance, D is the duty cycle, L is the inductor, and R is the output load resistance.

The method was achieved using a large output capacitance with a very high ESR value.

Tristate and pseudo conduction current mode controls have been proposed to remove the RHP zero at the cost of an extra one power switch between the input and output nodes [3], [4]. A low switching frequency control [5] has been proposed to eliminate the RHP zero using a low switching frequency. The adaptive voltage position technique and modified hysteretic current control have also been recommended to reduce the RHP zero effect and improve the transient response [6], [7].

The present study proposes an interleaved method with the time-multiplexing current balance (TMCB), as shown in Fig. 1(b), to move the RHP zero to higher frequencies compared with a conventional boost converter, as shown in Fig. 1(a). Although similar dual phase systems used voltage mode control have been proposed in [9], [10]. Those works focused on the high-power or high-current density application and the advantage of high speed is ignored. In addition, those models were presented based on the voltage mode control rather than the current mode control method. The value of the inductor can become half of that of the conventional design due to the interleaved operation of the preposed converter. Thus, the RHP zero can be moved to a higher frequency twice than that of the conventional design (see Fig. 2). Hence, the system bandwidth can be extended from ω_T to ω_T' in order to achieve a fast transient response. The hardware overhead can be reduced using the proposed TMCB technique without sacrificing the performance of the current balance because the TMCB technique needs only one error amplifier similar to the conventional design. The output voltage ripple is guaranteed to be smaller than that of the conventional design if the current balance correctly works on the closed-loop.

Many works have presented the small-signal behavior of a switching converter [11]–[21]. Some studies and their related works have presented the voltage-mode interleaved buck converter or boost converter [22]–[28]. In the current research, an analytic model of the current-mode interleaved boost converter with an average current balance is presented for system stability analysis.

The organization of this study is as follows. The interleaved operation with the TMCB technique is shown in Section II. The small-signal model and system stability analysis are presented in Section III. The circuit implementation is described in Section IV. The experimental results are shown in Section V. Finally, a conclusion is drawn in Section VI.

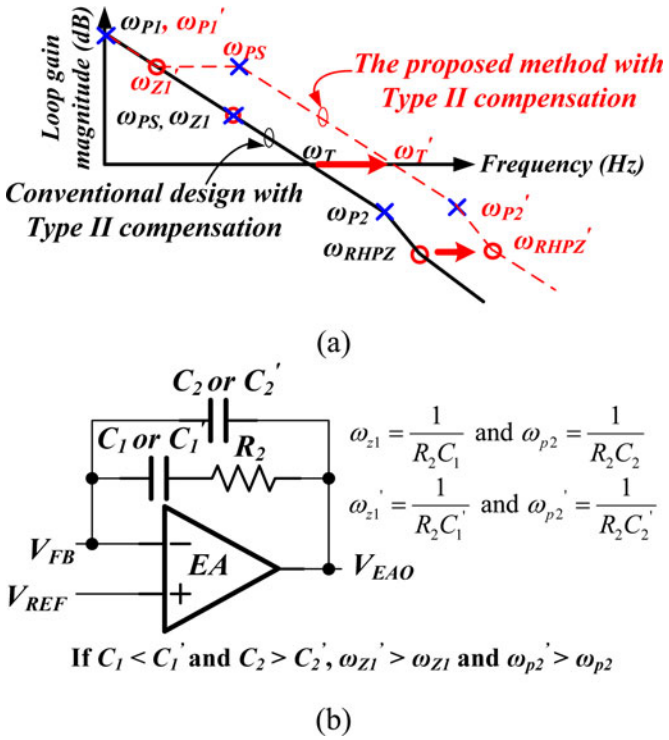

Fig. 2. (a) Extended bandwidth of the proposed boost converter when the RHP zero is moved to higher frequencies. (b) Type II compensator.

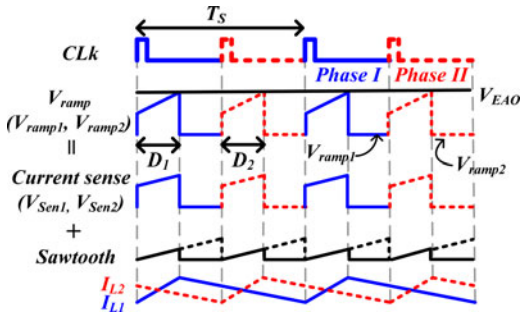

Fig. 3. Determination of the duty cycle in the TMCB technique.

II. Operation of the Interleaved Boost Converter With the TMCB

The proposed interleaved boost converter needs two inductors L_1 and L_2 to move the RHP zero to higher frequencies. In addition, two Schottky diodes D_1 and D_2 are necessary for the simple implementation of asynchronous rectifiers. Phase I is the operation period of the master channel composed of L_1, D_1, and a power MOSFET M_{N1}. Phase II is the operation period of the slave channel composed of L_2, D_2, and a power MOSFET M_{N2}. It was difficult to ensure the perfect matching between the two phases, and thus the current balance was worth. The TMCB technique was proposed to guarantee the current balance between the two phases. In the converter, a simple on-chip clock generator was built to provide a single clock without the synchronous issue between the two phases.

Similar to the conventional architecture, the duty cycle is determined using the comparison of the ramp signal V_{Ramp} and

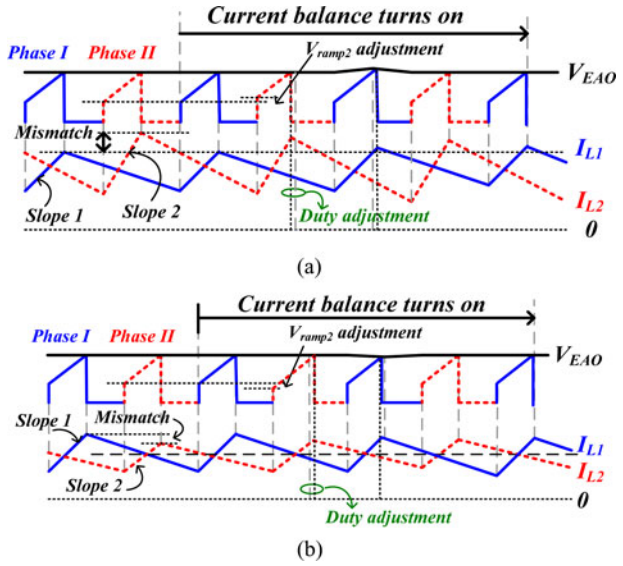

Fig. 4. If the driving current in phase I is larger than that in phase II, the TMCB technique adjusts the ramp slope of the phase II to increase the driving current in phase II when the operation is opposite in (a) and (b).

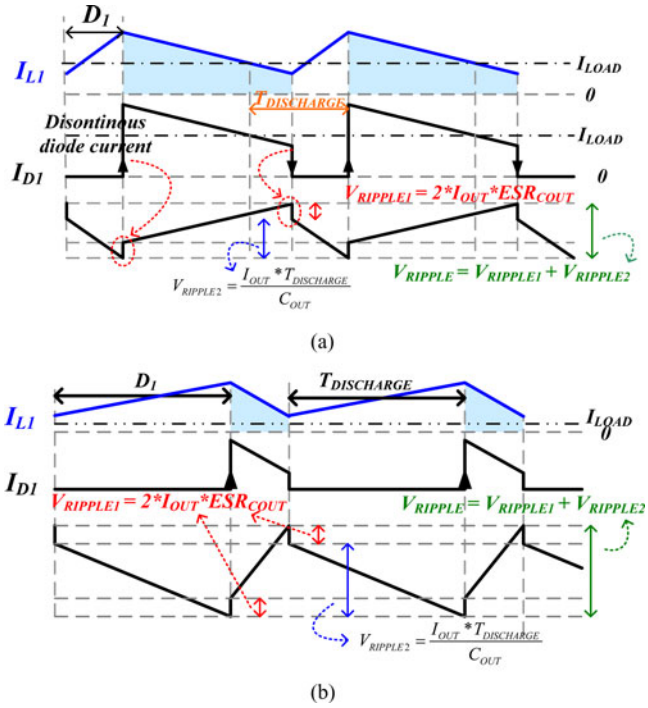

Fig. 5. Output ripple of the conventional boost converter: (a) when the duty cycle is less than 50%, (b) when the duty cycle is greater than 50%.

the error signal $V_{\rm EAO}$. The two phases share an error amplifier and a comparator. With a reduced hardware overhead, the dual-phase converter with a good current balance can achieve a fast transient response without being greatly affected by the RHP zero.

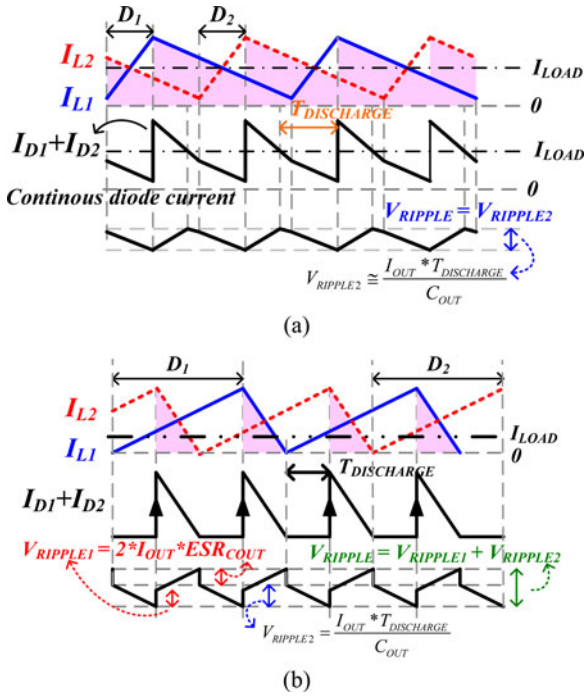

Fig. 6. Output ripple of the proposed boost converter: (a) when the duty cycle is less than 50%, (b) when the duty cycle is greater than 50%.

A. Compensation Design for Extending the Bandwidth

Fig. 2 shows the comparison of the bandwidth between the conventional and proposed converters. Usually, a Type II compensator is used to make the closed-loop transfer function sharp enough and ensure high low-frequency gain and adequate PM in a conventional current-mode boost converter. In the proposed converter, the compensation pole ω_{P1} at the origin substitutes the system pole, $\omega_{\rm PS}$ (i.e., $2/RC_L$) as the dominant pole. The new compensator for the proposed interleaved design with the TMCB technique is designed to have a maximum ω_T' because the RHP zero $\omega_{\rm RHPZ}'$ is located at high frequencies. Thus, a higher compensation pole and zero, ω_{Z1}' and ω_{p2}', respectively, can be achieved because the interleaved method uses a small inductor.

B. Operation of the Proposed TMCB Technique for Current Balance

The transient response time can be improved by a higher crossover frequency. However, the current balance is another design issue that needs to be solved to ensure a fast transient response without having subharmonic oscillation or longer settling time problems. The subharmonic oscillation is due to the sampling effect if the unity gain frequency of the current balance loop approaches one-tenth of the switching frequency [18], [20], [21], [29]. Besides, the longer setting time problem is caused by low bandwidth or slow response current balance loop. The offset current between the two phases, still results in the slave channel, affects the master channel even if the output voltage achieves its regulated value while the transient load is mainly supported by the master channel. The phenomena

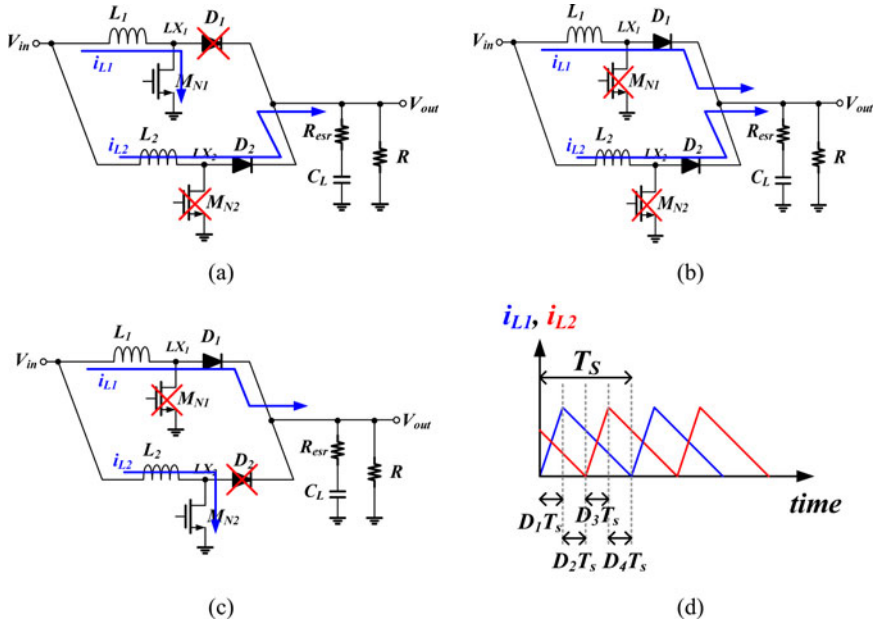

Fig. 7. Steady state analysis of the proposed converter in (a) state 1, (b) state 2 and state 4, and (c) state 3. (d) Duty ratio of the proposed converter.

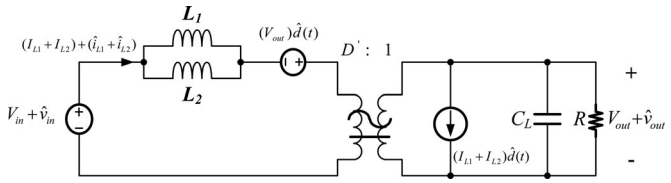

Fig. 8. Simplified power stage model of the proposed converter when the duty cycles are equal for each channel.

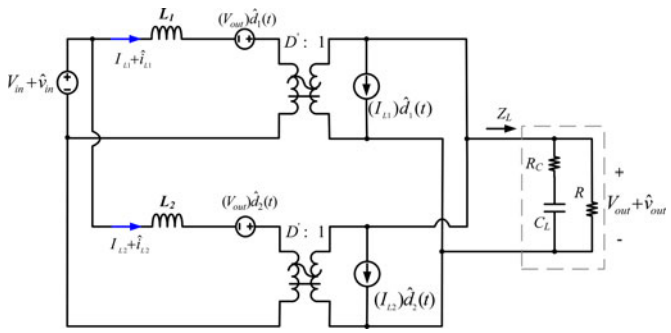

Fig. 9. Equivalent power stage model of the proposed converter if the duty cycle is not equivalent in each channel.

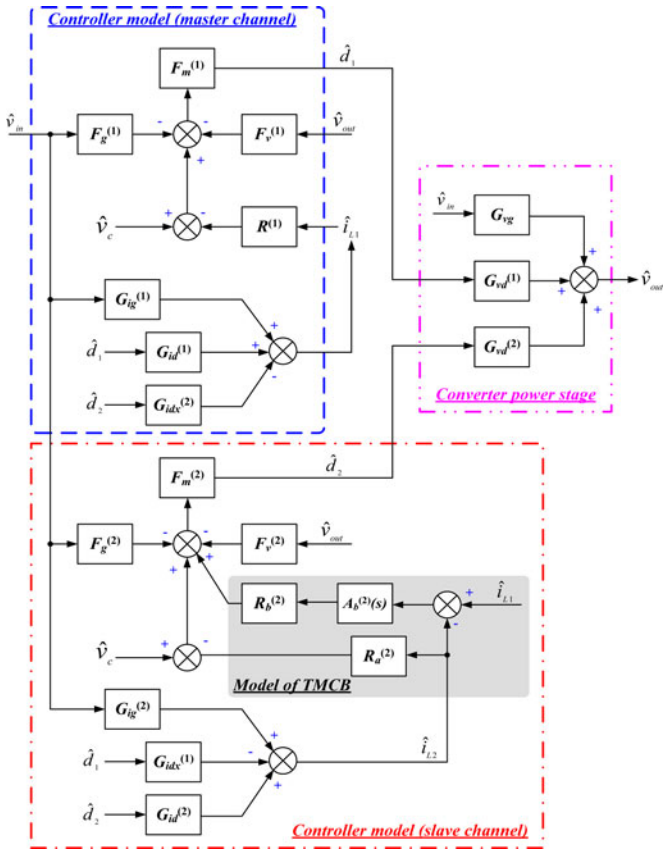

Fig. 10. Block diagram for the proposed interleaved current mode boost converter.

are simulated and presented in Section III. In Fig. 3, the proposed TMCB technique uses a clock with the time-multiplexing idea to modulate the duty cycles of the two phases. This is based on the main concept that there are two interleaved ramps generated by the TMCB technique, as shown in Fig. 3.

The mismatches between the two phases can lead to an enormously unbalanced current distribution. Thus, the current balance circuit is demanded to compensate the mismatches for inductor current unbalancing [10]. The proposed TMCB technique was used to adjust the ramp slope for the current balance in dual-phase operation, as shown in Fig. 4.

As can be seen in Fig. 4(b), the current in phase I is larger than that in phase II. The decrease in ramp voltage can enlarge the duty cycle and increase the current driving capability. On the contrary, the increase in ramp slope can lead to a smaller duty cycle and decrease the current driving capability. Therefore, the current balance can be achieved by comparing the voltage of the modified ramps with the same error signal.

TABLE I
TRANSFER FUNCTIONS OF THE PROPOSED CONVERTER

$G_{vd}^{(1)}$ (duty-to-output of master channel)	$G_{vd}^{(1)}=\frac{\hat{v}_{out}}{\hat{d}_1}=\frac{V_{out}}{D'}\cdot\frac{(sR_CC_L+1)\left(1-\frac{sL_1}{D'^2\cdot 2R}\right)}{s^2\frac{L_1C_L(2R+R_C)}{D'^2\cdot 2R}+s\left(\frac{L_1}{D'^2\cdot 2R}+R_CC_L\right)+1}$
$G_{vd}^{(2)}$ (duty-to-output transfer function of slave channel)	$G_{vd}^{(2)}=\frac{\hat{v}_{out}}{\hat{d}_2}=\frac{V_{out}}{D'}\cdot\frac{(sR_CC_L+1)\left(1-\frac{sL_2}{D'^2\cdot 2R}\right)}{s^2\frac{L_2C_L(2R+R_C)}{D'^2\cdot 2R}+s\left(\frac{L_2}{D'^2\cdot 2R}+R_CC_L\right)+1}$
$G_{id}^{(1)}$ (duty-to-inductor-current transfer function of the master channel)	$G_{id}^{(1)}=\frac{\hat{i}_{L1}}{\hat{d}_1}=\frac{V_{out}}{D'^2R}\cdot\frac{(1+s(R+R_C)C_L)}{s^2\frac{L_1C_L(2R+R_C)}{D'^2\cdot 2R}+s\left(\frac{L_1}{D'^2\cdot 2R}+R_CC_L\right)+1}$
$G_{id}^{(2)}$ (duty-to-inductor-current transfer function of the slave channel)	$G_{id}^{(2)}=\frac{\hat{i}_{L2}}{\hat{d}_2}=\frac{V_{out}}{D'^2R}\cdot\frac{(1+s(R+R_C)C_L)}{s^2\frac{L_2C_L(2R+R_C)}{D'^2\cdot 2R}+s\left(\frac{L_2}{D'^2\cdot 2R}+R_CC_L\right)+1}$
$G_{idx}^{(1)}$ (duty-to-other-inductor-current)	$G_{idx}^{(1)}=\frac{\hat{i}_{L2}}{\hat{d}_1}=\frac{V_{out}}{D'^2\cdot 2R}\cdot\frac{s^2\frac{L_1C\cdot R_C}{D'^2\cdot 2R}+s\left(\frac{L_1}{D'^2\cdot 2R}-R_CC\right)-1}{\left[s^2\frac{L_1C(2R+R_C)}{D'^2\cdot 2R}+s\left(\frac{L_1}{D'^2\cdot 2R}+R_CC\right)+1\right]}$
$G_{idx}^{(2)}$ (duty-to-other-inductor-current)	$G_{idx}^{(2)}=\frac{\hat{i}_{L1}}{\hat{d}_2}=\frac{V_{out}}{D'^2\cdot 2R}\cdot\frac{s^2\frac{L_2C\cdot R_C}{D'^2\cdot 2R}+s\left(\frac{L_2}{D'^2\cdot 2R}-R_CC\right)-1}{\left[s^2\frac{L_2C(2R+R_C)}{D'^2\cdot 2R}+s\left(\frac{L_2}{D'^2\cdot 2R}+R_CC\right)+1\right]}$

TABLE II
FEED-FORWARD GAIN AND RELATIVE PARAMETERS OF THE PROPOSED CONVERTER

Master channel	Input voltage-to-duty cycle feed-forward gain $F_g^{(1)}$	$F_g^{(1)}=\frac{(2D-1)\cdot T_S}{2L_1}$
	Output voltage-to-duty cycle feed-forward gain $F_v^{(1)}$	$F_v^{(1)}=(\frac{D'^2}{2L_1})\cdot T_S$
	Modulation gain $F_m^{(1)}$	$F_m^{(1)}=\frac{1}{(M_C)\cdot T_S}$
Slave channel	Input voltage-to-duty cycle feed-forward gain $F_g^{(2)}$	$F_g^{(2)}=(\frac{D}{2L_1}-\frac{D'}{2L_2})\cdot T_s$
	Output voltage-to-duty cycle feed-forward gain $F_v^{(2)}$	$F_v^{(2)}=\left(\frac{D'^2}{2L_2}\right)\cdot T_s$
	Modulation gain $F_m^{(2)}$	$F_m^{(2)}=\frac{1}{\left(M_C+\frac{M_{1A}}{2}+\frac{M_{2A}}{2}\right)\cdot T_s}$
	Pseudo average current modification term I_{bal}	$I_{bal}=\frac{(M_{1A}-M_{2a})\cdot DT_S}{2}$
Parameters	Inductor current *(I_{L1})* slope during charge phase of the M_{1A}	$M_{1A}=\frac{V_{in}}{L_1}$
	Inductor current *(I_{L2})* slope during charge slope of the M_{2A}	$M_{2A}=\frac{V_{in}}{L_2}$
	Artificial ramp slope of the M_C	$k\cdot M_{2A}$, $k>1/2$

C. Output Ripple Consideration

Low output ripple of dual-phase system is another advantage than single inductor system. Fig. 5 shows the output ripple of the conventional boost converter. The ripple voltage V_{RIPPLE} contains the ripple from the ESR at the output capacitor V_{RIPPLE1} as well as the ripple V_{RIPPLE2} from the charging/discharging of the output capacitor. Fig. 5(a) and (b) shows the output ripple when the duty was less than 50% and greater than 50%, respectively. The output V_{RIPPLE} contains the V_{RIPPLE1} regardless of the duty. Fig. 6 shows the output ripple of the proposed converter. The diode current (I_{D1}+I_{D2}) was continuous when the duty was less than 50%, as shown in Fig. 6(a). Due to the continuous diode current, the output ripple can be reduced to V_{RIPPLE2} during the charge/discharge phase compared with the conventional boost converter. Although the diode current (I_{D1}+I_{D2}) was not continuous when the duty was greater than 50%, the output ripple of the proposed converter was still smaller than that of the conventional converter because the average inductor

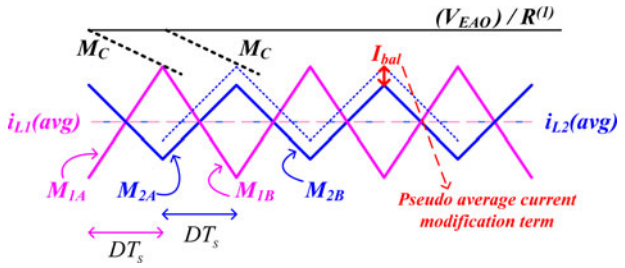

Fig. 11. Relationship between i_{L1}, i_{L2}, and $V_{\rm EAO}$ of the proposed converter.

current, as shown in Fig. 6(b), was half of that of the conventional converter. In addition, the discharge period $T_{\rm DISCHARGE}$, of the output capacitance was shorter than that shown in Fig. 5(b).

III. Small Signal Model

A. Simple Power Stage Model

From Fig. 1(a), the operation of the proposed converter can be classified into four states, as shown in Fig. 7. In state 1, as shown in Fig. 7 (a), the power switch M_{N1} is ON with the increasing inductor current I_{L1}. On the other hand, the power switch M_{N2} is OFF when the inductor current I_{L2} ramps down to charge the output capacitor C_L.

In state 2, as shown in Fig. 7(b), M_{N1} and M_{N2} are OFF and the inductor currents I_{L1} and I_{L2} ramp down to charge C_L. In state 3, as shown in Fig. 7(c), M_{N1} is OFF and inductor current I_{L1} ramps down to charge C_L. M_{N2} is ON, I_{L2} is increased. The status of state 4 is similar to that of state 2.

From the four states mentioned earlier, the state space equation can be separately established as

$$\dot{x}(t) = A_n x(t) + B_n u(t) \tag{3}$$

where *x(t)* is the state vector and expressed as $[i_{L1} \quad i_{L2} \quad V_{\rm out}]$, *u(t)* is the input vector defined as $V_{\rm in}(t)$, and *n* is the state.

The on-resistance r_1 and r_2 of power switches M_{N1} and M_{N2} are assumed to be identical to r_a, which is the ESR of the output capacitor, and on-resistance of diodes D_1 and D_2 are neglected in this case.

The node equation in state 1 can be expressed in the matrix form as follows:

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{i}_{L2} \\ \dot{V}_{\rm out} \end{bmatrix} = \begin{bmatrix} -\frac{r_1}{L_1} & 0 & 0 \\ 0 & 0 & -\frac{1}{L_2} \\ 0 & \frac{1}{C_L} & -\frac{1}{RC_L} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_{\rm out} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & \frac{1}{L_2} & 0 \end{bmatrix} [V_{\rm in}]$$

The matrixes in states 2–4 can also be expressed in similar forms as follows:

$$A_2 = A_4 = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} \\ 0 & 0 & -\frac{1}{L_2} \\ \frac{1}{C_L} & \frac{1}{C_L} & -\frac{1}{RC_L} \end{bmatrix},$$

$$A_3 = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} \\ 0 & -\frac{r_2}{L_2} & 0 \\ \frac{1}{C_L} & 0 & -\frac{1}{RC_L} \end{bmatrix}, \text{and}$$

$$B_1 = B_2 = B_3 = B_4 = \begin{bmatrix} \frac{1}{L_1} & \frac{1}{L_2} & 0 \end{bmatrix}.$$

For simplification, it was assumed that the duty ratios D_1 and D_3 in Fig. 7(d) have the same values in steady state. Hence, (4)–(6) can be derived as follows:

$$D_1 = D_3 = D \tag{4}$$

where

$$D' = (1 - D) = (D_2 + D_3 + D_4) = \frac{V_{\rm out}}{V_{\rm in}} \tag{5}$$

and

$$D_1 + D_2 + D_3 + D_4 = 1. \tag{6}$$

According to the state-space averaged theory and ignoring the second-order nonlinear term, a linearized ac model can be obtained as follows:

$$\hat{x}(t) = A\hat{x}(t) + B\hat{u}(t) + \{(A_d)X + (B_d)U\}\,\hat{d}(t) \tag{7}$$

where *A* is equal to$(D_1 \cdot A_1 + D_2 \cdot A_2 + D_3 \cdot A_3 + D_4 \cdot A_4)$, A_d is equal to $(A_1 + A_3 - A_2 - A_4)$, *B* is equal to $(D_1 \cdot B_1 + D_2 \cdot B_2 + D_3 \cdot B_3 + D_4 \cdot B_4)$, and B_d is equal to $(B_1 + B_3 - B_2 - B_4)$.

The matrixes are expressed as follows:

$$A = \begin{bmatrix} 0 & 0 & -\frac{(D_2 + D_3 + D_4)}{L_1} \\ 0 & 0 & -\frac{(D_1 + D_2 + D_4)}{L_2} \\ \frac{(D_2 + D_3 + D_4)}{C_L} & \frac{(D_1 + D_2 + D_4)}{C_L} & -\frac{(D_1 + D_2 + D_3 + D_4)}{RC_L} \end{bmatrix},$$

$$B = \begin{bmatrix} \frac{1}{L_1} & \frac{1}{L_2} & 0 \end{bmatrix},$$

$$A_d = \begin{bmatrix} 0 & 0 & \frac{1}{L_1} \\ 0 & 0 & \frac{1}{L_2} \\ -\frac{1}{C_L} & -\frac{1}{C_L} & 0 \end{bmatrix}, \quad \text{and} \quad B_d = 0.$$

In the scalar form, the vectors in (7) can be expressed as follows:

$$L_1 \frac{d\hat{i}_{L1}(t)}{dt} = \hat{V}_{\rm in}(t) - D'\hat{V}_{\rm out}(t) + (V_{\rm out})\hat{d}(t) \tag{8}$$

$$L_2 \frac{d\hat{i}_{L2}(t)}{dt} = \hat{V}_{\rm in}(t) - D'\hat{V}_{\rm out}(t) + (V_{\rm out})\hat{d}(t) \tag{9}$$

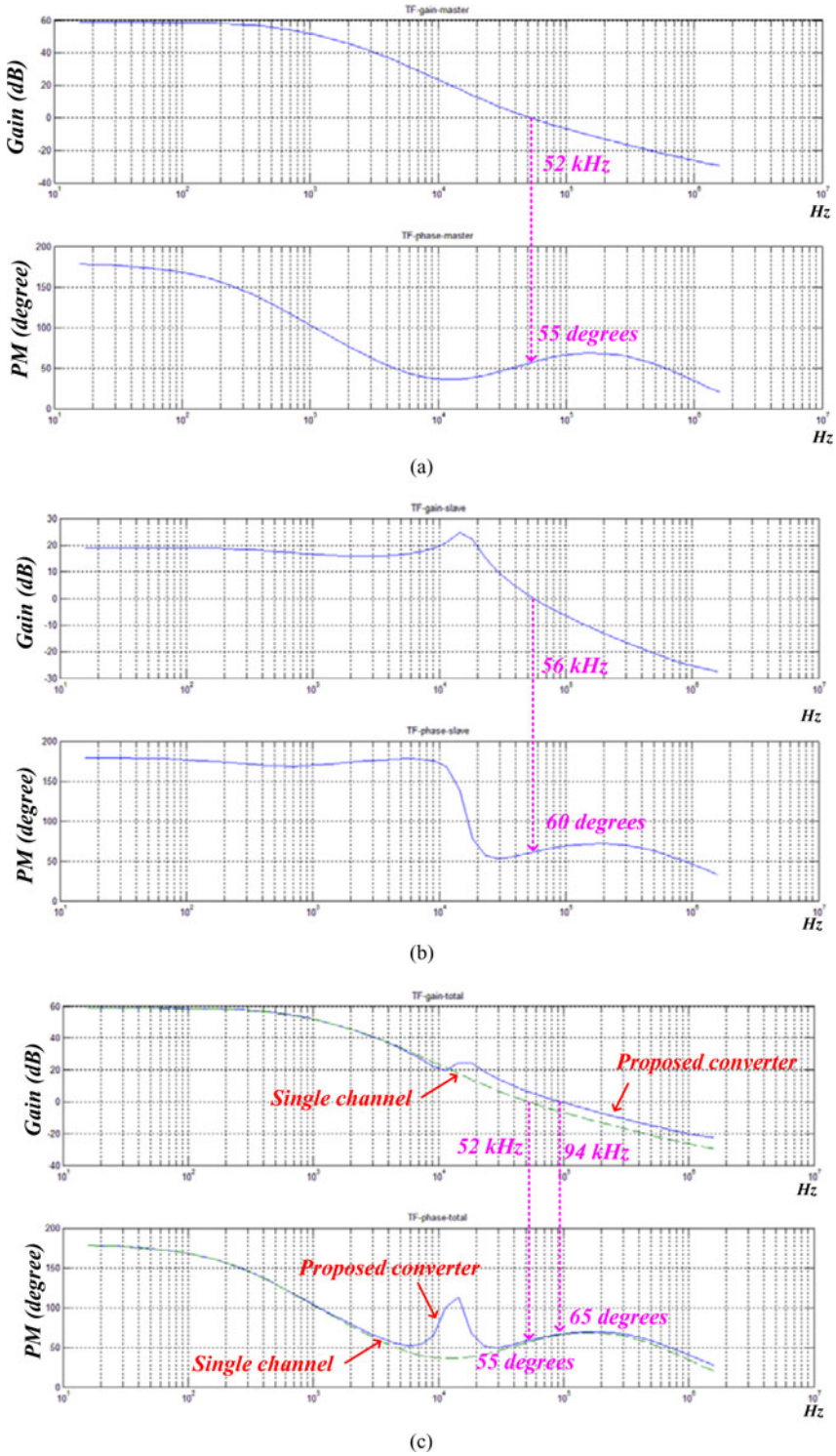

Fig. 12. (a) Bode plot of the master channel. (b) Bode plot of the slave channel. (c) Bode plots of the conventional and the proposed converter.

$$C_L \frac{d\hat{V}_{\text{out}}(t)}{dt} = D' \left[\hat{i}_{L1}(t) + \hat{i}_{L2}(t)\right] - \frac{\hat{V}_{\text{out}}(t)}{R} - (I_{L1} + I_{L2})\hat{d}(t). \quad (10)$$

Consequently, the equivalent circuit model can be constructed, as shown in Fig. 8. $V_{\text{in}} + \hat{v}_{\text{in}}$ is the input voltage with the perturbation, L_1 and L_2 are the inductor values, $V_{\text{out}} + \hat{v}_{\text{out}}$ is the output voltage with the perturbation, I_{L1} and I_{L2} are the dc inductor currents, D is the duty cycle in steady state, R is the equivalent loading resistance, and C_L is the output capacitance.

Using the simplified power stage model, the RHP zero can be derived as (11), and the effective inductor value is reduced to half of the original value. The effective inductor value is

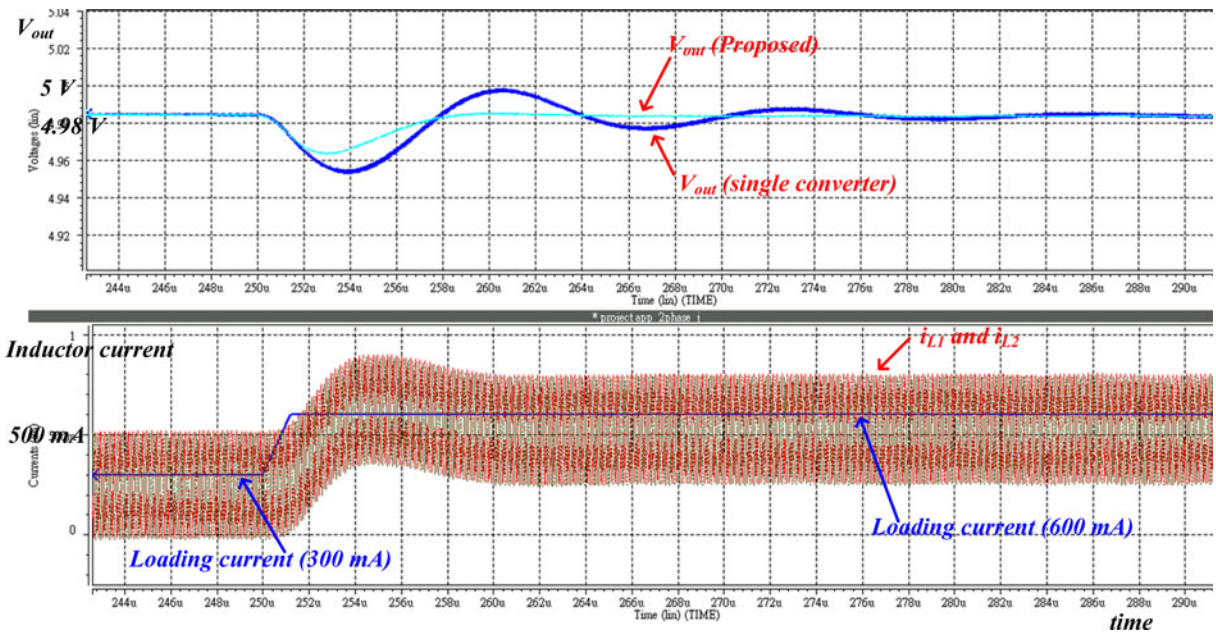

Fig. 13. Simulation waveforms of the single channel converter and the proposed interleaved converter.

TABLE III
DESIGN PARAMETERS AND SIMULATION CONDITIONS

Input voltage	**3.1 V**
Output voltage	**5 V**
Inductor (L_a/L_b)	**0.47 µH /0.47 µH**
Output capacitors (C_1)	**10 µF**
Switching frequency	**5 MHz**
ESR of output capacitor	**10 mΩ**
Loading current	**400 mA**

different from the result, which is equal to one, obtained by Xu *et al*. [10]. In addition, the RHP zero in the interleaved converter is half of that in the conventional single inductor boost converter

$$\omega_{Z(\mathrm{RHP})} = \frac{D'^2 R}{L_1 // L_2}. \tag{11}$$

B. Power Stage Model With Unequal Duty Cycle

If the duty cycles are not equal in each channel, the equivalent power stage model is modified, as shown in Fig. 9. The parameter definitions $\hat{d}_1$ and $\hat{d}_2$ are the perturbations for each channel, Z_L is the impedance seen at the output node, and the rest parameters are defined as previously discussed.

According to the equivalent power stage model, the individual duty-to-output transfer function G_{vd} and the duty-to-inductor-current transfer function G_{id} can be derived. Furthermore, the cross-couple term of the duty-to-other-inductor-current transfer function $G_{\mathrm{idx}}^{(1)}$ implies how the duty of the master channel d_1 affects the slave channel inductor current i_{L2}. On the other hand, the cross-couple term of the duty-to-other-inductor-current $G_{\mathrm{idx}}^{(2)}$ implies how the duty of the slave channel d_2 affects the master channel inductor current i_{L1}. With a carefully designed current balance mechanism, the average of each channel was mostly kept similar to each other, and the bandwidth of the TMCB was wide enough without affecting the transient response.

The duty-to-output transfer function of the master channel $G_{\mathrm{vd}}^{(1)}$ can be obtained when the independent voltage V_{in} and d_2 are assumed to be shorted to the ground and zero, respectively. Similarly, the duty-to-output transfer function of the slave channel $G_{\mathrm{vd}}^{(2)}$ can be derived. In addition, using the KCL theorem, the net current at the output node is zero. The cross-couple term of duty-to-other-inductor-current transfer functions, $G_{\mathrm{idx}}^{(1)}$ and $G_{\mathrm{idx}}^{(2)}$, can be obtained. Table I shows the summary of the power stage model transfer function of the proposed converter.

C. Controller Model and Transfer Function of the Proposed Converter

Fig. 10 shows the block diagram of the proposed interleaved current model boost converter. The block diagram is composed of three parts, including the converter power stage, and the controller models of master and slave channels. The power stage transfer functions are shown in Table I. In addition, the controller block diagrams can be determined using the relationship of the control signal V_{EAO} and inductor currents I_{L1} and I_{L2}. Two separate controller models are necessary to model the different values of duty cycle or the inductor of each channel. Moreover, the TMCB mechanism is derived and included in the slave channel controller model. As can be seen in Fig. 10, $R^{(1)}$, $R^{(2)}$, and $R_b^{(2)}$ are the current-to-voltage ratios; $\hat{V}_C$ is the small-signal part of the V_{EAO}. $A_b^{(2)}(s)$ is the transfer function of the current balance mechanism, including the error amplifier and the compensator. $F_g^{(1)}$, $F_g^{(2)}$, $F_v^{(1)}$, and $F_v^{(2)}$ are the feed-forward term from the input or the output voltage to the duty cycle; and $F_m^{(1)}$ and $F_m^{(2)}$ are the modulation gains of the two channels, including the slope compensation factor. Table II

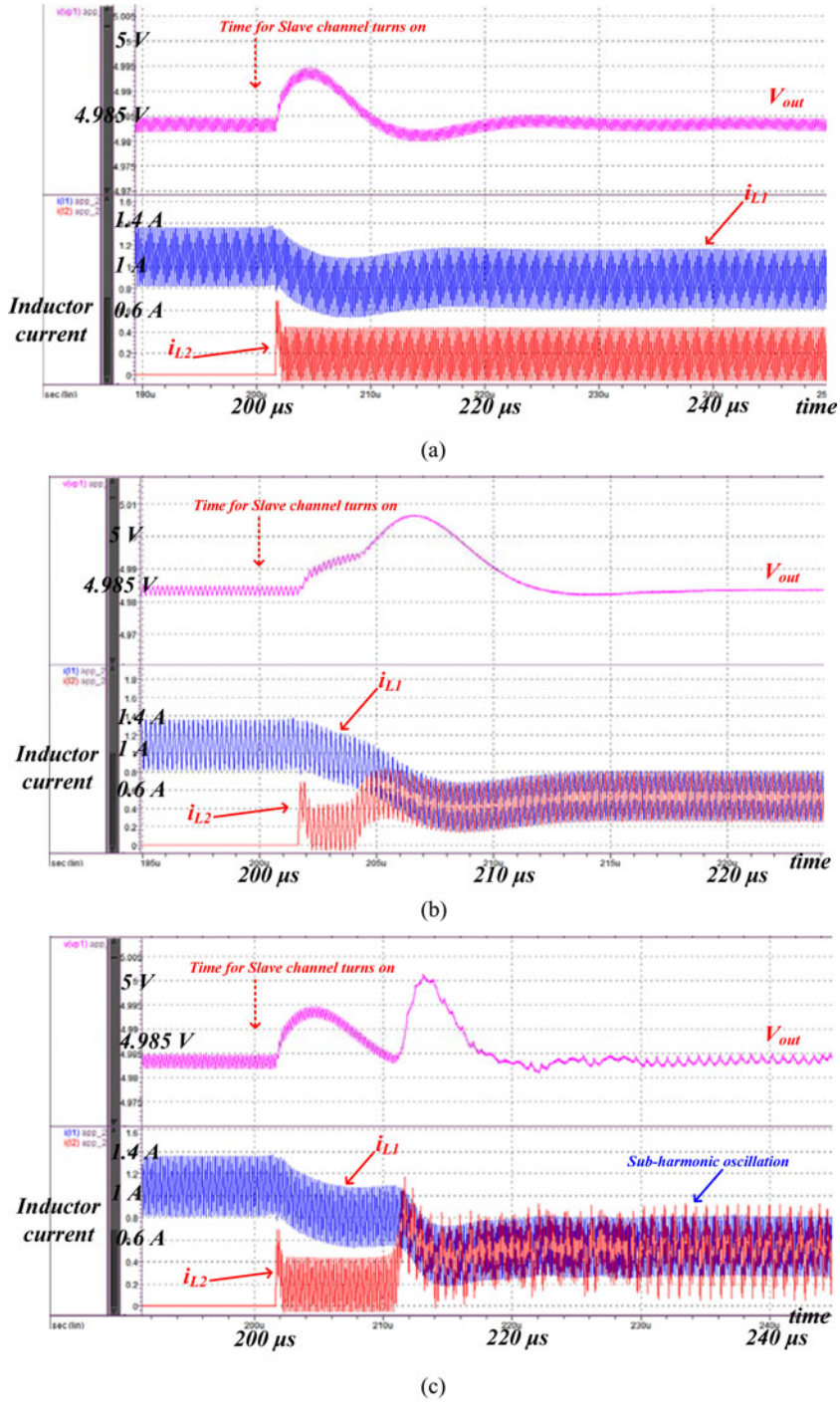

Fig. 14. (a) Simulation waveforms of the TMCB mechanism with a low-gain $A_b{}^{(2)}(s)$. (b) Simulation waveforms with a suitable design of the TMCB. (c) Simulation waveforms of the TMCB with an ultrahigh bandwidth.

shows the summary of the feed-forward gain of the proposed converter.

Fig. 11 shows the relationship between i_{L1}, i_{L2}, and $V_{\rm EAO}$ of the proposed converter. Due to the current balance mechanism, the average inductor current of i_{L1} and i_{L2} can be forced to have similar values with a pseudo average current modification term I_{bal}. According to the relationship shown in Fig. 11, I_{bal} can be expressed by M_{1A} and M_{1B} shown in Table II. In addition, $F_g^{(2)}$, $F_v^{(2)}$, and $F_m^{(2)})$ can be obtained after the process of perturbation and linearization. The modulation gain $F_m^{(2)}$ and the feed-forward gains $F_g^{(2)}$ and $F_v^{(2)}$ are different from those in the master channel due to the TMCB mechanism. The difference came from the modulation gain has the M_{1A} and the M_{2A} in the denominator.

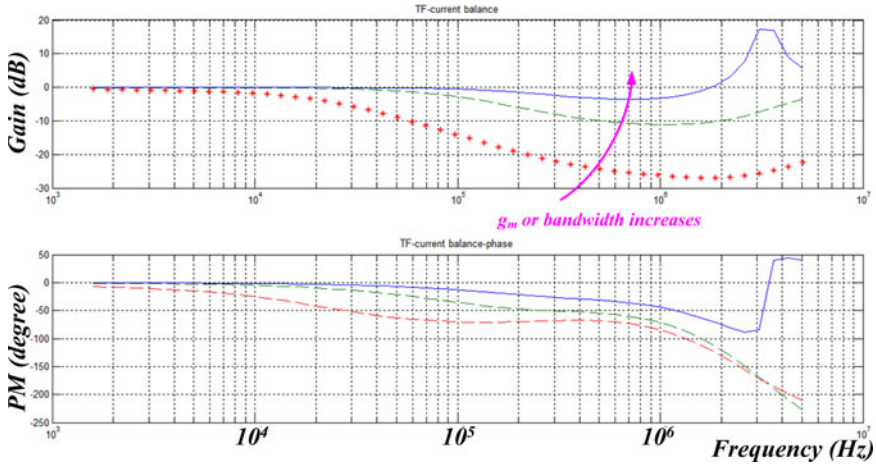

Fig. 15. Bode plot of current balance loop in closed form.

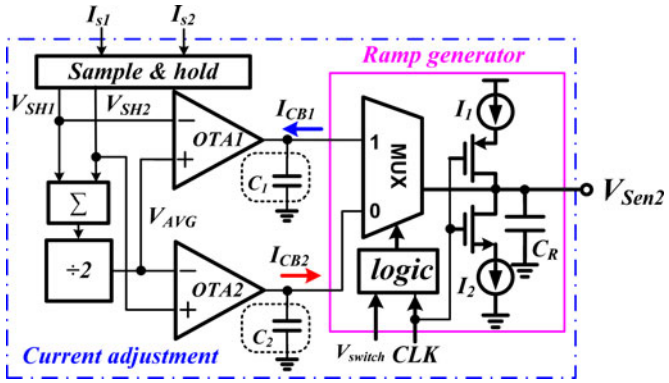

Fig. 16. Schematic diagram of the TMCB circuit.

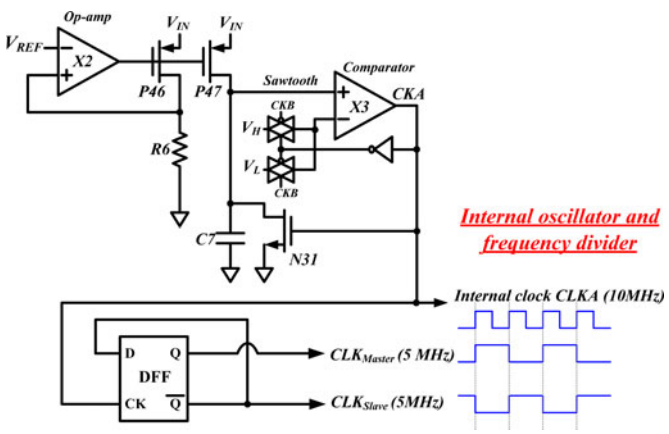

Fig. 17. Schematic diagrams of the internal oscillator and ramp generator.

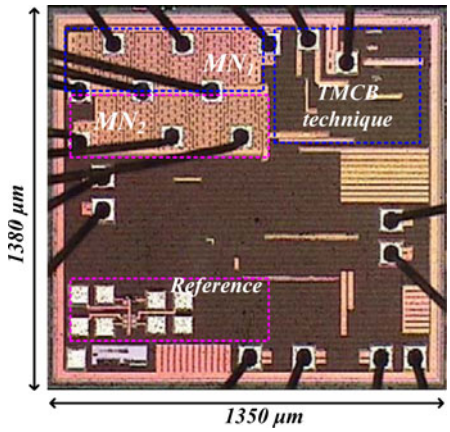

Fig. 18. Chip micrograph of the proposed converter.

As can be seen in Fig. 10, the control-to-output voltage in the closed-loop transfer function of the master channel T_{CL_M} can be derived as (12) to determine the stability of the master channel, as shown (12), at the bottom of this page. The closed-loop transfer function of the slave channel T_{CL_S} can also be derived as (13), shown at the bottom of the next page. The transfer function T_{CL_S} is used to verify the stability of the slave channel with the TMCB mechanism. The closed-loop transfer function of the proposed converter T_{CL_T} is the summation of (12) and (13). Besides, the closed-loop transfer function of the current balance loop i_{L2}/i_{L1} is expressed in (14), and (15) expresses the sampling effect at high frequency. Fig. 12(a) and (b) shows the Bode plots of the master and slave channels, respectively, using MATLAB. The simulation conditions and design parameters are summarized in Table III. Fig. 12(c) shows the Bode plots of the proposed converter and conventional single channel converter at the same loading of 400 mA. The proposed converter has a higher bandwidth compared with the conventional converter because the proposed converter has a higher loop gain derived

$$T_{CL_M} = \frac{F_m^{(1)} \cdot R^{(1)}}{\left(G_{\mathrm{id}}^{(1)} F_m^{(1)} / G_{\mathrm{vd}}^{(1)}\right) - \left(G_{\mathrm{idx}}^{(2)} \cdot F_m^{(1)} / G_{\mathrm{vd}}^{(2)}\right) - F_v^{(1)} F_m^{(1)} + \left(1/G_{\mathrm{vd}}^{(1)}\right)}. \tag{12}$$

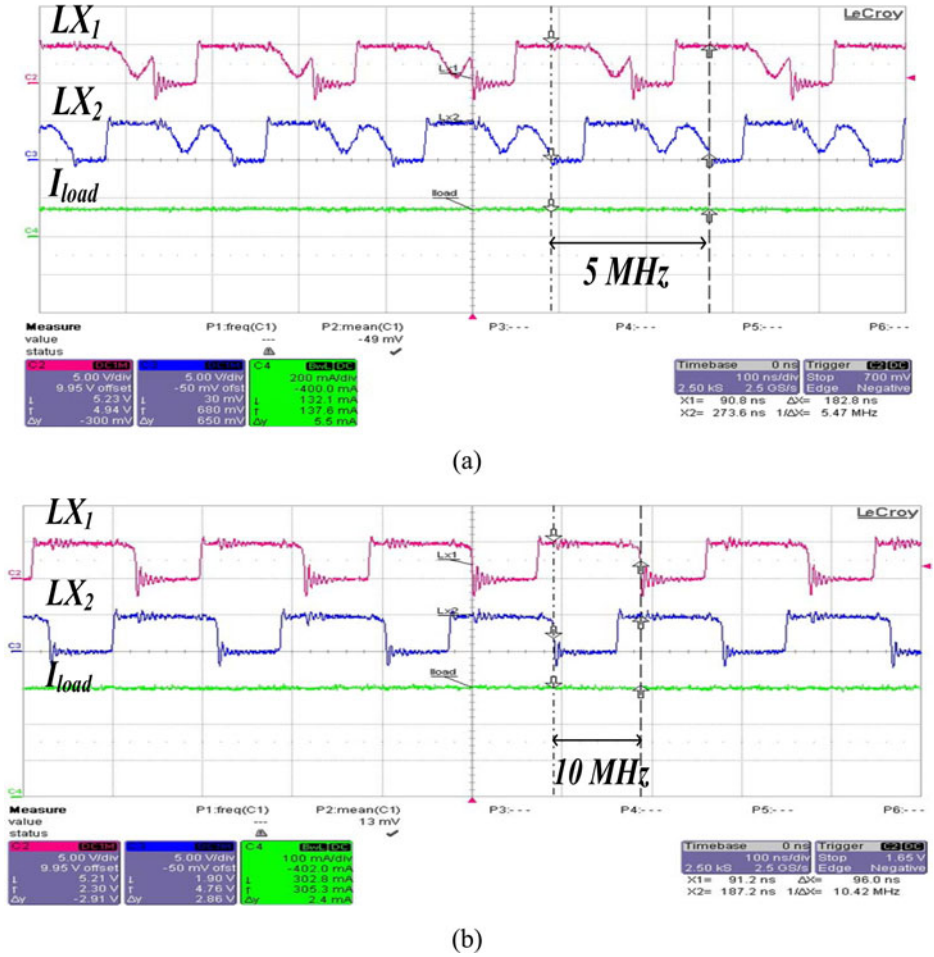

Fig. 19. Switching waveform of the TMCB boost converter with (a) a loading of 150 mA and (b) a loading of 300 mA.

from the summation of the master and slave channels

$$I_{\text{balance}} = \frac{\hat{i}_2}{\hat{i}_1} = \frac{A_a(s) F_m^{(2)} G_{\text{id}}^{(2)} H_e(s) + (G_{\text{idx}}^{(1)}/G_{\text{id}}^{(1)})}{A_a(s) F_m^{(2)} G_{\text{id}}^{(2)} H_e(s) + F_m^{(2)} G_{\text{id}}^{(2)} + 1} \tag{14}$$

$$H_e(s) = \frac{1}{1 + (2s/T_S) + (s^2/\pi^2 T_S^2)}. \tag{15}$$

Fig. 13 shows the simulation waveforms of the conventional converter and the proposed interleaved converter when the load current was increased from 300 to 600 mA. The output voltage of the proposed converter has better transient response than that of the single channel converter. The simulation results demonstrate the correction of the earlier analytic small-signal analysis.

The design of the TMCB is an important factor in the performance of the transient response. As mentioned earlier, a converter with a low bandwidth design in the TMCB leads to a slow transient response. Consequently, a converter with an ultrahigh bandwidth results in a subharmonic oscillation. Fig. 14 shows the simulation results of the transient response under the influence of the TMCB at the same load current condition of 300 mA and an inductor value of 0.47 μH. Fig. 14(a) shows a poor design example of TMCB wherein the current is unbalanced with a low gain $A_b^{(2)}$. On the other hand, Fig. 14(b) shows a converter with a suitable bandwidth design. However, Fig. 14(c) shows a converter with an ultrahigh bandwidth wherein a subharmonic oscillation occurs. The subharmonic oscillation is due to a too high bandwidth of current balance loop. The sampling effect should be considered together when the bandwidth approaches one-tenth of the switching frequency. Fig. 15 is the Bode plot of current balance loop in closed-loop form. It shows that the sampling effect appears when the bandwidth is extended to an enough high frequency as the g_m increases.

IV. Circuit Implementation

Fig. 16 shows the schematic diagram of the TMCB circuit. The current sensor estimates the current of each channel to

$$T_{CL\_S} = \frac{1}{(1/F_m^{(2)} G_{\text{vd}}^{(2)}) + R_a^{(2)} (G_{\text{idx}}^{(1)}/G_{\text{vd}}^{(1)}) + R_a^{(2)} (G_{\text{idx}}^{(2)}/G_{\text{vd}}^{(2)}) - \left((G_{\text{id}}^{(1)}/G_{\text{vd}}^{(1)}) + (G_{\text{idx}}^{(2)}/G_{\text{vd}}^{(2)}) - (G_{\text{idx}}^{(1)}/G_{\text{vd}}^{(1)}) + (G_{\text{id}}^{(2)}/G_{\text{vd}}^{(2)}) \right) R_b^{(2)} A_b(s) - F_v^{(2)}} \tag{13}$$

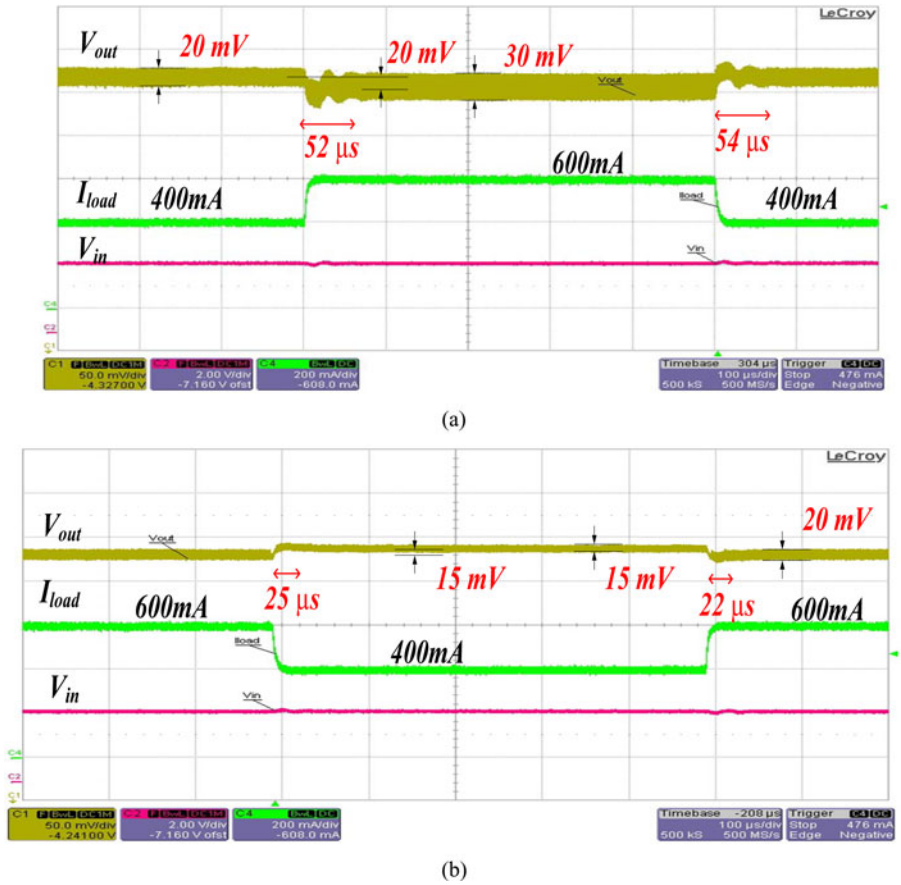

Fig. 20. (a) Measurement results of the load transient response in the conventional boost converter. (b) Measurement results of the load transient response in the proposed TMCB boost converter.

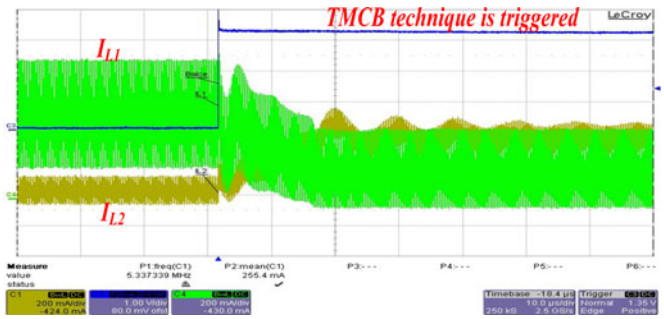

Fig. 21. Current balance turn-on waveform of the proposed converter.

obtain I_{s1} and I_{s2} for indicating the inductor current level in phase I and phase II, respectively. The switching operation causes the fluctuation on the values of I_{s1} and I_{s2}. Thus, the sample and hold circuit were adopted to obtain the average values of V_{SH1} and V_{SH2} to represent I_{s1} and I_{s2}, respectively. To obtain a better current balance operation, summation and divider circuits were used to generate the average channel current V_{AVG} through V_{SH1} and V_{SH2}.

The current adjustment circuit is composed of two operational transconductance amplifiers, *OTA1* and *OTA2*, to amplify the difference between V_{AVG} and V_{SH1} (or V_{SH2}) to produce the current balance signal I_{CB1} (or I_{CB2}). Each signal is injected into the ramp generator to modify V_{Sen2} of phase II for the current balance. As mentioned in the TMCB technique, the ramp voltage was adjusted using the time-multiplexing method. The outer voltage and inner current loops simultaneously exist in the closed loop. To ensure loop stability, the outer voltage loop must dominate the whole system in the multiphase operation wherein the voltage loop gain is higher than the current balance loop gain.

The embodied ramp generator circuit produces a voltage V_{Sen2} from the charging and discharging the capacitor C_R to determine the duty cycle. The charging and discharging currents are I_1 and I_2, respectively. Therefore, the current balance signals, I_{CB1} and I_{CB2}, can be injected into the C_R for the ramps in phase II. The higher value of I_{CB2} contributes to a higher ramp voltage leading to a reduced value duty cycle and a lower I_{CB2} results in a large duty cycle. The time-multiplexing control with modulated ramp amplitude can be easily achieved using a multiplexer. Unlike in the conventional interleaved architecture, all phases in the proposed converter share the same clock based on the time-multiplexing scheme. It can also eliminate the inevitable mismatch between multiple controllers using a single controller, and thus improving the accuracy of current sharing.

Ideally, the bandwidths of both loops must be as large as possible to accelerate the transient response. However, enlarging

TABLE IV
SPECIFICATIONS OF THE PROPOSED BOOST CONVERTER

Process	**0.3μm 5V/18V CMOS 2P3M**
Input voltage	**3.1V–3.3 V**
Output voltage	**4.5 V**
Inductor (L_a/L_b)	**0.47 μH /0.47 μH**
Output capacitors (C_1)	**20 μF**
Switching frequency	**5 MHz**
ESR of output capacitor	**10 mΩ**

TABLE V
COMPARISON BETWEEN THE PROPOSED AND THE CONVENTIONAL TOPOLOGIES

Topology	Proposed	Conventional boost converter
Inductor	**2**	**1**
Schottky diode	**2**	**1**
Output capacitance	**1**	**1**
Power switches	**2**	**1**
Error amplifier	**1**	**1**
Comparator	**1**	**1**
Chip area(normalized)	**120%**	**100%**
Output ripple	**20 mV**	**30 mV**
Transient response	**22μs /25μs**	**52μs /54μs**

the bandwidth of the current balance loop leads to a subharmonic oscillation because the bandwidth of the current balance loop (or sample and hold) is too closed to one-tenth of the switching frequency, and the inductor current ripple cannot be ignored. This phenomenon makes V_{Sen2} unstable with a constant value. On the other hand, a small bandwidth of the current balance loop leads to a longer transient time because V_{Sen2} cannot reach its stable value, and the loading is immediately supplied by the master channel. Although the master channel has supplied the loading and balanced, it is still affected by slave channel while the current balance loop is unbalanced.

Fig. 17 shows the schematic diagram of the internal oscillator and the frequency divider and the waveforms. The internal oscillator is composed of constant current source *P*47, comparator *X*3, and capacitance *C*7. The sawtooth is generated by charging/discharging *C*7 when the sawtooth voltage is less than the V_H or greater than the V_L, respectively. A D flip-flop, which is a simple frequency divider, was used to generate two interleaved clocks, the CLK_{Master} and the CLK_{Slave}. The waveforms of each signal are shown in Fig. 17.

V. EXPERIMENTAL RESULTS

The proposed TMCB current-mode boost converter was fabricated in a 0.3-μm 5-V/18-V CMOS 2P3M process. The input voltage was about 3.1–3.3 V and the output voltage was 4.5 V. The chip area was 1350 × 1380 μm^2. The internal clock generator was 10 MHz and each interleaved channel was operated at 5 MHz. The inductor value was 0.47 μH, and the output capacitance was 20 μF with an ESR of 10 mΩ. Fig. 18 shows the chip micrograph of the proposed TMCB boost converter. The power MOSFETs, MN_1 and MN_2, are located at the left-top corner for easy wire bonding.

Fig. 19 shows the measurement results of the proposed TMCB boost converter. The load currents were 150 and 300 mA as shown in Fig. 19(a) and (b), respectively. The accurately interleaved operation demonstrates that each channel can operate at a switching frequency of 5 MHz.

Fig. 20(a) shows the measurement results of the load transient response in a conventional boost converter if the load current is changed from 400 to 600 mA, or vice versa. The input and the output voltages were 3.3 and 4.5 V, respectively. The light-to-heavy and heavy-to-light settling times were 52 and 54 μs, respectively. On the other hand, as shown in Fig. 20(b), the light-to-heavy and heavy-to-light settling times improved to about 22 and 25 μs, respectively, due to the large bandwidth and dual-phase operation. The output voltage ripple was effectively reduced to about half of that of conventional design because the proposed TMCB technique ensured a good current balance between the two phases.

To show the effective current balance contributed by the TMCB technique, the two inductors, L_1 and L_2, were set to 0.47 and 1.2 μH, respectively. The mismatch between the two inductors was about 153%. The TMCB technique was switched ON to start the current balance between the two phases, as shown in Fig. 21. Finally, the two phases can drive the same current to the output even there was a large mismatch between the two inductors. Table IV shows the specifications of the proposed converter, and Table V shows the comparison between the proposed and the conventional boost converters. The proposed boost converter has a better transient response than the conventional converter due to a higher frequency RHP zero. Moreover, the compensator can be modified to have a larger bandwidth.

VI. CONCLUSION

In the current study, the proposed TMCB boost converter has been shown to be capable of providing a topology that reduces the output ripple and the effects of the RHP zero. A small and effective inductor value can move the RHP zero to

higher frequencies, thus allowing the bandwidth to be extended to a higher value. In addition, the proposed TMCB technique is demonstrated and the current mode ac model with the couple effect is presented. The test chip uses the 0.3-μm 5-V/18-V CMOS technology. Experimental results demonstrate that the proposed converter can improve the transient response from 22 to 52 μs.

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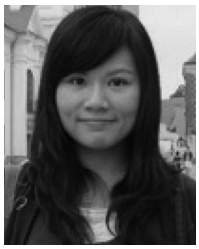

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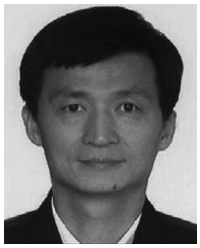

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