Microelectronic Engineering 95 (2012) 5–9

Contents lists available at SciVerse ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Surface potential mapping of p^+/n-well junction by secondary electron potential contrast with *in situ* nano-probe biasing

Jeng-Han Lee [a,*], Po-Tsun Liu [b]

[a] Department of Photonics and Institute of Electro-Optical Engineering, National Chiao Tung University, 1001 Ta-Hsueh Rd., HsinChu 30010, Taiwan, ROC
[b] Department of Photonics and Display Institute, National Chiao Tung University, 1001 Ta-Hsueh Rd., HsinChu 300, Taiwan, ROC

ARTICLE INFO

Article history:
Received 18 August 2011
Received in revised form 15 December 2011
Accepted 16 January 2012
Available online 1 February 2012

Keywords:
Secondary electron potential contrast (SEPC)
Scanning electron microscope (SEM)
Nano-probe

ABSTRACT

This article investigates the surface potential distribution of a biased p^+/n-well diode using secondary electron potential contrast (SEPC) with an *in situ* nano-probe trigger. The SEPC image is digitized and quantified for the conversion of the image contrast to the voltage scale, allowing for the identification of the depletion region and the electrical junction. The overlap length between the poly silicon gate and the p^+ region is also depicted by two-dimensional (2-D) imaging. This study demonstrates that the proposed *in situ* nano-probe system is highly effective for surface potential mapping.

1. Introduction

Semiconductor device performance is determined by the distribution and concentration of the dopant [1,2]. The 2-D junction profile technique has become vital to the development of nano-scale devices. Many studies have investigated the junction profile through various methods including secondary ion mass spectrometry (SIMS) [3], chemical delineation [4,5], scanning capacitance microscope (SCM) [6], Kelvin force probe microscope (KFPM) [7], and electron holography [8,9]. KFPM and electron holography depict the junction profile through surface potential mapping [7–9]. KFPM uses a tiny probe to scan across the junction and measure the long range electrostatic potential interaction between the probe and specimen surface. Off-axis electron holography reconstructs the electrostatic potential distribution across a diode based on electron interference.

Recent research has proposed the use of secondary electron potential contrast (SEPC) to inspect junction profiles with a sensitivity ranging from 10^{16} to 10^{20} cm^{-3} and a spatial resolution of 10 nm [10–14]. Since 1960, researchers have been investigating the mechanism of dopant contrast in scanning electron microscope (SEM). Various studies have investigated factors that influence dopant contrast. Perovic et al. and Turan et al. proposed that surface potential determines the secondary electron emission rate [15,16]. Sealy et al. proposed that the presence of a three-dimensional field outside the specimen is a major factor in dopant contrast [17]. Hsiao et al. studied strain effects in dopant contrast enhancement [18]. Elliott et al. and Venables et al. reported that the SEPC profile of a p^+/n-well junction shows a linear relationship with the logarithm of the SIMS depth profile [10,11]. Elliott's study on a biased junction found that the SEPC intensity is proportional to the built-in voltage [10].

Though the above-mentioned studies show that SEPC is a promising technique for junction profiling, few applications for SEPC in the junction profiling of actual circuits have been reported, probably because SEPC is difficult to observe in site-specific locations due to the reduced SEPC signals under standard SEM conditions. Sealy et al. suggested that surface band bending on a cleaved diode will reduce the dopant contrast [17]. Recent site-specific studies suggest that FIB sample preparation may indeed facilitate the inspection of dopant contrast [19]. During sample preparation, however, damage to the surface layer has been reported to reduce dopant contrast [19] and, in the worst case, SEPC cannot be observed by SEM imaging [20]. Hence, this study fills a gap in the literature by investigating solutions for enhancing dopant contrast by the *in situ* bias of the diode with nano-probe tips. The specific aims of this report are (a) to enhance dopant contrast with nano-probe assistance, (b) to link the image contrast to a voltage scale, and (c) to elucidate theoretical assumptions about the device physics. The proposed solution may also serve as a basis for further studies of SEPC mechanisms with static triggers. The simplicity of the method should enable its widespread adoption in dopant profile inspection.

2. Experimental

The experimental specimen was a functional static random access memory (SRAM) module manufactured with 90 nm IC tech-

* Corresponding author.
E-mail address: jameslee395@gmail.com (J.-H. Lee).

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doi:10.1016/j.mee.2012.01.008

nology, on a p-type (100) silicon wafer substrate with 8–12 Ω cm resistivity. After patterning the active area, implantation procedures formed the well and plus regions. Thermal activation at 1000 °C for 5 s and metallization were carried out sequentially as formal procedures. An SRAM chip with normal functionality was fabricated and manually polished with an Allied Multiprep™ to enable cross-sectional observation by SEM. In this work, the specimen is an SRAM chip with one poly layer and five metal layers. The diamond film was changed from coarse to fine to minimize scratching of the specimen surface. The specimen was prepared in cross-section for dopant profile inspection.

All SEM images in this paper were obtained with a Hitachi S4800 equipped with an $E \times B$ filter. The typical secondary electron (SE) energy is smaller than 50 eV. The $E \times B$ filter removes the high energy tail of the backscattered electron (BSE) and guides SE to the upper detector to enhance the SEPC effect on the silicon. The SEM operating conditions were optimized to visualize the diode. The image was acquired with a 1 keV primary electron energy at a working distance of 6 mm.

Despite the $E \times B$ detector's enhancement of the SEPC image, surface band bending and damage to the surface layer could reduce SEPC and limit its application in real circuits. To minimize the contrast reduction effect from these factors, a nano-probe system was installed in the SEM chamber. The junction condition was reverse-biased with a four-micromanipulator nano-probe system mounted to the Hitachi S4800 stage. The nano-probe tip had a 50 nm radius and could probe any node found in the SEM image. Fig. 1 depicts a partial cross section of the SRAM chip to schematically illustrate the SEPC inspection procedure, and three p^+/n-well junctions, two polycrystalline Si gates, and a nano-probe tip probe are shown in the middle of a p^+/n-well node. The middle p^+/n-well node serves as a positive node (V_{dd}) for SRAM and connects to the n-well through metal routing. The other two p^+/n-well nodes serve as the SRAM drain node. The middle p^+/n-well junction was electrically biased with a trigger voltage of 1 V. The p-substrate was kept in the ground state. The colors of the left and right p^+/n-well junctions and p-substrate illustrate the dopant contrast after bias voltage was applied.

3. Results and discussion

Fig. 2 shows an SEM image corresponding to the setup illustrated in Fig. 1. The nano-probe tip was applied to the middle p^+/n-well node with positive 1 V and the p-substrate with the ground. Because the middle p^+/n-well node, serving as an SRAM V_{dd} node, was connected with the n-well through a metal layer, thus the surface potential of the n-well will also be positive 1 V. The figure shows high contrast in the p-substrate and p^+ region, and low contrast in the n-well region. Fig. 3 presents a magnification of the SEPC image shown in Fig. 2. Two poly silicon gates and three p^+/n-well junctions are visible. The left and right p^+ regions show high contrast. The figure not only clearly shows the p^+ regions, but also the lightly-doped drain region (p^- region), thus confirming the good spatial resolution of the SPEC method. Contrast is low in the middle p^+ region since it acts as an SRAM V_{dd} node and is connected with the n-well region with positive 1 V. Additionally, the absence of doping contrast was restored when the bias voltage was triggered in the junction, indicating that SEPC is affected by the surface potential of the specimen.

The nano-probe system can assist the application of the p^+/n-well junction nodes in a reverse biased condition. Fig. 4 shows the intensity profile of the p^+/n-well diode with trigger voltages of 0 V on the p^+ node and 1 V on the n-well nodes. To further elucidate the device physics, a series of data analyses of p^+/n-well intensity profiles were performed. Each point in the intensity curve is the average of four of its adjacent points. The intensity curve was

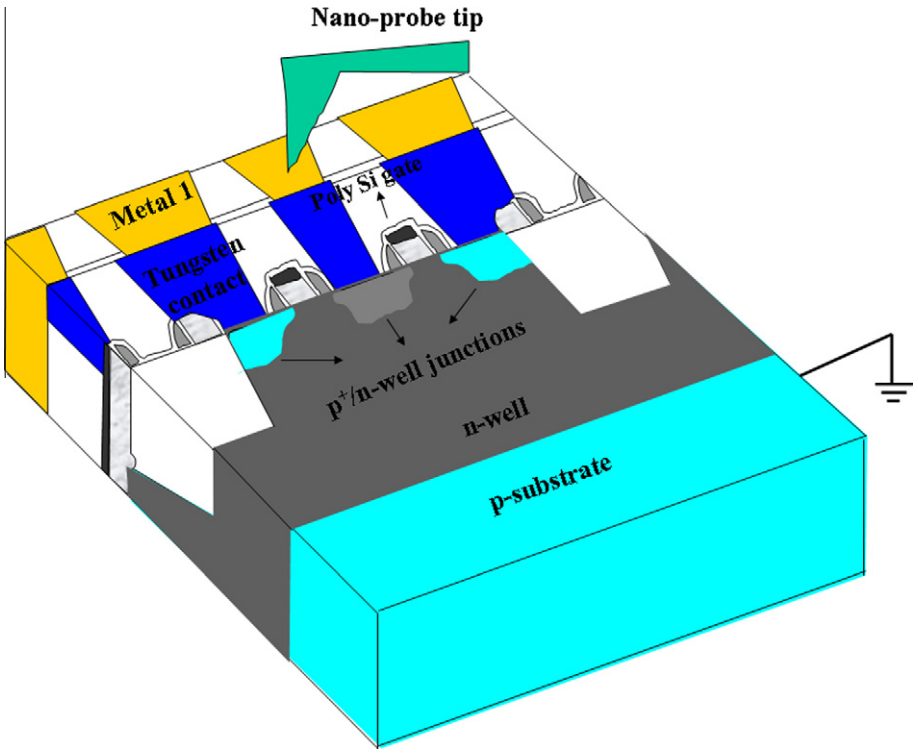

Fig. 1. A partial cross-section of the SRAM chip schematically illustrates the SEPC inspection; three p^+/n-well junctions, two polycrystalline Si gates, and a nano-probe tip are shown. The middle p^+/n-well junction was electrically biased with a trigger voltage 1 V. The p-substrate was kept on the ground state. The colors of the left and right p^+/n-well junctions and p-substrate illustrate the dopant contrast after electricity was biased. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

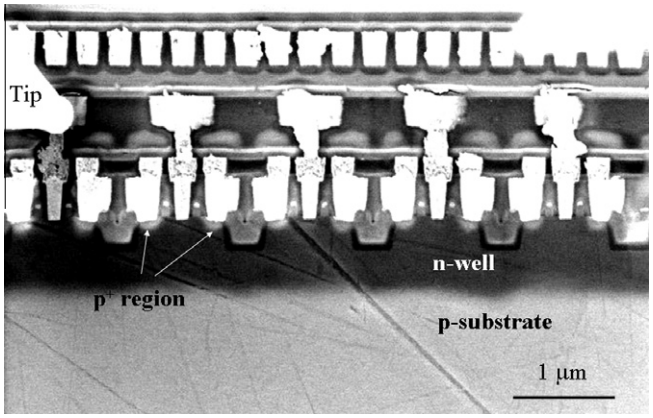

Fig. 2. The SEM image corresponds to Fig. 1, in which nano-probe tip applied to the middle p^+/n-well node with positive 1 V and the p-substrate with ground. Dopant contrast is clearly observed with the p-substrate and p^+ region providing the high contrast and the n-well providing the low contrast.

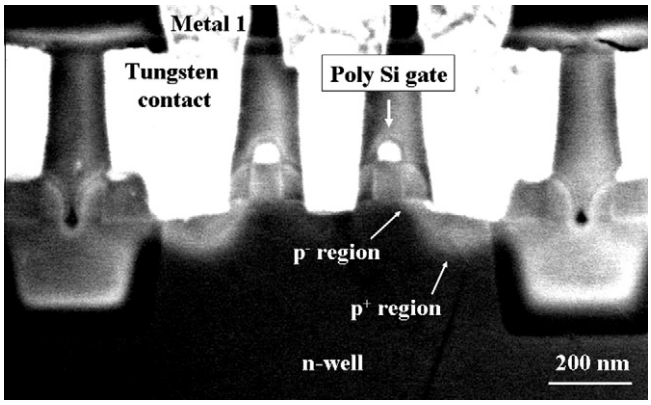

Fig. 3. A magnified SEM image of the image shown in Fig. 2, two poly silicon gates and three p^+/n-well junctions are visible. The left and right p^+ regions show high contrast. The figure clearly shows not only the p^+ regions, but also the lightly-doped drain regions (p^- region).

grouped into three regions: p^+ region, depletion region, and n-well region. In the p^+ region, the rapid drop in the intensity indicates the contact that makes with the tungsten plug. The two stable contrast regions represent the p^+ and n-well regions, and the gradually declining contrast represents depletion region, which is consistent with the device physics [20]. The pink curve in Fig. 4 represents the polynomial regression fit result when neglecting the contact region. Elliot et al. reported that the SEPC intensity in a biased silicon diode is proportional to its built-in voltage, which indicates that the image intensity reflects the surface potential of the specimen [10]. Thus the polynomial regression fit curve in Fig. 4 was converted proportionally into a voltage scale in which the p^+ region and n-well region are respectively set at 0 V and 1 V. Fig. 5 shows the surface potential profile of the p^+/n-well junction after conversion. The electrical field curve could be deduced by the first derivative of the surface potential curve. The electrical junction is located on the maximum point of the electrical field, and the measurement data show the depth of electrical junction is 123 nm. The proposed method successfully used SEPC to identify the depletion region and the electrical junction. Thus SEPC was used as a voltage mapping tool instead of matching SEPC signal with the carrier concentration, as in previous studies.

One-dimensional (1-D) intensity profile analysis was followed by 2-D image processing. Different colors were assigned depending on the intensity level of the p^+ region and the definition in the depletion and well regions: the p^+, depletion and well regions are respectively indicated in red, green, and blue. Fig. 6 shows that the upper and lower lines of the depletion region are two parallel curves as in an actual depletion region, and the profile of the p^+ region is as expected. The convex area on the left side of the p^+ region is the p^- region. Every pixel in Fig. 6 represents 3.8 nm. A 15 nm gap between the p^+ region and the poly silicon gate is also clearly visible in Fig. 6. The length of the gap is a crucial in determining the source/drain resistance of the transistor and has not been previous addressed in the literature.

Experimental results confirm that the *in situ* nano-probe system shows promise for inspecting p^+/n-well and n-well/p-well junctions. The next focus is to apply the method to inspecting n^+/p-well junction profiles. Fig. 7 presents an SEPC image of an n^+/p-well obtained in the current study. Since the two probe tips on two n^+ contacts had a positive 1 V, the substrate was kept at 0 V to ensure that

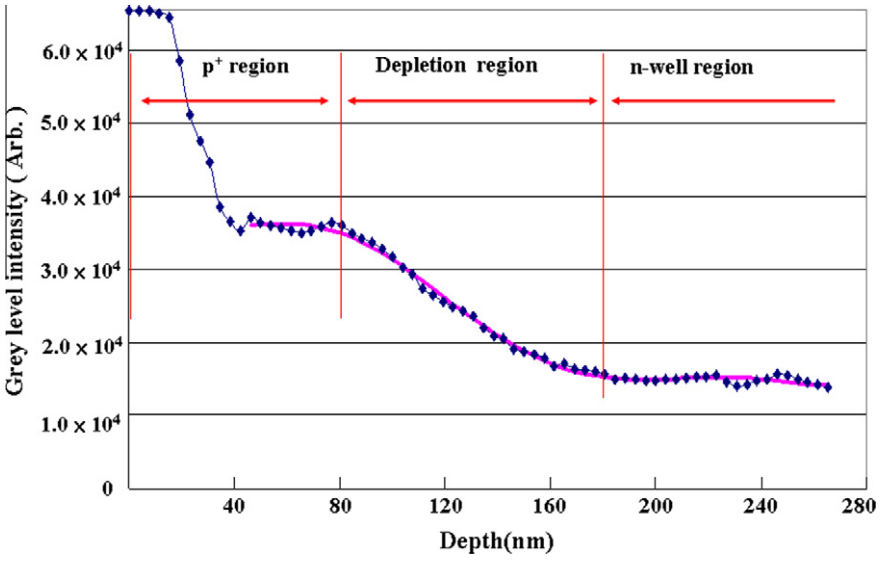

Fig. 4. The intensity profile of a biased p^+/n-well diode with a trigger voltage 0 V on the p^+ node and 1 V on the n-well node. Intensity curve was grouped into three regions, p^+ region, depletion region, and n-well region. The pink curve represents the polynomial regression fit result with $n = 6$. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

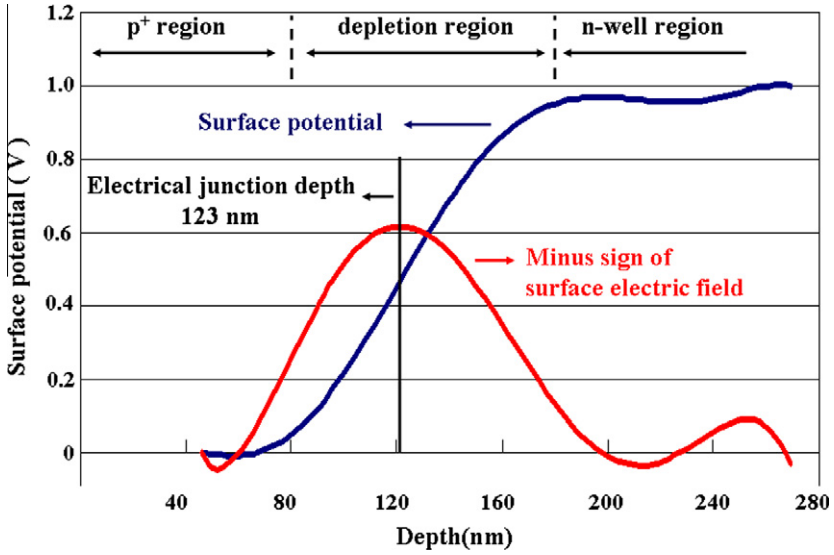

Fig. 5. The surface potential profile and electrical filed profile of a biased p^+/n-well diode. The polynomial regression fit curve in the Fig. 4 was converted proportionally into voltage scale. The p^+ region and n-well region are set in 0 V and 1 V, respectively. The electrical field curve is deduced by the first derivative of the surface potential curve. The depth of the electrical junction is located on the maximum point of the electrical field curve and its value is 123 nm.

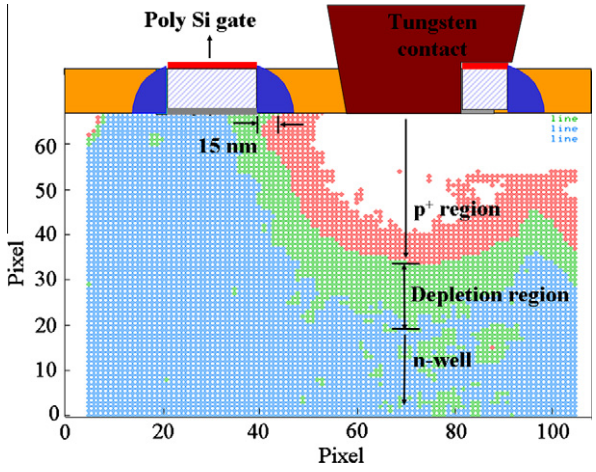

Fig. 6. The 2-D image processing result. The p^+ region, depletion region and well region were indicated in red, green, and blue, respectively. The gap length between the depletion region and the poly silicon gate is 15 nm. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

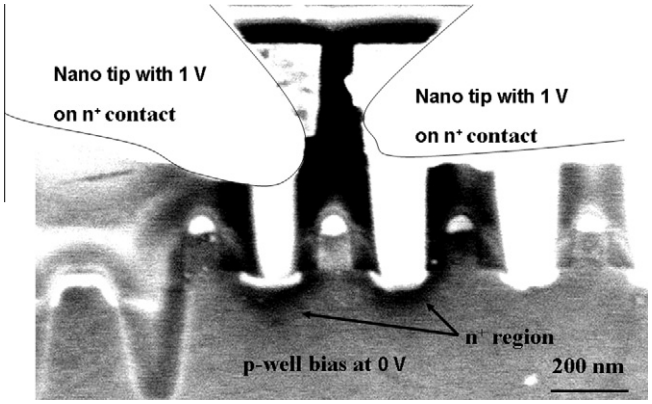

Fig. 7. A n^+/p-well junction SEM image in which nano-probe tips were electrically biased with 1 V on the n^+ node and 0 V on the p-well node. The SEM images show that contrast in the n^+ regions appeared when bias voltage was applied. The n^+ region without a nano-probe tip showed no SEPC signal. However the SEPC signal and image quality of the n^+/p-well junction were inferior to those in the p^+/n-well.

the n^+/p-well junction was biased under a reverse condition. The SEM images show that contrast appeared in the n^+/p-well junction when bias voltage was triggered. The n^+/p-well junction without a nano-probe tip showed no SEPC signal. However the contrast and image resolution of the n^+/p-well junction were inferior to those in the p^+/n-well. This result corresponds with Venables' experimental result regarding the abnormal depth of the n^+ region [11]. Venable et al. suspected that the internal, bulk electric field of the junction could be hindering the SEPC inspection [11]. Our study indicates that the dopant profiling of the n^+/p-well junction using *in situ* nano-probe biasing is not workable under current SEM conditions.

4. Conclusion

The nano-probe and SEPC effectively characterized the p^+/n-well junction and confirmed that *in situ* biasing is a promising method for junction profiling in actual SRAM chips. The method could be used to maintain the junction under stable voltage conditions to eliminate contrast reduction resulting from surface band bending and damage to the surface layer. The results indicate that contrast depends mainly on the specimen's surface potential.

Regarding qualitative junction profile inspection, the findings are also consistent with previous empirical studies. However, unlike previous studies that tried to link contrast with dopant concentration, this study is the first to link contrast with surface potential. A gradual decrease in contrast in the depletion region was observed in the reverse bias p^+/n-well junction. The depth of the electrical junction was identified after converting the image intensity to a voltage scale. In the two-dimensional dopant profile analysis, the proposed method also showed spatial resolution sufficient to identify the p^- region. Finally, a 15 nm gap between p^+ region and poly silicon gate was successfully identified. These are all novel findings which can be used to develop an efficient junction profiling procedure for use in the quantitative study of voltage distribution in a biased junction. The findings are also applicable to other solid state diodes such as solar cells and light emitting

diodes. Future studies may consider the use of SEPC as a routine monitoring method during the fabrication process.

Although the method effectively characterized the p^+/n-well junction, the image contrast and spatial resolution in the n^+/p-well junction are inferior to those in the p^+/n-well junction. Further studies of n^+/p-well junctions are needed to obtain a complete contrast mechanism for SEPC analysis.

Acknowledgements

The authors also would like to acknowledge David Su, Y.S. Huan, Y.T. Lin, C.C. Wu, and Edward Hsu for their kindly support and valuable discussion.

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