60-GHz Dual-Conversion Down-/Up-Converters Using Schottky Diode in 0.18 μm Foundry CMOS Technology

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***Abstract*—Due to the benefits of Schottky diodes, 0.18-μm CMOS technology is being promoted for millimeter wave applications. In this paper, 60-GHz dual-conversion down-/up-converters using Schottky diodes are realized by using 0.18-μm foundry CMOS technology. A $CoSi_2$–Si Schottky diode, fabricated on a lower doped N-well by blocking the threshold voltage adjustment implant, has a lower reverse leakage current and a better ideality factor. Thus, it is ideal for the 60-GHz sub-harmonic mixer design. Two new types of Schottky-diode mixers, a down-conversion sub-harmonic mixer with a dual-band lump-distributed phase-inverter rat-race coupler and an up-conversion sub-harmonic mixer with a trifilar transformer, are realized and employed at the high-frequency conversion stage of the dual-conversion architecture to achieve small size and broadband isolations. The silicon-based Schottky diode with a low turn-on voltage offers great advantage in LO pumping power, especially for an antiparallel diode pair structure. In our Schottky-diode sub-harmonic mixers, the required LO power is only 1 dBm. The dual-conversion down-converter achieves 5-dB conversion gain and 19 dB noise figure under $V_{dd} = 2.5$ V and $I_{dd} = 22$ mA, and the dual-conversion up-converter, with $V_{dd} = 2.5$ V and $I_{dd} = 26$ mA, attains greater than 40-dB sideband rejection and -1 dB conversion gain over the whole 60-GHz bandwidth.**

***Index Terms*—Converter, dual conversion, mixer, phase-inverter rat-race coupler, Schottky diode, single-sideband rejection, sub-harmonically pumped mixer, trifilar transformer, 0.18-μm foundry CMOS technology, 60-GHz.**

I. Introduction

A 60 GHz millimeter-wave system with unlicensed 7-GHz bandwidth conspicuously stands out in short-range high-data-rate applications, such as wireless personal area network (WPAN) and high-definition multimedia interface (HDMI). In 2004, the first CMOS 60-GHz amplifier was successfully demonstrated in standard 0.13-μm CMOS technology, beginning 60-GHz transmission using the CMOS-based IC [1]. Subsequently, different architectures for receivers, transmitters and transceivers [2]–[16] were proposed and came into fruition by using standard advanced CMOS and SiGe HBT processes. However, fully-CMOS-based designs still encounter great difficulties in term of noise and power performances. Fig. 1(a) shows the comparison of stand-alone 60-GHz LNAs using 130-nm, 90-nm, 65-nm CMOS and III-V compound technologies. The noise figure of 60-GHz CMOS-based LNAs are above 5 dB while the III-V compound LNAs has the noise figure smaller than 3-dB due to the superior device noise property. The best III-V compound LNA [27] is based on 0.1-μm InP heterojunction FETs and provides 2-dB NF and 23-dB gain with drain current of 8 mA at $V_{dd} = 0.8$ V, thanks to the minimum device NF of 0.6 dB at 60-GHz. Thus, the III-V compound technologies are very attractive for the 60-GHz LNA design. For entire 60 GHz receivers, the noise figure (NF) of a 130-nm CMOS receiver [3] is up to 12.5 dB while 90-nm CMOS receivers [5]–[13] achieve a better NF of 5.5 $\sim$ 8 dB. Recently, 65-nm [14], [15] or 45-nm [16] CMOS technology has also been devoted in the 60-GHz transmission. To date, the noise figures of the 65-nm and 45-nm CMOS receivers are 5.5 $\sim$ 7 dB and 6 $\sim$ 8 dB, respectively. The receiver noise figure improves slightly as the device scales down. Moreover, a 60-GHz power amplifier (PA) is also a key component because the output power of PAs has a great impact on the maximum transmission distance especially due to the high path loss at 60 GHz. The power amplifier does not prefer the CMOS scaling rule and PAE becomes even lower for the more advanced technology node due to lower breakdown voltage. A survey of the state-of-the-art 60-GHz PAs using advanced CMOS and III-V compound technologies is shown in Fig. 1(b). Compared with III-V compound technologies, standard CMOS PAs have lower PAE [54]–[58], and PAE and $OP_{1\ dB}$ obviously decrease as the CMOS device is scaled down.

The scaling rule has caused both chip size shrinkage and steady reductions in IC manufacturing costs. Research and development (R&D) costs were never a concern and could easily be accounted for in the manufacturing stage in the past. However, R&D costs recently have become an issue as the transistor size of the CMOS process approaches the photolithography limit. In millimeter-wave IC design, much iteration is unavoidable due to inaccurate device modeling and high process variation, greatly aggravating R&D costs. Nowadays, 60-GHz radio is implemented in the phased-array transceiver format to avoid the signal blocking during transmission. An inefficient CMOS power amplifier becomes a severe problem in the 60 GHz beam-forming system because PAs and LNAs consume the most of chip area and the power

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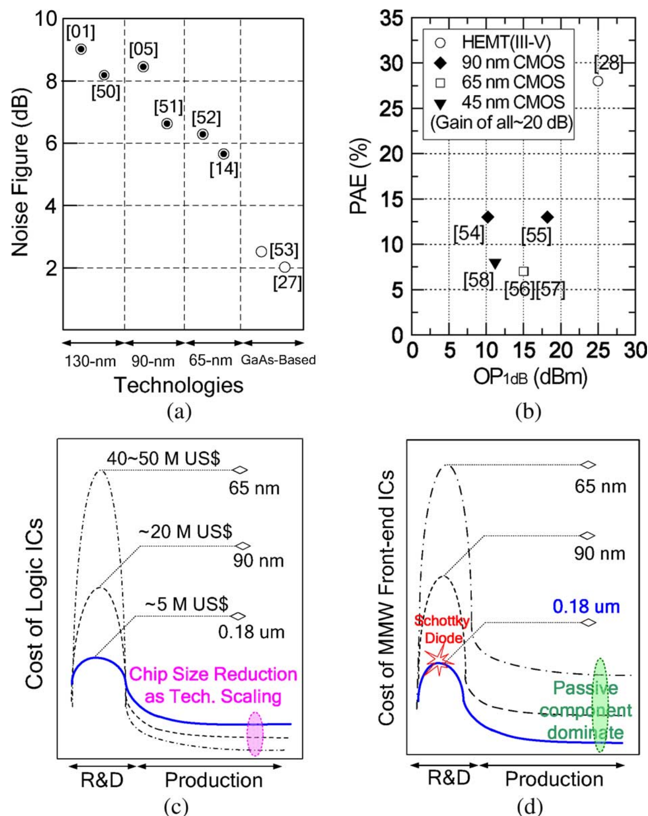

Fig. 1. (a), (b) the superior capabilities of III-V compound technology in the 60-GHz noise and power performances, and the cost issue in (c) logic ICs and (d) millimeter-wave front-end ICs as a function of R&D and manufacturing phases for different CMOS generations.

consumption. Passive components, used in millimeter-wave transceiver, occupy a large percentage of the chip and cannot be scaled down by using advanced CMOS technology [6]. Thus, the phased-arrayed transceiver size does not shrink sufficiently as the scaling rule proceeds due to the inefficient CMOS PAs. As shown in [29], the size of LNAs and PAs of 60-GHz RX and TX is more than 80% of total die area $(8.64 \times 8.93\ \mathrm{mm}^2)$. It is noticeable that the quarter-wavelength-based matching networks of PAs and LNAs occupy the most of chip area. The cost of the fully integrated CMOS phased-array transceiver is not low. Figs. 1(c) and 1(d) illustrate the costs of the logic ICs and millimeter-wave front-end ICs as a function of the R&D and manufacturing phases, respectively. The high R&D expense forms a barrier to product development. In Fig. 1(c), the high R&D costs of an advanced CMOS technology may still be covered for the logic IC product because of lower manufacturing cost by the device scaling rule. However, that is not the case for the millimeter-wave IC product because the scaling rule does not considerably decrease the manufacturing cost, as shown in Fig. 1(d).

While most of other researches follow the CMOS scaling rule and employ advanced CMOS technologies for the 60-GHz application, an alternative solution for the 60 GHz transceiver by simultaneously incorporating the advantages of III-V compound semiconductors and low-cost standard CMOS process is proposed and illustrated in Fig. 2. The use of external LNA/PA in III-V compound technologies is desirable because the resulting 60-GHz phased-array transceiver based on our proposed approach is expected to have much less LNAs and PAs for the same EIRP (Effective Isotropic Radiation Power) and sensitivity achieved by advanced CMOS technologies. The reduction of power consumption makes the 60 GHz transceiver based on our approach possible for portable applications. In this paper, the first 60 GHz Schottky-diode-based front-end including up- and down-converters are demonstrated in a 0.18-μm foundry CMOS process.

The Schottky diode, a majority-carrier device, has no minority storage effect and thus possesses very high-speed response for mixing and rectification. Among the GaAs-based technologies, Schottky-diode mixers have matured [17]. However, little attention has been paid to the silicon processes because of the absence of Schottky diodes in a standard CMOS process. A 12-GHz down-converter using silicon Schottky diodes was demonstrated using bipolar technology with an extra processing step for Schottky diodes [18]. In 1996, the first experimental work to form Schottky diodes without an extra processing step in a foundry CMOS process was demonstrated by arranging the layout layers appropriately [19]. The initial rectifying effect of the Schottky diodes was limited to 600 MHz, possibly due to the long wire bonding used in the measurement setup. Until 2005, Schottky diodes with a cut-off frequency beyond several hundred GHz were developed in standard CMOS [20]. The Schottky diodes based on the standard silicon process offer superior frequency conversion, and thus key components such as signal detectors [22], [26], frequency doublers [25], and mixers [24] have been implemented in the millimeter-wave regime. These results [22], [25], [26] shed light on the suitability of Schottky diodes in millimeter-wave applications using foundry CMOS process. The Schottky diode, like a catalyst, significantly reduces the R&D cost barriers shown in Fig. 1(d) and makes a 60-GHz transceiver with 0.18-μm CMOS technology possible. However, no millimeter-wave transceiver based on the Schottky diodes has been reported to date.

A direct conversion requires accurate quadrature LO signal generation directly at the same frequency of RF signals. Fully integrated transceivers, based on the direct conversion architecture, have been successfully demonstrated below 5 GHz because IQ signal generation is less sensitive to the parasitic effects of the practical layout. When the channel bandwidth approaches several GHz at the millimeter-wave frequency, it becomes difficult to generate a precise, wideband IQ signal at 60 GHz. Thus, as discussed later in this paper, a dual-conversion architecture is employed to accomplish the band selection and quadrature generation in two separate steps. As shown in Fig. 2, the block diagrams for the 60-GHz dual-conversion up-/down-converters are depicted inside the dashed-square area. A precise IQ signal is generated by a fixed quadrature LO_2 at low-frequency conversion while channel selection is achieved by sweeping LO_1 at high-frequency conversion. The dual conversion consists of a high-frequency conversion using the microwave/millimeter-wave design approach and a low-frequency conversion using the analog design approach. For the higher-frequency conversion, a dual-band lump-distributed phase-inverter rat-race coupler and a compact trifilar transformer together with antiparallel diode pairs (APDPs) are proposed for

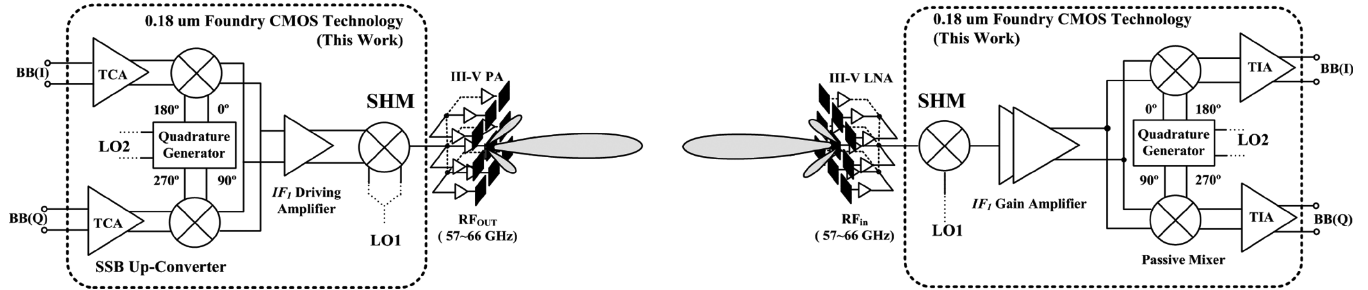

Fig. 2. Block diagram of the demonstrated dual-conversion up-/down-converters using Schottky diodes in 0.18-μm standard CMOS technology for a 60 GHz transmission system.

Schottky-diode sub-harmonic down-conversion and up-conversion mixers (SHMs), respectively. The SHMs reduce the LO frequency to one-half of a fundamental mixer, and thus alleviate the difficulty of millimeter-wave LO generation with 0.18-μm CMOS technology. The proposed SHM topologies provide inherent cancellations among all ports of SHMs to achieve broadband isolations. For lower-frequency conversion, analog mixers such as resistive and Gilbert mixers are employed due to size concern. There is a trade-off in designing IF_1 frequency. In consideration of the problem of image/sideband signal at the high-frequency conversion, IF_1 designed at higher frequency to facilitate the image/sideband signal suppression is preferred. However, the gain requirement for IF_1 amplifiers sets an upper limit. In this paper, IF_1 frequency is set at 10 GHz for 0.18-μm CMOS technology. The image/sideband signal is 20 GHz away from the desired RF band of 57 $\sim$ 66 GHz and can be easily filtered out by not only the bandpass response of the 60-GHz LNA/PA but also the preceding RF bandpass filter.

This paper is organized as follows. In Section II, a Schottky diode with small leakage current and good ideality factor is presented. The properties of Schottky diodes, extracted from the S-parameter measurement, are characterized and discussed for the 60-GHz SHM design. Circuit implementations and measurement results of the demonstrated 0.18-μm CMOS 60-GHz dual-conversion down-/up-converters are presented in Sections III and IV, respectively. Section V contains the conclusions of this paper.

II. Schottky Diode With Lower Doping Density Implemented in a Foundry CMOS Process

In the silicon-based technology, a thermal stable cobalt-silicide $(\mathrm{CoSi_2})$ Schottky contact is formed by directly depositing metals on n- or p-wells with subsequent thermal silicidation. This is a well-known method for implementing Schottky contacts [19]–[21]. However, the default doping density of the n-well, defined by layer mask, is equivalent to that of the nominal pMOS device $(V_T \sim -0.5\ \mathrm{V})$ in a TSMC 0.18-μm standard CMOS process. Here, V_T represents the threshold voltage. The doping density needs to be adjusted for different generations of CMOS technology. In an advanced process, higher doping density is required, but this also affects the reverse leakage current and ideality factor of the Schottky contact. In the standard TSMC 0.18-μm CMOS process, there are two types of n-wells with different doping densities for high $V_T(\sim -0.5\ \mathrm{V})$ and low $V_T(\sim -0.2\ \mathrm{V})$ devices. Here, an optional mask for low V_T, which blocks pMOS threshold

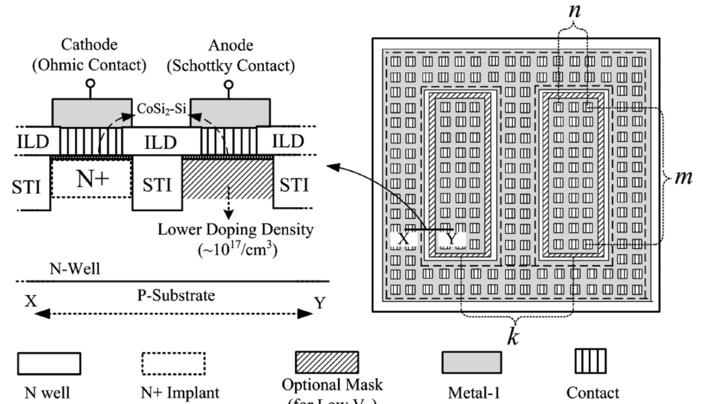

Fig. 3. Cross section and layout of the Schottky diode with low-doping density implemented in 0.18-μm foundry CMOS technology.

voltage adjustment implant in the well region, is used here to reduce the doping density of the n-well underneath the contact metal.

The contact number of Schottky diode is determined by the product of rows (m), columns (n), and fingers (k), as illustrated in Fig. 3. Each contact size is $0.22 \times 0.22\ \mu\mathrm{m}^2$ and the spacing between contacts is 0.28 μm complying with the minimum spacing in the design rule. The measured ideality factor of the Schottky diode with $\mathrm{m \times n \times k = 10 \times 10 \times 1}$ is around 1.12, and its leakage current of 0.86 A/cm^2 at $\mathrm{Vbias} = -1\ \mathrm{V}$ is two-order magnitude smaller than that without the optional mask, as shown in Fig. 4(a). The reverse avalanche breakdown voltage, barrier height and built-in voltage are 11 V, 0.53 eV and 0.4 V, respectively. Based on the standard C–V measurement, the doping density is on the order of $2 \times 10^{17}\ \mathrm{cm}^{-3}$. Here, a Schottky diode with low built-in voltage offers great advantages for the LO power design, especially in an antiparallel diode pair (APDP) SHM. Since it is infeasible to bias the diodes in an APDP structure, the required pumping power depends almost entirely on the diode's built-in voltage. Compared with GaAs-based Schottky diodes with 0.7-V built-in voltage, APDP SHMs in CMOS technology at millimeter-wave frequency has a great advantage in term of LO driving power.

Fig. 4(b) shows the series resistances (R_S) and junction capacitances (C_j) of the Schottky diodes with different sizes. The numbers of Schottky contact number are (I) $m \times n \times k = 5 \times 3 \times 1$ and (II)-(IV) $m \times n \times k = 10 \times 3 \times k (k : 1 \sim 4)$, as illustrated in Fig. 3. The anode is surrounded by the cathode to reduce the access resistance. R_S and C_j are extracted from

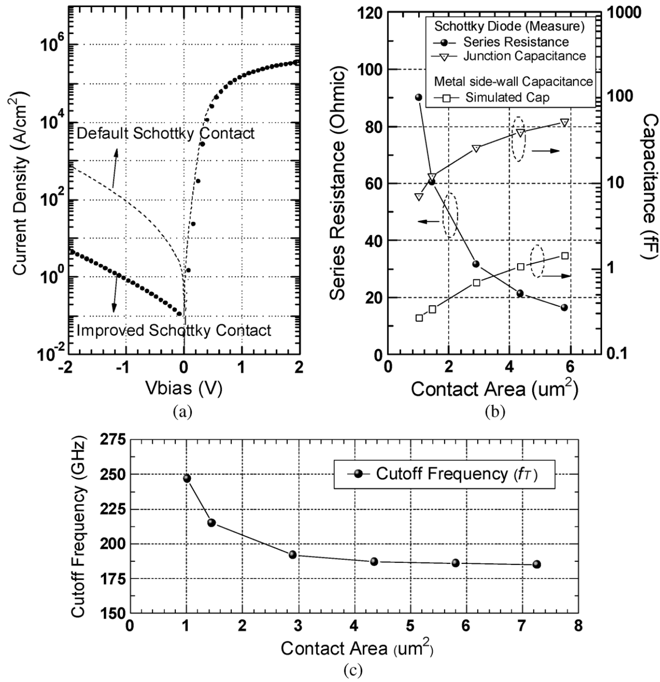

Fig. 4. (a) Comparison of the measured I-V, and (b) the series resistance/junction capacitance/metal side-wall capacitance and (c) cut-off frequency of the improved Schottky diode.

two-port S-parameter measurements at zero bias and the parasitic effect of GSG pads is calibrated out in the parameter extraction. Measured S-parameters at 25 GHz are used. As shown in Fig. 4(c), the Schottky diode with contact number of $5 \times 3 \times 1$ and the area of 0.726 μm^2 has the highest cutoff frequency, $f_T = 1/(2\pi R_S C_j)$, of 250 GHz because the access resistance is minimized when the overall diode shape is close to a square shape. As the diode size increases, the cutoff frequency decreases until it finally starts to be stabilized at 185 GHz for diodes with contact number of $10 \times 3 \times 2$. The cutoff frequency of a Schottky diode, determined by the resistance and capacitance, obviously increases for diodes with fewer rows, columns and fingers because the effect of access resistance is alleviated. It is expected that a diode with a single contact should achieve very high cutoff frequency. In the literature, diodes with a single contact of 0.45×0.45 μm^2 and 0.32×0.32 μm^2 can reach the cutoff frequencies of 400 GHz and 1.5 THz for 0.18 μm [21] and 0.13 μm [22] CMOS foundry processes, respectively. However, APDP configuration is used for our SHM design. The n-well capacitance behaves as a shunt capacitor to the ground in an APDP configuration and thus can destroy the APDP high frequency performance such as matching and linearity [23]. For example, severe high frequency performance degradation has been observed for the single contact diode of 0.32×0.32 μm^2 with the capacitance of 7.3 fF while the n-well to substrate capacitance is 41 fF [23]. The effect of the n-well capacitance on the high frequency is pronounced for diodes with small contact areas. Thus, a large contact area diode with a higher ratio of diode capacitance to n-well capacitance is employed to alleviate the notorious n-well capacitance effect in this paper. Diodes with the contact number of $10 \times 3 \times 2$ are employed in this paper despite of a lower cut-off frequency. Each Schottky diode used in the APDP of the SHMs only works below 30 GHz, and the speed of all test-keys is high enough for our circuit design. Moreover, the simulated metal side-wall capacitances of the structures (I)-(V), shown in Fig. 4(b), are 0.26, 0.34, 0.7, 1, 1.44 fF, respectively. Compared with C_j of each Schottky diode, the metal side-wall capacitance only contributes less than 4% and has a small impact on the cut-off frequency. For example, the cut-off frequency of the structure (I) increases from 250 GHz to 260 GHz after subtracting the side-wall effect. Thus, the degradation on conversion gain at 60 GHz by the side-wall capacitance is negligible and much smaller than 0.5 dB from simulation.

In general, a diode with large C_j is chosen for a narrow-band mixer to minimize the series resistance effect. The large C_j can be formed by connecting the small devices with better f_T in parallel if a higher conversion gain is needed despite of a larger device area. However, the effect of the n-well capacitor on APDP also sets a lower limit on the small device size in our work. A wideband mixer should use a diode with a small C_j to alleviate the capacitive loading effect caused by the diode. But, its high series resistance degrades conversion efficiency and requires a larger LO driving power because of the difficulty in impedance matching. The trade-off exists in the diode-size selection for mixer design.

III. The Demonstrated 60-GHz Dual-Conversion Down-Converter

The 60 GHz dual-conversion down-converter demonstrated in this research is composed of an SHM driven by the LO_1 signal (first LO), the first intermediate-frequency (IF_1) amplifier, a resistive mixer driven by the LO_2 signal (second LO), a wideband amplifier (IF_2), and a quadrature generator (LO_2) as shown in Fig. 5(a). The frequency planning of the dual-conversion is illustrated in Fig. 5(b). It is easy to fix the LO_2 frequency at the most accurate point of the IQ generator to obtain a precise baseband IQ output while the designated RF channel is selected by tuning the LO_1 frequency. Here, the $2f_{LO1}$ signal is tuned between 47 $\sim$ 54 GHz and the LO_2 signal is fixed at 10 GHz. In the high-frequency conversion, the silicon Schottky-diode SHM with low turn-on voltage facilitates the LO_1 buffer amplifier design. In this section, each stage of dual-conversion down-converter in Fig. 5(a) is presented and discussed in detail.

A. 60-GHz Sub-harmonically Pumped Mixer Using Dual-Band Lumped-Distributed Phase-Inverter Rat-Race Coupler

The first stage in the dual conversion is a 60-GHz SHM, which includes a dual-band phase-inverter rat-race coupler and two Schottky-diode mixer cells in APDP configuration, as shown in Fig. 6. The coupler merges an RF divider and an LO_1 balun into one passive component to reduce the area necessary for SHM. An in-phase/out-of-phase signal is generated from the RF/LO port while the two APDPs are series-connected between the remaining two ports as shown in Fig. 5(a). The in-phase/out-of-phase signal is always maintained for all frequencies because the physical paths from the RF/LO ports to the other two outputs are equal in geometry for the phase-inverter rat-race coupler. The balanced LO signals are achieved by a phase-inverter. The size of the phase-inverter in IC process

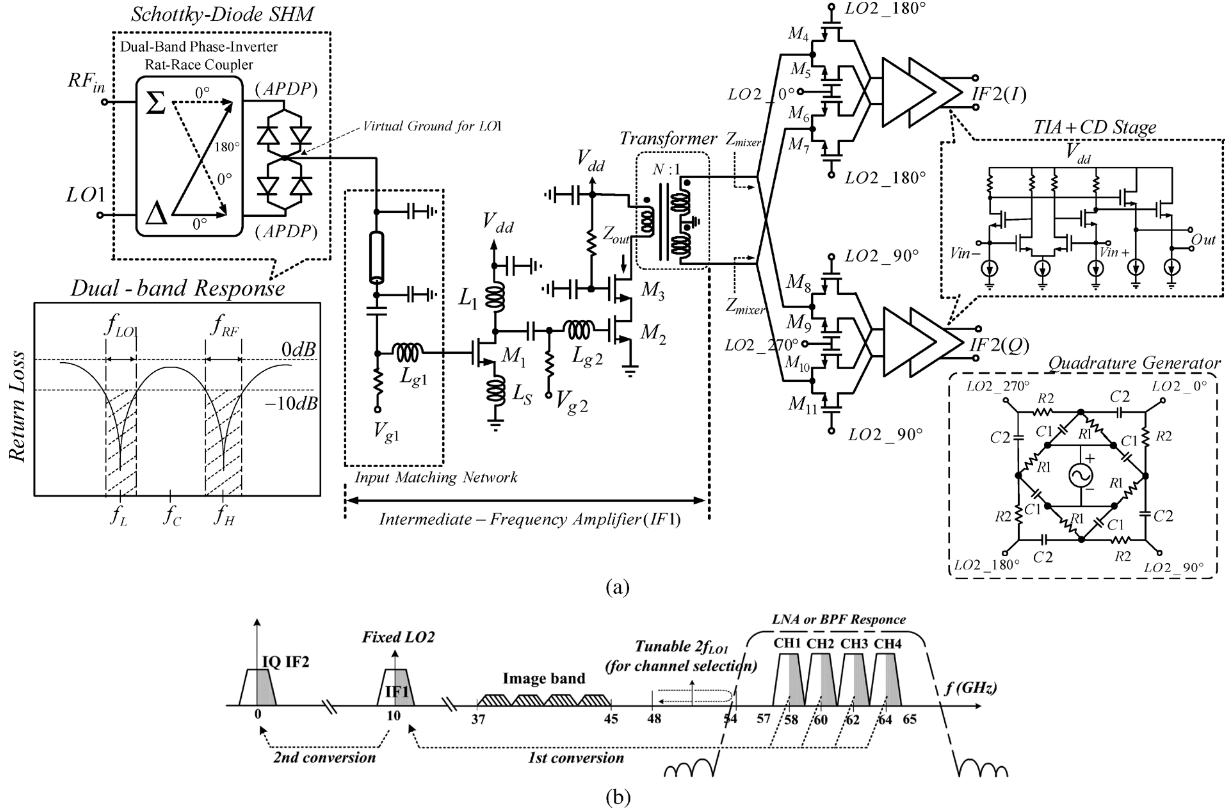

Fig. 5. (a) Schematic and (b) frequency planning of the 60-GHz dual-conversion down-converter by using Schottky diodes in 0.18-μm CMOS technology.

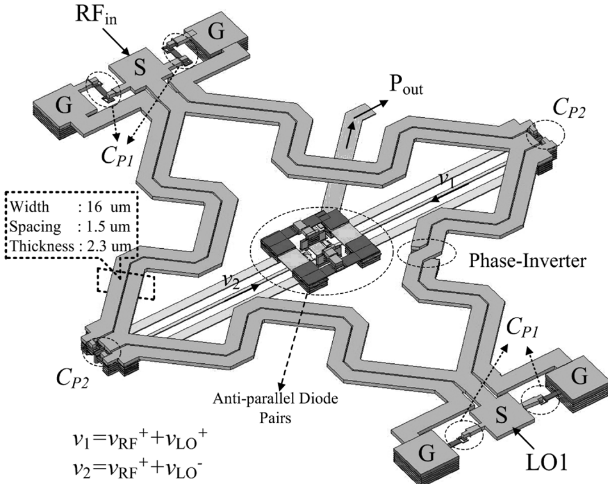

Fig. 6. 3D view of the 60 GHz sub-harmonically pumped mixer using a dual-band lumped-distributed phase-inverter rat-race coupler in 0.18-μm CMOS technology.

is a small proportion of the transmission line, and thus has a slight influence on the LO phase accuracy.

The output IF signal is taken from the virtual ground of the LO_1 signals, formed at the middle point of two series connected APDPs, to achieve a good broadband LO-to-IF isolation. There are good broadband isolations between the RF and LO ports due to the intrinsic isolation property of the wideband four-port coupler. The APDP structure inherently possesses an even-harmonic rejection, enabling it to achieve good broadband $2LO_1$-to-RF and $2LO_1$-to-IF isolations. Here, the rat-race coupler must handle RF and LO signals at two widely separate frequencies for the SHM. The RF signal ranges from 57 to 66 GHz, while the LO_1 signal covers 23.5–28 GHz. The bandwidth of a phase-inverter rat-race coupler is determined by the input matching instead of the magnitude/phase imbalance. Thus, we design the return-loss as a dual-band, and two matching dips can be arranged by adjusting the equivalent transmission-line impedance of each arm of the phase-inverter rat-race coupler [30], [31].

As expressed in (1), $\hat{z}$ is the normalized equivalent characteristic impedance of a coplanar stripline transmission line of the phase-inverter rat-race coupler and $\theta = \beta\ell$

$$\hat{z} = \sqrt{2(1-\cot^2\theta)} = \sqrt{2(1-\cot^2\beta\ell)} = \sqrt{2\left(1-\cot^2\left(\frac{\pi}{2}\frac{f_0}{f_c}\right)\right)}. \tag{1}$$

f_0 and f_C represent the frequencies of the matching dips and the center frequency of the lumped-distributed phase-inverter rat-race coupler, respectively. The spacing of the two split matching dips is extended when the equivalent characteristic impedance is continuously reduced, as shown in Fig. 7. It is the well-known Chebyshev-response design [31]. Although the wider bandwidth is realized by choosing lower characteristic impedance, there exists a trade-off between bandwidth and return-loss magnitude at $f/f_C = 1$. The limitation of a Chebyshev band-broadening technique is determined by the acceptable return loss at the center frequency of $f/f_C = 1$ [32] (e. g. 10 dB in general case). As the characteristic impedance decreases further, a dual-band bandwidth response forms. The dual-band response, as shown in Fig. 5, is desired since only

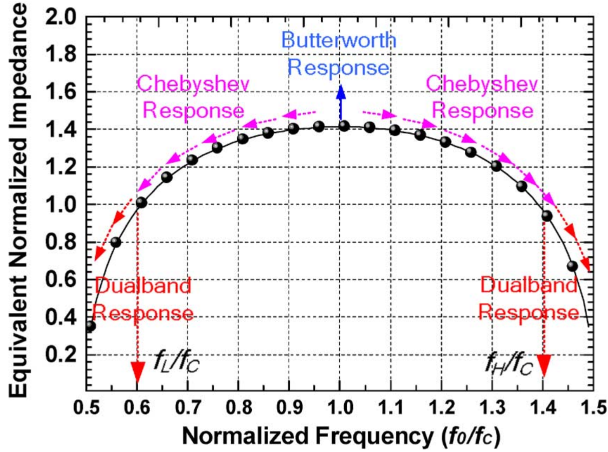

Fig. 7. Bandwidth and characteristic impedance design of a phase-inverter rat-race coupler.

return-loss bandwidth near LO_1 and RF frequencies needs to be covered for a sub-harmonic mixer design. The ratios of the two matching points to the center frequency of f_H/f_C and f_L/f_C are designed to be 1.4 and 0.6. $f_H = 61.5$ GHz and $f_L = 25.75$ GHz are the center frequencies for the RF and LO_1 bands, respectively. Here, a lump-distributed technique, shunting capacitors at each port, is incorporated with the Chebyshev band-broadening technique to simultaneously achieve wide bandwidth and size reduction [33]. The equivalent characteristic impedance of the lumped-distributed transmission line of each arm is around 45 Ω for the desired ratio of f_H/f_C and f_L/f_C, in which the characteristic impedance of the coplanar stripline transmission line is designed as 55 Ω by setting the spacing and width of metal-6 to 1.5 μm and 16 μm, respectively. Because the junction capacitance from the APDP, contributing to the size reduction, is not negligible, the shunting capacitance (C_{P1}) at both RF and LO ports is larger than that (C_{P2}) of the other two ports. C_{P1} and C_{P2} are 40 fF and 25 fF, respectively. The phase-inverter rat-race coupler shown in Fig. 6 is directly implemented on the silicon substrate. Compared with the transmission line formed by interconnect metals and interlayer dielectrics, a coplanar stripline directly on the silicon substrate has a shorter effective wavelength due to its higher silicon dielectric constant ($\varepsilon_r = 11.8$), while the inter-metal dielectric has a smaller dielectric constant of 3.8 ∼ 4. For a distortionless transmission line, energy is equally lost to the substrate and metal lines because of the equality condition between R/L and G/C, and size reduction by the dielectric constant still holds true as the case of a lossless transmission line. Distortionless transmission theory and concept for passive component miniaturization is developed in the appendix-B of our previous work [32]. High silicon dielectric constant has a great benefit in size shrinkage when implementing a microwave component directly on silicon substrate. The length of each arm in the lumped-distributed phase-inverter rat-race coupler at $f_{center} = 40$ GHz is only 510-μm. By winding the arms, the phase-inverter rat-race coupler can be further compacted to a square with sides of 400 μm in length, and the practical size of a stand-alone SHM is only 0.16 mm^2 as shown in Fig. 8. Finally, from the EM simulation, the LO amplitude and phase

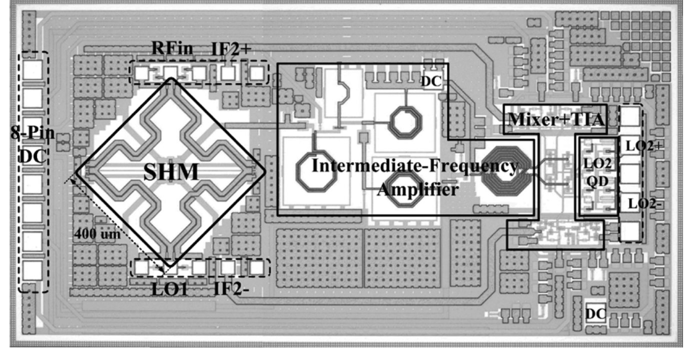

Fig. 8. Die photograph of the 60 GHz dual-conversion down-converter using 0.18-μm CMOS technology.

errors over the whole operating frequency keep within 0.5 dB and 1 degree. The pure loss of the phase-inverter rat-race coupler is 5 ∼ 6 dB.

B. Intermediate-Frequency Amplifier (IF_1), Second-Stage Mixer, Wideband Output Buffer and Quadrature Generator

After the first conversion, the noise figure caused by the second conversion must be low enough to achieve an acceptable noise figure for the 60 GHz dual-conversion down-converter. Our goal is to have the overall noise figure of dual conversion below 20 dB based on the gain and noise figure of GaAs-based LNAs at 60 GHz. The first stage Schottky-diode SHM has a conversion loss of 15 dB. It means that the noise figure of the subsequent stage, including the intermediate-frequency (IF_1) amplifier, the second stage resistive mixer and the wideband output buffer, must be lower than 5 dB at $f_{IF1} = 10$ GHz. A topology with low noise figure and high gain, as shown in Fig. 5(a), is chosen for the IF_1 amplifier. The IF_1 amplifier consists of a common source stage with the source degeneration inductor of L_S for simultaneous noise and gain match and a subsequent cascode stage for gain boosting. Here, the gain of the IF_1 amplifier is designed to be around 18 ∼ 20 dB to suppress the noise caused by the resistive mixer. The bandpass response of the input matching network of the IF_1 amplifier suppresses the f_{LO1} leakage signal. A 25-dB reduction in the LO_1 leakage signal is obtained in simulation. At the output load of the IF_1 amplifier, a single-to-differential transformer is employed for ac coupling, dc blocking, balanced-signal generation, and impedance transformation. The primary-coil inductance combined with the parasitic capacitance of the cascode device, M_3, forms an LC tank at f_{IF1}, and the secondary-coil inductance resonates out the parasitic capacitance at the source of the resistive mixer. The transformer is designed with a turn ratio of two $(\mathrm{N} = 2)$ to transfer the high output impedance (Z_{out}) of the cascode stage to the low input impedance (Z_{mixer}) of the double-balanced resistive mixer. The transformer has a coupling factor of 0.7 while the primary and secondary inductances are 1.62 nH and 0.62 nH, respectively. The peak of quality factor is designed as closely as possible to f_{IF1}. The maximum quality factor of the primary coil is 7.8 at f_{Qmax} of 8.5 GHz while the quality factor at 10 GHz is 7.5. The maximum quality factor of the secondary coil is 6.9 at f_{Qmax} of 10.3 GHz. To generate IQ baseband signals

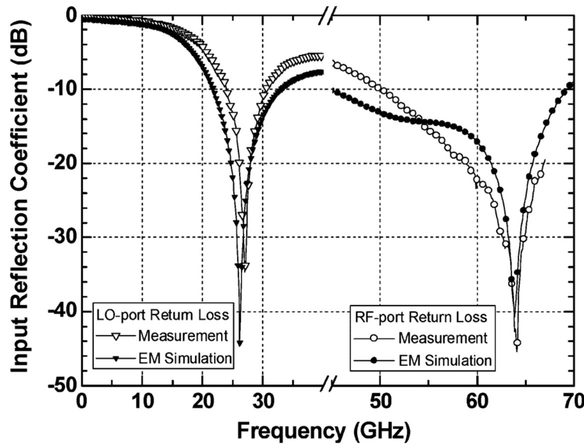

Fig. 9. Measured and simulated RF/LO reflection coefficient of the miniature dual-band rat-race coupler of the 60-GHz dual-conversion down converter using 0.18-μm CMOS technology.

at the low-frequency conversion stage, a poly-phase shifter is employed at the LO_2 ports of the 10-GHz double-balanced resistive mixers. As shown in Fig. 5, a two-stage poly-phase shifter is cascaded to reduce the process variation, and the pole frequencies of the first and two stages are chosen at 11.8 and 8.2 GHz. A 38% bandwidth is covered. The poly resistor of $\mathrm{R}_1(\mathrm{R}_2)$ and MIM cap of $\mathrm{C}_1(\mathrm{C}_2)$ have the values of 190 Ω (560 Ω) and 60 fF (30 fF), respectively. R_2 is designed to be larger than R_1 to minimize the voltage loss. The voltage gain is -1.5 dB, and IQ phase imbalance is smaller than 1 degree in simulation.

C. Experimental Results

Fig. 8 shows the die photograph of the demonstrated 60-GHz dual-conversion down-converter using 0.18-μm CMOS technology. The chip size is 1.9×1 mm^2 while the circuit area excluding the pads is 1.5×0.73 mm^2. An 8-pin DC pad is on the left side of the chip and the GSGSG pad for differential LO_2 signal is on the right side of the chip. Two differential pads on the top and bottom sides are used for RF/LO_1 and IF_{2+}/IF_{2-}, respectively. The total current consumption is 22 mA under 2.5-V supply voltage.

Fig. 9 shows the simulated and measured input reflection coefficient of the RF and LO_1 ports. The RF bandwidth, defined by the 10-dB reflection coefficient, is from 50 GHz to 70 GHz and fully covers our interest band of 57 $\sim$ 66 GHz. The other matching bandwidth at lower frequency is located at the desired LO_1 band of 23 $\sim$ 30 GHz. The measured conversion gain versus LO_1 power begins to flatten once the LO power exceeds 1 dBm as shown in Fig. 10. The required LO_1 pumping power is small for the SHM due to the good-matching design at f_{LO1} and the low turn-on voltage of the Schottky diodes. According to the literatures [34], [35], a 20 $\sim$ 30 GHz CMOS driving amplifier with 0-dBm output power is easily implemented using 0.18-μm CMOS technology because the maximum available gain at 25 GHz of common-source/cascode configuration is higher than 8 dB/15 dB. The measured $2LO$-to-RF and LO-to-RF isolations as shown in Fig. 11 are in the range of -60 dB and -30 dB, respectively. For comparison, a stand-

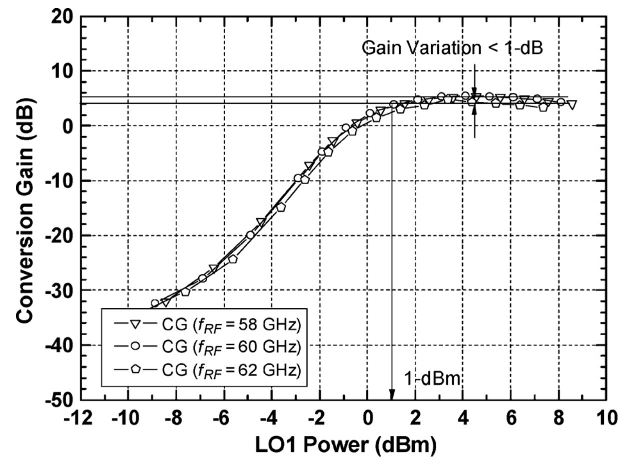

Fig. 10. Measured conversion gain of the 60-GHz dual-conversion down-converter versus LO_1 power for different RF frequencies.

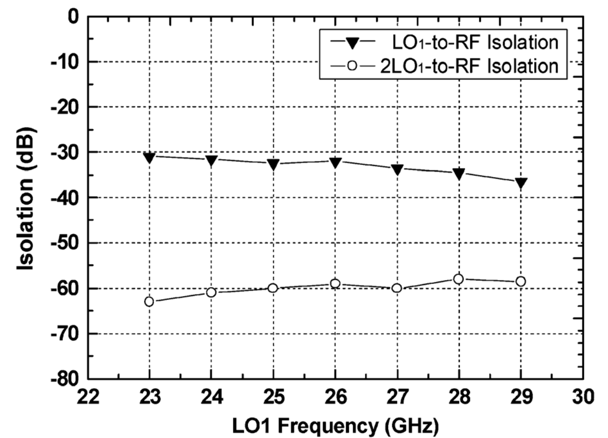

Fig. 11. Measured $2LO_1$-to-RF and LO_1-to-RF isolations of the 60-GHz dual-conversion down-converter using 0.18-μm CMOS technology.

alone SHM, which is identical to the high-frequency SHM of the dual-conversion converter, is fabricated. The measured conversion loss of the stand-alone SHM from 57 GHz to 66 GHz is around 15 dB.

The results of the stand-alone SHM together with other state-of-the-art millimeter-wave mixers are summarized in Table I. It is found that the demonstrated silicon-based antiparallel Schottky-diode SHM with no extra DC biasing circuit has a low LO power, good isolation performance and small size.

The measured conversion gain and power performance of the 60-GHz dual-conversion down-converter are depicted in Fig. 12. At $f_{IF2} = 1$ GHz, the conversion gain remains around 5 dB from 57 GHz to 66 GHz. The corresponding $\mathrm{IP}_{1\ \mathrm{dB}}$ and IIP3 are $-6 \sim -4$ dBm and 3 $\sim$ 5 dBm, respectively. The measured 3-dB IF_2 bandwidth, shown in Fig. 13, is up to 2.1 GHz and the gain variation is less than 1 dB for IF_2 frequency of up to 1.8 GHz. The measured noise figure at $f_{RF} = 60$ GHz keeps around 19 dB for IF_2 frequencies from 100 MHz to 2.2 GHz. For a 60-GHz gigabit transmission, the IF_2 bandwidth must be higher than 1 GHz for a 2-GHz RF channel. Here, the demonstrated dual-conversion down-converter has enough RF and IF bandwidths. Finally, the measured output IQ waveform under $f_{IF2} = 1$ GHz is shown in Fig. 14. The phase and amplitude errors are 0.3° and 0.8%, respectively.

TABLE I
COMPARISON OF MICROWAVE/MILLIMETER-WAVE MIXERS

	Tech.	f_{RF} (GHz)	CL (dB)	P_{LO} (dBm)	2LO-to-RF Isolation (dB)	Size (mm^2)
[36]	HEMT-Based resistive mixer	60	9	~8	N.A.	2x2
[37]	0.18 µm CMOS gate-drain connected diode mixer	25~56	<15	N.A.	N.A.	0.48x0.72
[38]	0.13 µm CMOS resistive mixer	45~73	15	5	N.A.	0.7x0.7
[39]	0.13 µm CMOS resistive mixer	28~50	9.6~11	7	33	0.75x0.81
[40]	0.18 µm CMOS gate-drain connected diode mixer	10~40	15~17	8*a	51~59	1.1x0.67
[23]	0.13 µm SiGe BiCMOS Schottky diode mixer	100~120	6~7	16	N.A.	0.78x0.43
This work	0.18 µm CMOS Schottky diode mixer	50~70	~15	1*b	60~65	0.4x0.4

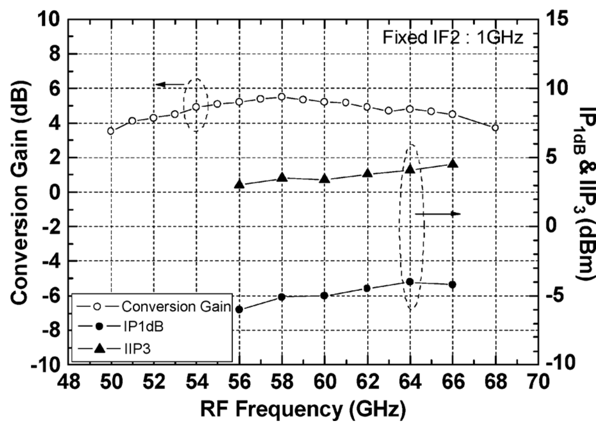

Fig. 12. Measured conversion gain and power performance of the 60-GHz dual-conversion down-converter using 0.18-μm CMOS technology.

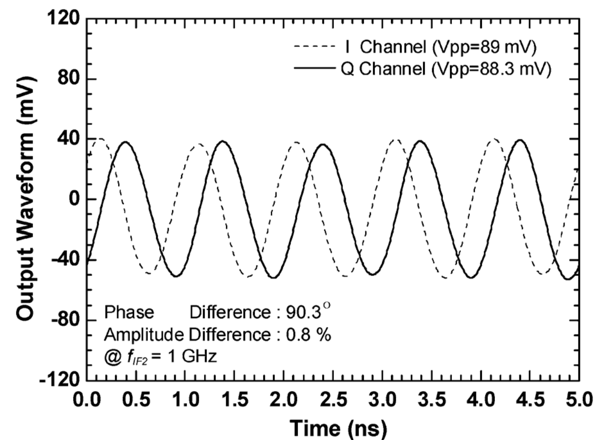

Fig. 14. Measured I/Q output waveform of the 60-GHz dual-conversion down-converter using 0.18-μm CMOS technology.

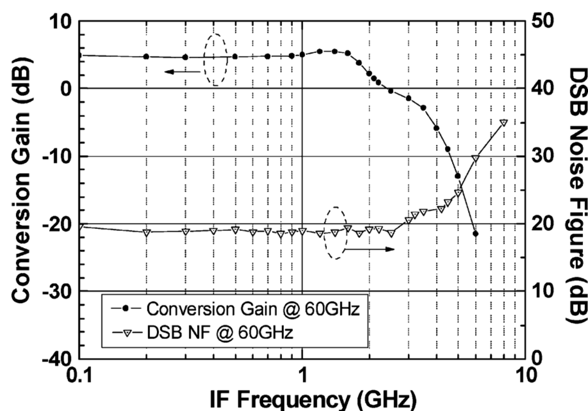

Fig. 13. Measured conversion gain and noise figure of the 60-GHz dual-conversion down-converter using 0.18-μm CMOS technology.

IV. THE DEMONSTRATED 60-GHz DUAL-CONVERSION UP-CONVERTER

The 60 GHz dual-conversion up-converter and its frequency planning are shown in Figs. 15(a) and 15(b), respectively. The frequency planning is similar to that of Fig. 5(b) for the compatibility with the frequency arrangement of LO generator in the 60 GHz dual-conversion down-converter. The IF_1 signal is at 10 GHz when the LO_2 frequency is also fixed at 10 GHz; thus, the sideband signal caused by the high-frequency conversion is 20 GHz away from the 60 GHz channel and easily filtered out by the subsequent bandpass circuits. However, $2LO_1$ leakage signal, located at 48 $\sim$ 54 GHz, is very close to the 60-GHz signal. It is difficult to suppress the $2LO_1$ leakage signal by the subsequent bandpass circuits, meaning that $2LO_1$ leakage signals could be emitted together with the desired 60-GHz signal. A good $2LO$-to-RF isolation is very important in the transmitter design. Thus, an SHM using trifilar transformer is proposed to

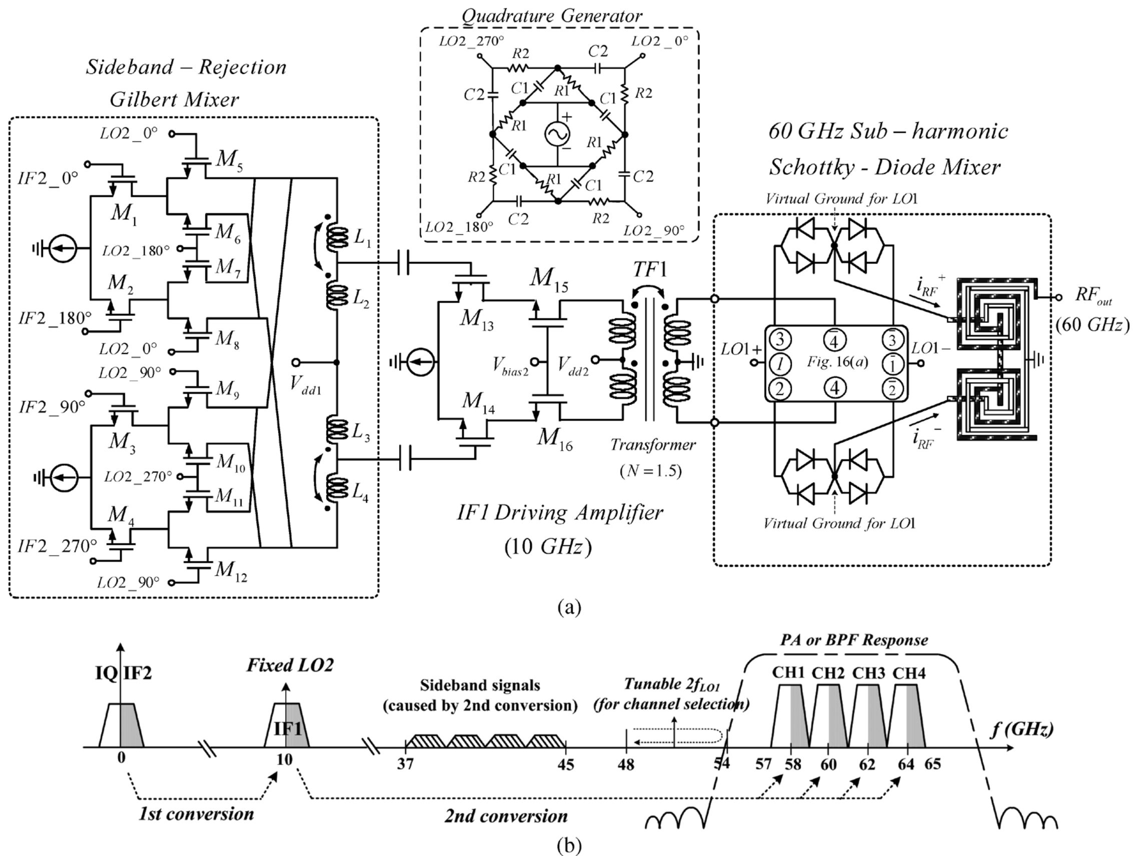

Fig. 15. (a) Schematic and (b) frequency planning of the 60-GHz dual-conversion up-converter by using Schottky diodes in the 0.18-μm CMOS technology.

solve the problem of port-to-port isolations. In addition, the 60 GHz up-converter consists of a single sideband (SSB) up-conversion mixer pumped by LO_2 signal at low-frequency conversion and an IF_1 differential driving amplifier inserted between the two-step up-conversion stages. Details of the schematics are presented below.

A. 60 GHz Sub-Harmonic Schottky-Diode Mixer Using Trifilar Transformer

The 60 GHz SHM includes a trifilar transformer for differential IF_1 and LO_1 inputs, series-connected Schottky-diode APDPs in double-balanced configuration for sub-harmonic mixing, and a Marchand Balun for 60-GHz differential RF signal extraction. A trifilar transformer with one primary coil and two secondary coils is a useful microwave passive circuit [41] and has been employed in image-reject down-converters [42] and quadrature voltage-controlled oscillators. Here, we use a trifilar transformer with 2:1:1 turn ratios to implement an SHM in millimeter-wave frequency. The schematic and physical layout are illustrated in Fig. 16(a). The IF_1 signal is fed via the center-taps of two secondary coils while the LO_1 signal is coupled by the magnetic flux from the primary coil to two secondary coils. The design parameters are shown in Fig. 16(b)–16(d). The quality factor and inductance value of the primary/two secondary coils of the trifilar (at 25 GHz) are 11.8/8.5 and 1.2 nH/0.45 nH, respectively. The self-resonances are all around 48 GHz, and the coupling factor from primary to secondary coils (k_1 and k_2) at 25 GHz is 0.51. The simulated transmission coefficients in the cases of LO_1/IF_1 excitation are shown in Fig. 16(e), (f).

Due to the port arrangements, the mutual isolations between the LO and IF ports are achieved by the trifilar. As shown in Fig. 15(a), two series-connected APDPs are placed at the remaining ports of a trifilar transformer such that the middle point of each series-connected APDPs is a virtual ground for the differential LO_1 signal. Thus, an inherently good LO_1-to-RF isolation can be attained because differential RF signals are taken from the virtual-ground points. At the same time, $2LO_1$-to-RF isolations are achieved due to the APDP configuration. In order to drive the external single-ended amplifier, a Marchand balun is used for the differential-to-single conversion. The Marchand balun adopts slotted shielding to block the lossy silicon substrate for loss reduction and to reduce the speed of the propagating wave for size reduction. Because the frequency between IF_1 and RF signals is widely separated, the IF-to-RF isolation can be achieved by the bandpass response of the Marchand balun.

There is a trade-off in the coupling design for the IF_1 and LO_1 inputs to the ports connected to the APDPs because the trifilar transformer deals with two signals with different frequencies at the same time. All the terminals are labeled as shown in Fig. 16(a). If the coupling between the LO_1 ports (terminals of 1 and $\overline{1}$) and the ports connected to the APDP (terminals of 2, $\overline{2}$, 3 and $\overline{3}$) is too high, the signal transmitted from LO_1 ports to the ports connected to the APDP increases; thus, the required LO_1 power is lowered at the cost of low transmission between IF (terminals of 4 and $\overline{4}$) and the ports connected to the

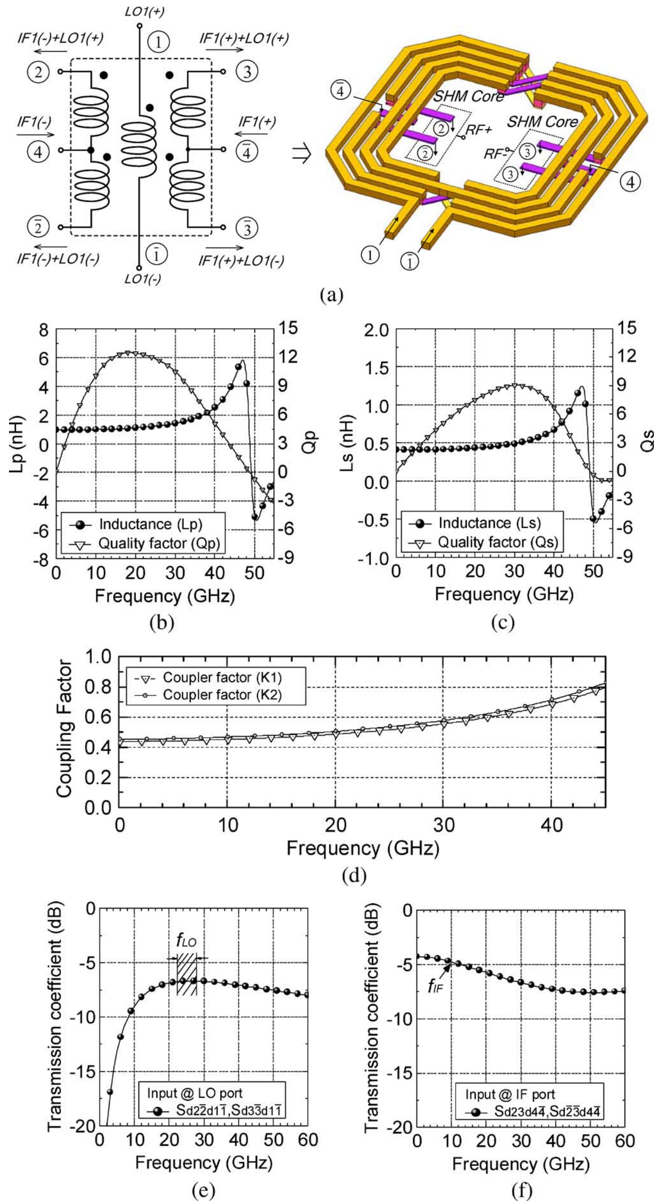

Fig. 16. (a) The trifilar schematic, (b), (c) quality factors and inductance values of the primary/two secondary cores, (d) coupling factor between primary and two secondary coils, and (e), (f) the simulated transmission coefficients in the cases of LO_1/IF_1 excitation.

APDP (terminals of 2, $\overline{2}$, 3 and $\overline{3}$). Figs. 16(e) and 16(f) show the LO_1-to-RF and IF_1-to-RF insertion loss versus operating frequency by EM-simulations. A trade-off between the LO_1 pumping power and the up-conversion loss exists in designing the coupling strength of a trifilar. In this work, the IF_1-to-RF insertion loss at 10 GHz is about 4.7 dB while the LO_1-to-RF insertion loss at 23.5 $\sim$ 28 GHz is around 7 dB. The simple analysis by hand calculation is described in Appendix A.

B. 10 GHz Single Sideband Gilbert Mixer and IF_1 Differential Driving Amplifier

The 10-GHz SSB mixer consists of two Gilbert multipliers, a quadrature generator and two center-tapped inductors. Each multiplier is composed of a double-balanced Gilbert cell ($M_5 \sim M_8$ or $M_9 \sim M_{12}$), IF_2 input trans-conductance stage ($M_1 \sim M_2$ or $M_3 \sim M_4$), and one current source. It is difficult to generate a millimeter-wave transmitting signal with good sideband rejection by a direct up-conversion because the parasitic effects degrade the amplitude and phase accuracy of IQ signals. A dual conversion remedies the problem. The SSB mixer is used to up-convert the spectrum of the desired based-band IQ signal to the IF_1 frequency with good sideband rejection at low-frequency conversion. The signal at IF_1 frequency is then up-converted to 60 GHz by an SHM. Because the high-frequency mixer does not have sideband rejection, the IF_1 frequency is set at 10 GHz to enable the undesired sideband signal generated by the high-frequency conversion to be easily filtered out by the subsequent external bandpass filter and power amplifier. Thus, generating a millimeter-wave signal with good sideband rejection is achieved by a two-step conversion. In order to overcome headroom limitation, the T-coil inductors ($L_1 \sim L_2$ and $L_3 \sim L_4$) are used as the output load for gain enhancement at $f_{IF1} = 10$ GHz.

The differential driving amplifier, employed between the SHM and the sideband-rejection mixer, raises the IF_1 output power before the IF_1 signal enters the 60-GHz SHM. Because the frequency response of a cascode configuration is better than that of a common-source configuration, a higher maximum available gain (MAG) at 10 GHz can be obtained by the former under the same DC current. Here, the size of each transistor ($M_{13} \sim M_{16}$) is $0.18 \times 4 \times 30$ μm^2. The fully-differential architecture with symmetrical layout has less sensitivity to the parasitic effects at the ac-ground point. A differential transformer (TF_1) is used at the output load to increase the dynamic range, and also to achieve conjugate impedance match to the SHM's input via a turn ratio of 1.5.

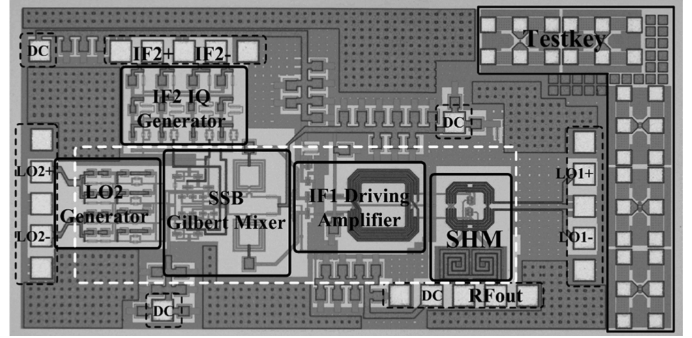

Fig. 17. Die photograph of the 60-GHz dual-conversion up-converter using 0.18-μm CMOS technology.

C. Experimental Results

The die photo of the 60 GHz dual-conversion up-converter is shown in Fig. 17. The circuit area, excluding pads and test-key, is 1.4×0.87 mm^2, and the compact 60-GHz SHM with the compact trifilar transformer occupies a mere 0.23×0.33 mm^2. The differential baseband IQ signals are generated by applying the differential signals to a two-stage polyphase shifter to facilitate the measurement. The IF_2 is designed at 1 GHz for a 2-GHz channel. If the IF_2 IQ generator is also deducted, the area of the SHM, IF_1 amplifier, SSB mixer, and LO_2 generator, is 1.4×0.44 mm^2 (as marked by the white dashed line).

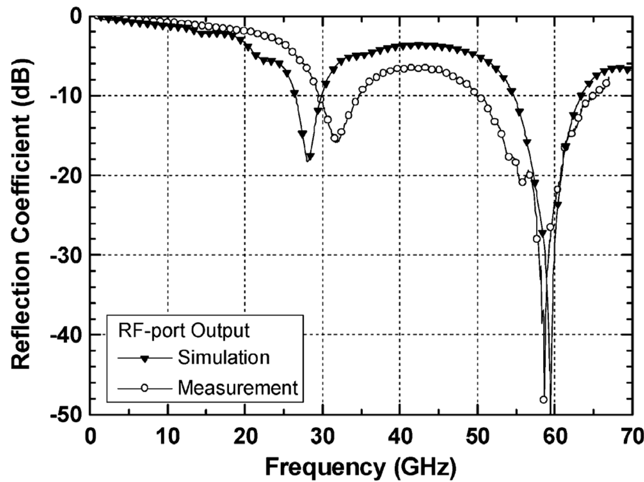

Fig. 18. Measured and simulated RF output reflection coefficient of the 60-GHz dual-conversion up-converter using 0.18-μm CMOS technology.

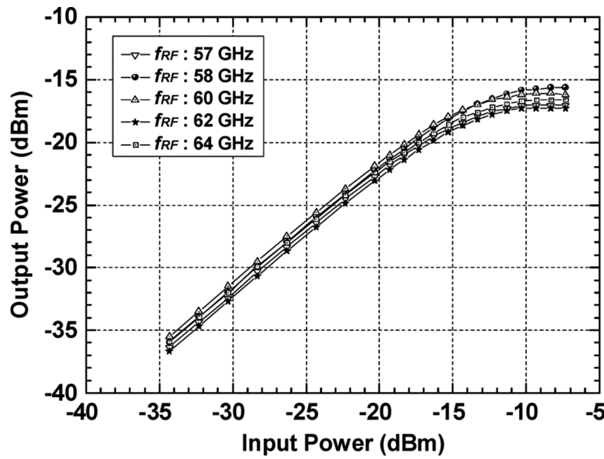

Fig. 19. 60-GHz RF output power verses baseband IF_2 input power for the different RF frequencies.

The total power consumption of the main circuit is 26 mA at a supply voltage of 2.5 V. Here, the driving IF_1 amplifier consumes most of the DC power.

Fig. 18 shows the measured and simulated S-parameter of RF output reflection coefficient. The measured RF output return below -10 dB is from 50 to 66 GHz. Fig. 19 shows the measured power performance. The $\mathrm{OP}_{1\ \mathrm{dB}}$ for each channel is close to $-17 \sim -18$ dBm and the maximum saturated power is -16 dBm at $f_{RF} = 58$ GHz. Each 60-GHz channel has an almost identical power performance. Moreover, the measured $51 \sim 66$ GHz conversion gain, shown in Fig. 20, is around -2 dB and the RF bandwidth is basically limited by the output reflection coefficient of the RF marchand balun. Within the 3-dB bandwidth, the measured OIP_3 remains around -6 dBm in most cases.

Fig. 21 shows the measured SSB output power spectrum at $f_{RF(out)} = 60$ GHz and $f_{IF2} = 1$ GHz, and the sideband rejection (SBR) reaches 41.43 dB. The SBR is better than 40 dB over $50 \sim 66$ GHz and remains nearly constant. The best performance is nearly 44 dB rejection at $f_{RF(out)} = 57$ GHz, meaning that the LO_2 quadrature signal keeps the amplitude and phase errors smaller that 0.2 dB and 1°, respectively. Moreover, the $2f_{LO1} + f_{LO2}$ (10-GHz LO_2 signal leaked to the RF interest band) suppression, referring to desired output power, is about $22 \sim 23$ dBc. The measured suppression and isolations across the entire 60 GHz bandwidth are shown in Fig. 22. Here, LO_1-to-RF isolation is about $30 \sim 40$ dB, and $2LO_1$-to-RF isolation is better than 65 dB thanks to the fully-symmetrical design of the double-balanced SHM by using the trifilar transformer and the APDPs structure.

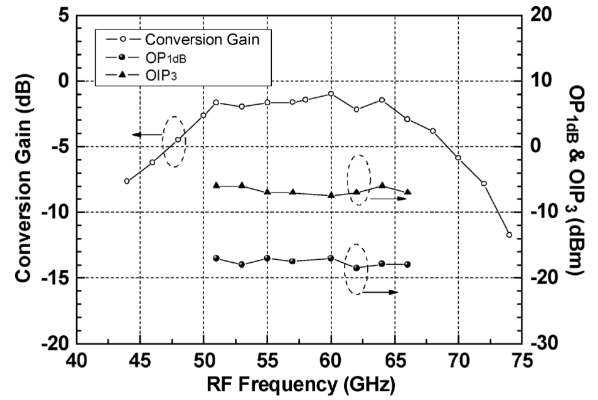

Fig. 20. Measured conversion gain of the 60-GHz dual-conversion up-converter using standard 0.18-μm CMOS technology.

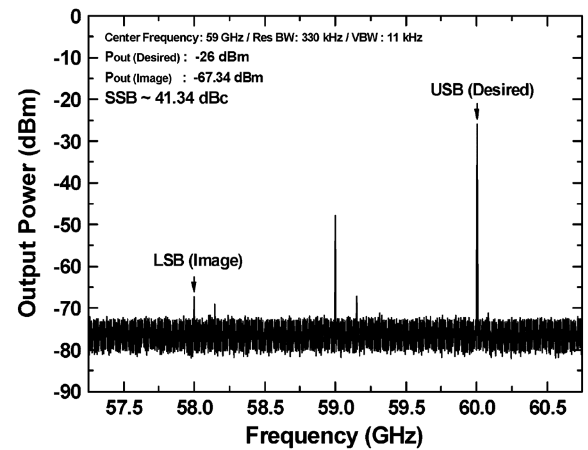

Fig. 21. Sideband rejection ratio (SBR) of the 0.18-μm CMOS 60-GHz dual-conversion up-converter at $f_{RF} = 60$ GHz.

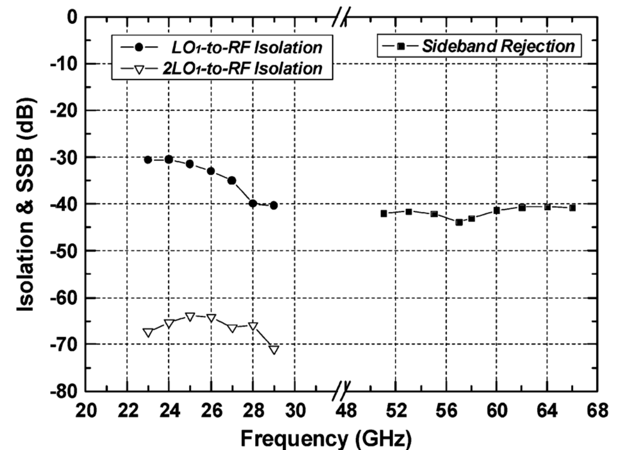

Fig. 22. Measured isolations and sideband rejection of the 60-GHz dual-conversion up-converter verses operating frequency.

TABLE II
COMPARISON OF SINGLE-SIDEBAND REJECTION OF MICROWAVE/MILLIMETER-WAVE UP-CONVERTERS

	Technology	f_{RF} (GHz)	CL (dB)	In-Band *LO2* Rejection (dBc)	SBR (dBc)	Size (mm²)
[43]	0.13 µm CMOS	20~40	13	20~30	> 20 #a	0.68x0.58
[44]	0.13 µm CMOS	35~65	6	> 24 #b	> 20	0.98x0.8
[45]	GaAs	44.5	11	10~20 #b	20~30	1.7x1.7
[46]	GaAs HBT	50~110	< 20	15~23	22	2.0x2.0
[47]	GaAs	76.5	12~15	< 10	24	2.0x1.6
[48]	Hybrid	60	14.2	N.A.	> 20	5.15x1.35
[49]	90-nm CMOS #d	60	N.A.	N.A.	20 #c	0.49x0.42
This work	0.18 µm CMOS #d	57~65	1	22 ~ 23 #e	**> 40 #f**	1.5x0.87

#a SSB $>$ 40 dBc only from 27 GHz to 30 GHz
#b 2 $*$ LO Suppression (SHM)
#c SSB is achieved by using polyphase filter at 60 GHz
#d Dual-conversion up-converter
#e 2 $* f_{LO1} + f_{LO2}$ suppression (DUC)
#f This performance **almost remains the same** over whole interesting 60 GHz bandwidth.

The performances of the 60-GHz up-converter and other state-of-the art up-converters at millimeter-wave frequency are summarized in Table II. Our proposed dual-conversion up-converter has the highest SBR over the 60 GHz bandwidth of any circuit on the list.

V. CONCLUSION

The introduction of Schottky diodes with a cut-off frequency of several hundred GHz in standard CMOS process has changed the scenario of the scaling rule. This enabling technology makes possible the implementation of 60-GHz dual-conversion up-/down-converters using 0.18-μm foundry CMOS process even though MOS transistors have only f_T/f_{max} of 50-GHz/60-GHz. Additionally, both microwave/millimeter-wave and analog design approaches are used to accomplish the low-cost 60-GHz transceiver. In the dual-conversion architecture, 60 GHz Schottky-diode SHMs are employed in the high-frequency conversion while analog mixers with accurate IQ signal generation are chosen for low-frequency conversion. Because the silicon-based Schottky diode possesses a low turn-on voltage and the advanced passive circuits, such as the proposed phase-inverter rat-race coupler and trifilar transformer, are available, the Schottky-diode millimeter-wave mixers using 0.18-μm foundry CMOS process become practical. The demonstrated 60-GHz dual-conversion down-converter, operating from 57 $\sim$ 66 GHz, has conversion gain of 5 dB, $\mathrm{IP}_{1\ \mathrm{dB}}$ of -5 dBm and IIP_3 of 5 dBm. The corresponding Schottky-diode SHM requires only the small LO power of 1 dBm. For the 60-GHz dual-conversion up-converter, conversion gain of -2 dB, $\mathrm{OP}_{1\ \mathrm{dB}}$ of -17 dBm, and broadband sideband rejection better than 40-dB are achieved. Based on the results of this work, incorporating the demonstrated 0.18-μm CMOS dual-conversion up-/down-converters with high-performance HEMT-based LNA and PA gives an alternative attractive solution for 60-GHz transmission.

APPENDIX A
ANALYSIS FOR A TRIFILAR WITH DIFFERENT EXCITATIONS

The simple equivalent model of the trifilar with turn ratio of 2:1:1 is shown in Fig. 23. k is magnetic coupling factor, and n is equal to $(L_P/L_S)^{1/2}$. k^2L_P and $(1-k^2)L_P$ represent the magnetizing and leakage inductances of the primary coil, respectively. The simulated mutual coupling among two secondary coils is around 0.1, much smaller than that between primary and secondary coils, and thus is ignored here. Two impedances of $n^2k^2(Z_L+r_S)$ reflected from port 2 and port 3 are in parallel with the shunt inductance $\mathrm{k^2L_P}$, as illustrated in Fig. 23(b). In this work, $Z_L = 50\ \Omega$. $L_P(L_S)$ and $r_p(r_S)$ are the self-inductance and parasitic resistance of primary (secondary) winding, respectively.

The voltage transformation in consideration of the leakage inductance effect and parasitic resistance is as follows:

$$\frac{V_2}{V_S} = \frac{V_2^+ + V_2^-}{V_S^+ + V_S^-} = \frac{\left(\dfrac{\dfrac{n^2k^2(Z_L+r_S)}{2}\times j\omega k^2L_P}{\dfrac{n^2k^2(Z_L+r_S)}{2}+j\omega k^2L_P}\right)}{j\omega(1-k^2)L_P+\left(\dfrac{\dfrac{n^2k^2(Z_L+r_S)}{2}\times j\omega k^2L_P}{\dfrac{n^2k^2(Z_L+r_S)}{2}+j\omega k^2L_P}\right)+r_P} \times \frac{1}{nk}\times\frac{Z_L}{r_S+Z_L} \tag{A.1}$$

where the relation between $\mathrm{V_S^-}$ and $\mathrm{V_S^+}$ is defined as follow,

$$V_S^- = \left(S_{11}|_{V_2^+=V_3^+=0}\right)V_S^+. \tag{A.2}$$

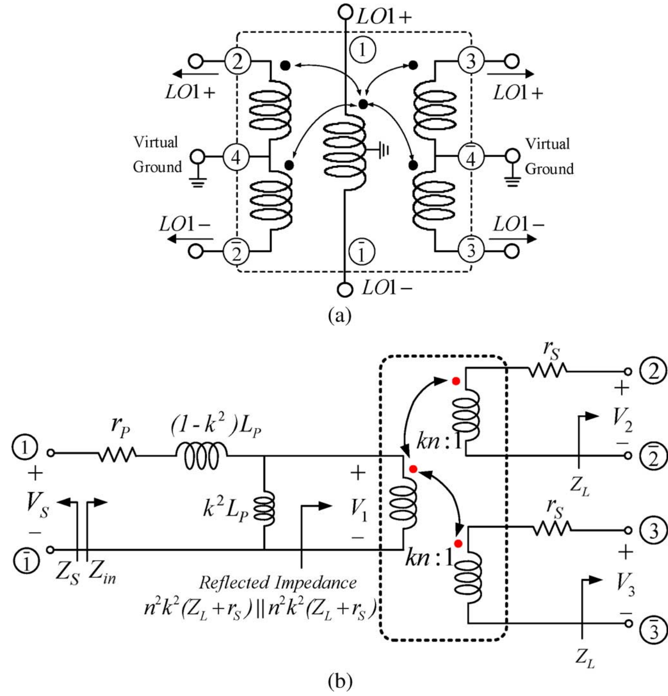

Fig. 23. (a) The diagram of the trifilar excited by a differential LO1 signal and (b) a simple equivalent model of the trifilar.

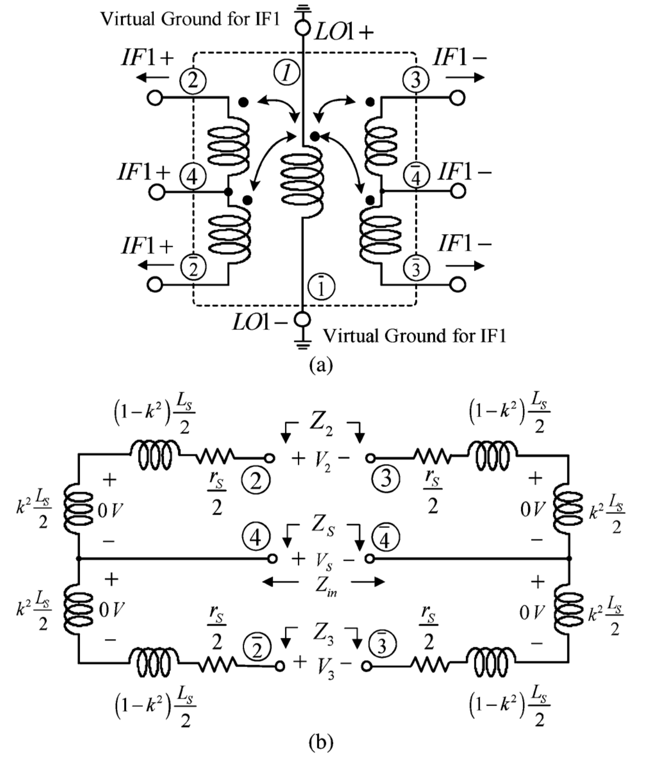

Fig. 24. (a) The diagram of the trifilar excited by a differential IF_1 signal and (b) the simple equivalent model.

We can get the deviation of S_{21} by (A.1) and (A.2)

$$S_{21}|_{V_2^+=0,\ V_3^+=0} = \frac{V_2^-}{V_S^+} = \left(1+S_{11}|_{V_2^+=V_3^+=0}\right)\times\frac{V_2}{V_S} \quad \text{(A.3)}$$

and the reflected coefficient of S_{11} is expressed as follows:

$$S_{11}|_{V_2^+=V_3^+=0} = \frac{Z_{\text{in}}-Z_S}{Z_{\text{in}}+Z_S} = \frac{\left(j\omega(1-k^2)L_P+\dfrac{\dfrac{n^2k^2(Z_L+r_S)}{2}\times j\omega k^2L_P}{\dfrac{n^2k^2(Z_L+r_S)}{2}+j\omega k^2L_P}+r_P\right)-Z_S}{\left(j\omega(1-k^2)L_P+\dfrac{\dfrac{n^2k^2(Z_L+r_S)}{2}\times j\omega k^2L_P}{\dfrac{n^2k^2(Z_L+r_S)}{2}+j\omega k^2L_P}+r_P\right)+Z_S} \quad \text{(A.4)}$$

where $\mathrm{Z_S} = 50\ \Omega$. The calculated S_{21} is around -6.5 dB at 25 GHz according to the simulated parameters of the trifilar ($L_P =$ 1.22, nH, $L_S = 0.45$ nH, $k = 0.51$, $r_p = 16\ \Omega$, $r_S = 8.2\ \Omega$ and $n = 1.63$ at $f_{LO1} = 25$ GHz). The simple analysis is close to the simulated loss value of 7 dB in Fig. 16(e).

When the trifilar is excited by a differential IF signal from the two center-tape ports, the LO port illustrated in Fig. 24(a) is the virtual ground for the IF signal. Fig. 24(b) shows the simple equivalent model of the trifilar for estimating IF_1 transmission coefficient. The magnetizing inductance of k^2L_S is shorted due to the virtual ground of the primary coil as shown in Fig. 24(b), and only leakage inductance of $(1-k^2)L_S$ and parasitic resistance (r_S) are considered in the voltage transformation between the IF input and output ports.

The voltage transformation between IF input (port of $4\bar{4}$) and two output ports (ports of 23 and $\overline{23}$) can be obtained by the voltage-division rule

$$\frac{V_2}{V_S} = \frac{V_2^+ + V_2^-}{V_S^+ + V_S^-} = \frac{Z_0}{Z_0 + j\omega(1-k^2)L_S + r_S} \quad \text{(A.5)}$$

where $V_S^- = (S_{11}|_{V_2^+=V_3^+=0})V_S^+$. Here, the reflected coefficient of S_{11} is as follows:

$$S_{11}|_{V_2^+=V_3^+=0} = \frac{V_S^-}{V_S^+} = \frac{Z_{\text{in}}-Z_S}{Z_{\text{in}}+Z_S} = \frac{\left(\dfrac{Z_0}{2}+j\omega(1-k^2)\dfrac{L_S}{2}+\dfrac{r_S}{2}\right)-Z_S}{\left(\dfrac{Z_0}{2}+j\omega(1-k^2)\dfrac{L_S}{2}+\dfrac{r_S}{2}\right)+Z_S} \quad \text{(A.6)}$$

and the deviation of S_{21} is similar as the case of LO excitation by applying (A.5) and (A.6) to (A.3). At $f_{IF1} = 10$ GHz, $L_S =$ 0.41 nH, $r_S = 8.2\ \Omega$, $k = 0.45$ and n is 1.54. By the hand calculation, we can obtain $\mathrm{S}_{21} = -4.1$ dB at 10 GHz, similar to the simulated loss value of 4.7 dB in Fig. 16(f).

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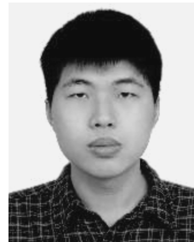

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