All Digital Linear Voltage Regulator for Super- to Near-Threshold Operation

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***Abstract*—In this paper, an all digital push-pull linear voltage regulator is proposed that consists of a digital error detector, a voltage divider, a mode indicator, a pull device, and grouped push devices. The digital regulator is suitable for super- to near-threshold region operation by providing a variable output voltage that ranges from 0.5 to 1 V in steps of 0.1 V. The maximum load current is 100 mA for every output level. The current efficiency is 99.8% with only 164.5 μA quiescent current on UMC 65-nm standard CMOS technology. A response time constraint is developed to provide a design guideline for (all) the digital control system. It describes the correlation between required speed of the digital control system, the output performance and the size of the decoupling capacitor. A time interleaving control technique is then proposed to have a tradeoff between output performance, quiescent current, and the size of decoupling capacitor.**

***Index Terms*—Current efficiency, digital, linear regulator, push-pull, response time constraint, time interleaving.**

I. Introduction

FUTURE applications span from high-performance processors and portable wireless applications, to sensor nodes and medical implants [1]. Power has become the primary design concern for all these applications. The full spectrum of the supply voltage from super- to subthreshold region is explored to enhance the power/energy efficiency. In order to provide more flexibility on power control, scalable supply voltage [2], [3] were presented which requires variable power supplies. The emerging heterogeneous multicore and system-on-a-chip (SoC) designs further complicate the power structure because multiple adjustable power supplies can be demanded. Fully integration of power supplies is also preferred to reduce the cost.

Switching converters [4]–[8] and linear regulators [9]–[15] are two basic types of power supplies. Switching converters can use capacitive (switched capacitor converter) or inductive (buck converter) energy storage. Switched capacitor converter [4] is usually used for low voltage and light load environment whereas buck converters [5]–[8] are usually for large load environments. Switching converters have the potential for more than 90% power efficiency [5] and are capable of digital control. For example, delay lock loop technique was used for multiphase control [6] and a continuous-time digital controller [7] was also presented in literature. Large integration area cost is the major issue of switching converters especially the ones that use inductive energy storage.

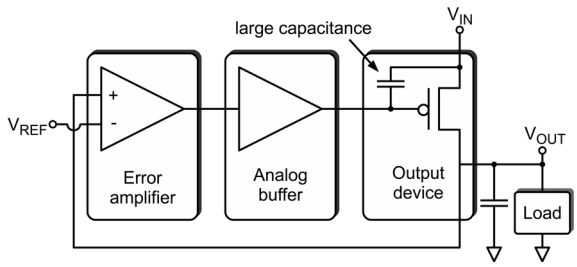

Fig. 1. Conventional analog style linear regulator [14].

On the other hand, linear regulators are much easier to be integrated on-chip without area consuming inductors. Conventionally linear regulators use analog building blocks as the example shown in Fig. 1. An analog error amplifier determines the difference between the regulated voltage and the reference voltage. The output devices with a large gate capacitance are controlled by the output of the amplifier through an analog buffer. The advantage of analog linear regulators is the continuous time response that can respond immediately to system condition change.

The maximum power efficiency of the linear regulator is limited by the ratio of output and input voltages. Therefore, low drop-out characteristic [9]–[12] is preferred when designing linear regulators. And low quiescent current is desired to maintain a good power efficiency. However, small quiescent current results in slower circuit response in analog circuits. Meanwhile, analog circuits usually have transistor stacking and rely on device matching in some structures. These characteristics make analog circuits suffer from voltage scaling and technology scaling [16].

The design of analog circuits has become more difficult in advanced technology. Digital assisted analog circuits were then suggested to leverage digital-computing capabilities to improve power and performance of analog electronics [17]. Unlike analog circuits, digital circuits consume very little current in steady state and provide large output current when switching. They function well as the supply voltage decreases. Digital circuits are also easy for technology migration without a redesign from the beginning.

The digital controlled linear regulator such as ones in [14], [15] is therefore a good candidate that combines both advantages of digital circuit and linear regulators. The work in [14], however, is not quite digital although the authors used inverters

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to construct the control system. The circuits still behaved as amplifiers whereas the outputs of such amplifiers were then digitized by skewed inverters. This analog-like behavior also drew a large 25.7 mA quiescent current. A real digital regulator was presented in [15] aiming at a 200 μA low load condition. It used a clocked comparator to replace the analog error amplifier and 256 flip-flops to control the output devices. Though the reported quiescent current was as low as 2.7 μA, it used a relatively large 0.1 μF decoupling capacitor and the system control loop speed was only 1 MHz. In this paper, the proposed digital controlled linear regulator will be designed for large load conditions with fast control loop time, real digital behavior and low quiescent current.

On the other hand, it was also suggested that the near-threshold region operation retains much of the energy savings of subthreshold region with more favorable performance and variability characteristics [1], [18]. Most of the applications can benefits from a scalable voltage from super- to near-threshold region in terms of both performance and energy saving. Consequently, the proposed digital controlled linear regulator is designed to provide a variable output voltage ranging from 1 to 0.5 V in steps of 0.1 V.

The rest of this paper is organized as follows. Section II presents the architecture of the proposed digital controlled voltage regulator. The response time constraint for the digital control system and the proposed time interleaving control are also reported in this section. Section III evaluates the accuracy of the digital control system in the presence of variations. Technology migration of the digital regulator is demonstrated in Section IV. Section V presents the experimental results of the test chip and some discussions. Finally Section VI concludes this paper.

II. Digital Controlled Linear Regulator

The digital controlled voltage regulator was first proposed in [19]. It is designed to provide a variable regulated voltage ranging from 1 to 0.5 V in steps of 0.1 V. The maximum load current is 100 mA for every output voltage level. The idea of the proposed digital controlled linear regulator is to replace the analog building blocks shown in Fig. 1 with their digital counterparts.

The architecture of the proposed digital controlled linear regulator is presented in Fig. 2. Push-pull topology as in [13] is used. The major components are a digital error detector (DED), a voltage divider, a mode indicator, a pull device, and grouped push devices with their own drivers. The digital error detector is the replacement of the analog error amplifier. The voltage divider, the mode indicator and the grouped output devices are designed for the purpose of variable output voltage. The analog buffer in Fig. 1 is replaced by digital control logics and drivers of the output devices.

A. Digital Control System

In previous works, analog amplifiers were used for comparing regulated output with reference voltage [4], [6] or for analog-to-digital conversion (ADC) [7], [20]. The use of analog amplifiers partly negates the benefits of digital control. In this work, the proposed digital error detector is a fully digital circuit block with

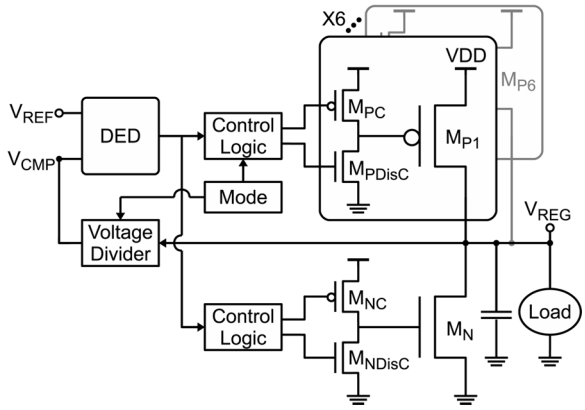


Fig. 2. Block diagram of the proposed digital controlled linear regulator.

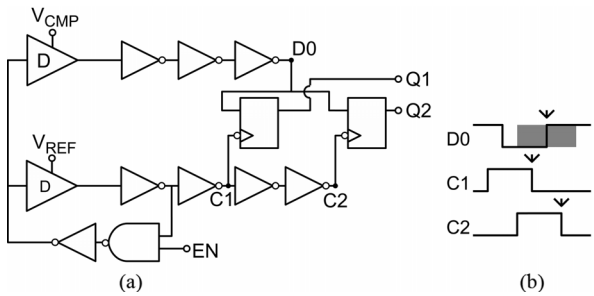


Fig. 3. (a) Block diagram of the digital error detector and (b) illustrative waveforms.

real digital behavior. It adapts the concepts of delay line-based ADC [21] and phase comparison techniques to compare voltage signals digitally. Typical delay line based ADC uses a long delay line, e.g., 1 ns [21] and longer, to have a good resolution. Long delay line results in slow control response of linear regulator. Therefore, short delay line is used instead in this work.

The block diagram of the DED is shown in Fig. 3(a). Two delay lines are implemented in parallel and controlled by regulated voltage (divided version, denoted as $V_{\rm CMP}$ in the figure) and reference voltage ($V_{\rm REF}$), respectively. The delay line includes one voltage controlled delay cell and several standard inverters for waveform shaping. Both delay lines are triggered by the ring oscillator forming from the reference delay path. It makes sure that two delay lines are synchronized. The DED can be activated or deactivated by an "enable" signal.

Voltage-to-delay transformations of $V_{\rm CMP}$ and $V_{\rm REF}$ are performed through two delay lines. Transformed delay informations are phase compared using two flip-flops as shown in Fig. 3(a). The flip-flops are clocked by the reference path delay line to capture the output of the comparison path. Illustrative waveforms are shown in Fig. 3(b). Meaningful edges of each signal are marked in the figure.

D0 edge will vary in the range of gray area depicted in Fig. 3(b) as $V_{\rm CMP}$ changes. If $V_{\rm CMP}$ is equal to $V_{\rm REF}$, D0 edge will lie in the middle of C1 and C2 edges. The values of captured Q1 and Q2 are "0" and "1", respectively. When $V_{\rm CMP}$ is lower than $V_{\rm REF}$, delay line controlled by $V_{\rm CMP}$ will be faster. Therefore, Q1 and Q2 will both capture logic "1" values. Logic "0" will be captured in both Q1 and Q2 when $V_{\rm CMP}$ is higher than $V_{\rm REF}$. The resolution of phase comparison in

TABLE I
STATES OF Q1/Q2 CORRESPONDING TO $V_{\rm CMP}$

V_{CMP} States	Q1	Q2
V_{CMP} <0.495V	1	1
0.495V <V_{CMP} <0.505V	0	1
0.505V <V_{CMP}	0	0

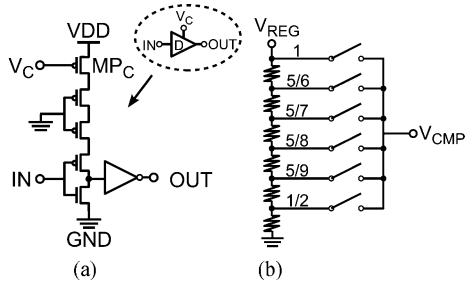


Fig. 4. Schematics of (a) the voltage controlled delay cell and (b) the voltage divider.

DED is one inverter delay since ideally C1 and C2 edges have one inverter delay earlier and later than D0 edge, respectively. The design of the voltage controlled delay cell determines the voltage resolution of DED. In this work, the delay variation will exceed one inverter delay at a 5 mV control voltage deviation. Therefore, the resolution of DED will be $\pm$ 5 mV for $V_{\rm CMP}$ to lock at $V_{\rm REF}$. The corresponding states of $V_{\rm CMP}$, Q1 and Q2 are listed in Table I. The maximum error of the regulated voltage will be $\pm$ 10 mV at 1 V output in steady state since a 1/2 dividing ratio is applied.

There is a possibility that one of the flip-flops is meta-stable since the position of D0 edge varies. However, the signals at data and clock input of flip-flops are already shaped by several inverters as shown in Fig. 3(a). The switching slopes of the signals are sharp such that meta-stable state rarely happens. It is more possible that the setup time and hold time of flip-flops are violated when $V_{\rm CMP}$ is at the boundary of DED's detection resolution. One of Q1 and Q2 may not be the expected value. However, this is not a serious issue. As the regulated output changes to go beyond the detection resolution, the DED can produce correct Q1/Q2 values as soon as in the next trigger period.

The schematic of the voltage controlled delay cell is shown in Fig. 4(a). Note that instead of using control voltage as supply of the delay cell [21], the control voltage is fed to the gate node of MP_C and denoted as V_C. The grounded pMOS transistors are inserted to reduce the coupling noise to V_C from the switching of the delay line. The fact that the delay cell is supplied by the input voltage results in a little degradation on the number of current efficiency. However, there is no difference in the big picture since all the load circuit and the control system are equivalently powered by the input voltage supply. Therefore, regardless of slightly current efficiency degradation, the configuration is used because it can reduce the perturbation from the control system to the regulated voltage.

The voltage controlled delay cell is designed to work around the reference voltage which is assumed to be 0.5 V. In order to have a comparable pair of reference and regulated voltages, a voltage divider is required to divide the regulated voltage to 0.5 V when it is higher than that. The divided regulated voltage is denoted as $V_{\rm CMP}$. Fig. 4(b) depicts the resistive voltage divider. It takes the regulated voltage, $V_{\rm REG}$, as input and provides five different dividing ratios. Together with non-divided $V_{\rm REG}$, there are six intermediate dividing results. Only one intermediate result will be passed to the $V_{\rm CMP}$ output by the switch. The switching task is managed by the mode indicator. For example, if 0.7 V regulated voltage is demanded, the mode indicator will activate the third switch. The regulated voltage will be equal to 0.7 V when $V_{\rm CMP}$ from 5/7 dividing ratio is locked at $V_{\rm REF}$ through the voltage-to-delay transformation by delay lines.

TABLE II
STATES OF OUTPUT DEVICES CORRESPONDING TO Q1/Q2

Q1	Q2	M_{PC}	M_{PDisC}	M_{P1}	M_{NC}	M_{NDisC}	M_N
1	1	OFF	ON	ON	OFF	ON	OFF
0	1	OFF	OFF	(HOLD)	OFF	ON	OFF
0	0	ON	OFF	OFF	ON	OFF	ON

The acquired Q1/Q2 results are used to control the push and pull devices. To simplify the description, one push device with its drivers is assumed here. As Fig. 2 shows, the push device M_{P1} is control by a p-type driver $M_{\rm PC}$ and a n-type driver $M_{\rm PDisC}$. The states of the drivers and the resulting statuses of the push device M_{P1} corresponding to Q1 and Q2 are listed in Table II. For example, if regulated output is too low, Q1 and Q2 will be both logic "1" and $M_{\rm PDisC}$ will be turned on whereas $M_{\rm PC}$ will be turned off. As a result, M_{P1} is turned on to supply current and to charge up the regulated output. Note that there is a HOLD condition for M_{P1} that both of its drivers are OFF when the regulated output is equal to the target value. The exact state (ON or OFF) of M_{P1} depends on the previous condition of the regulated output. If the regulated output is too low previously, M_{P1} will remain ON, otherwise it will remain OFF. As a result, the stabled regulated output tends to be a little higher than the target value.

The states of the pull device M_N and its drivers M_{NC} and $M_{\rm NDisC}$ are also listed in Table II. The pull device is turned on only when the regulated output is too high, i.e., Q1/Q2 are both logic "0". It can be observed in the table that the state patterns of the drivers and Q1/Q2 have great similarity. Hence $M_{\rm PC}$, M_{NC}, and $M_{\rm NDisC}$ can be directly controlled by Q2 whereas $M_{\rm PDisC}$ is controlled by Q1. There is no complex control logic. Only adequate inverter based fan-out buffers are used to propagate the control signals. Fig. 5 shows a simplified diagram of control logics passing Q1/Q2 to drivers by fan-out buffers. The sizes of fan-out buffers and the drivers are configured such that the turn-on/turn-off speed of push and pull devices is acceptable.

As described, the output devices (push and pull) and their drivers are all digitally controlled that can only be fully turned on or off. The magnitude of supplied current when the push devices are ON depends on the drain-source voltage $(V_{\rm DS})$ and the size of the push devices. The drain-source voltages $(V_{\rm DS})$ will be different when the regulator supplies different output voltages. Note that the target supply levels (0.5 to 1 V in steps of 0.1 V) are considered here while ignoring voltage ripples. The total size of push devices must meet the requirement of maximum load current at highest 1 V output voltage. However,

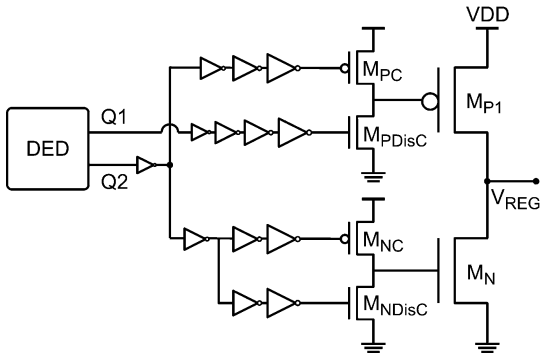


Fig. 5. Simplified block diagram of control logics by using fan-out buffers.

TABLE III
GROUP OF PUSH DEVICES ACTIVATION STATUS

Output Voltage	Push Devices					
	G#1	G#2	G#3	G#4	G#5	G#6
0.5V	Act.	OFF	OFF	OFF	OFF	OFF
0.6V	Act.	Act.	OFF	OFF	OFF	OFF
0.7V	Act.	Act.	Act.	OFF	OFF	OFF
0.8V	Act.	Act.	Act.	Act.	OFF	OFF
0.9V	Act.	Act.	Act.	Act.	Act.	OFF
1.0V	Act.	Act.	Act.	Act.	Act.	Act.

the same amount of push devices will be providing up to 4× current at lowest 0.5 V output voltage because of increased $V_{\rm DS}$. This current boost is unnecessary and also impacts the stability of the regulated voltage. Therefore, the push devices are divided into six groups and operated in an accumulative manner.

Table III lists the accumulative activation statuses of six push device groups. Only the first group is activated when providing the lowest 0.5 V output voltage whereas all six groups are activated for highest 1 V output voltage. The sizes of groups are designed such that it can supply 100 mA in each output level. The grouping configuration also reduces the charge/discharge power since the gate capacitance is reduced for fewer activated groups. For each target level, the activated groups of output devices are all directly controlled by Q1/Q2 to turn on or off simultaneously for regulation. Different fan-out buffer trees and drivers are used for different groups such that individual enable/disable function can be embedded in the buffer trees.

Conventional analog regulator uses amplifier to detect error and to drive the output devices. The design of the amplifier and the output devices are correlated. In the proposed technique, however, the output devices are decoupled from the DED since the output devices and their drivers are all digitally controlled (by Q1 and Q2). The total size of output devices, the maximum load current and the dropout voltage are mutual correlated parameters. Very low dropout voltage and large load current can be simultaneously achieved as long as the sizes of output devices are large enough. Consequently, the maximum load current and the dropout voltage can be arbitrarily chosen depending on the target application while the DED remains the same. Only fan-out buffers from Q1/Q2 as well as the drivers need to be resized for acceptable switching speed of output devices.

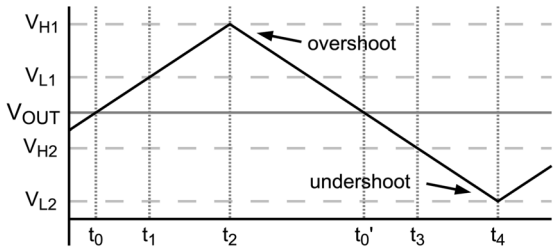


Fig. 6. Illustration of overshoot and undershoot of the regulated voltage.

B. Response Time Constraint

Discrete operation is the major drawback when using digital control circuit for linear regulator. The control system cannot respond to the change of the regulated voltage until next trigger. If the trigger period is too long and the decoupling capacitor is too small, the regulated voltage ripple will be large. The requirement of the control loop response will be investigated in this section in terms of the relationship between the control loop response time, the size of the decoupling capacitor and the maximum ripple of the regulated voltage.

Fig. 6 is the illustration of overshoot and undershoot of the regulated voltage for analysis. $V_{\rm OUT}$ is the target output voltage. V_{H1} and V_{L2} specify the upper and lower bounds of voltage ripple, respectively. The digital control system will be evaluated separately for voltage overshoot and undershoot situations.

The region from t_0 to t_2 in Fig. 6 depicts the voltage overshoot. In the worst case, there is no discharge current (neither pull current nor load current). Only push current exists to charge up the decoupling capacitor. Note that the voltage-to-delay transformation of DED described in Section II-A actually averages the input voltage during the transformation period. Considering the worst case again, the transformation acts from t_0 to t_1. The produced average deviation is just equal to DED's resolution such that it is not recognizable by DED. Meanwhile, V_{L1} at t_1 will be a deviation of twice the resolution value from $V_{\rm OUT}$. The next voltage-to-delay transformation of the control loop starts at t_1. At t_2 the push devices have been turned off such that the upper bound V_{H1} is not exceeded. The required control loop response time, T_R, for upper bound V_{H1} is defined as $t_2 - t_1$. In this time period, the control system needs to detect the overshoot and to respond by turning off push devices. Therefore, T_R includes both the DED detection time, T_{V2D} and the control signal propagation delay, T_D.

The value of the regulated voltage is related to the total charge stored in the decoupling capacitor as

$$Q = CV_{\rm OUT} \tag{1}$$

where Q is the total charge, $V_{\rm OUT}$ is the value of the regulated voltage and C is the decoupling capacitor. The charging current, i.e., push current, can be obtained from differentiating (1) as

$$I_{\rm push}(V_{\rm OUT}) = \frac{dQ}{dt} = C\frac{dV_{\rm OUT}}{dt}. \tag{2}$$

The push devices are in the linear region. So (2) becomes

$$\frac{1}{2}k(V_{\rm DD} - V_{\rm OUT})(V_{\rm DD} + V_{\rm OUT} - 2V_{\rm th}) = C\frac{dV_{\rm OUT}}{dt} \tag{3}$$

where $V_{\rm DD}$ is the supply voltage, k and $V_{\rm th}$ are the process transconductance parameter and the threshold voltage of the push device, respectively. Equation (3) can be rewritten in differential form as

$$dt = \frac{2CdV_{\rm OUT}}{k(V_{\rm DD}-V_{\rm OUT})(V_{\rm DD}+V_{\rm OUT}-2V_{\rm th})}. \quad (4)$$

Then both sides are integrated with time from t_1 to t_2 and $V_{\rm OUT}$ from V_{L1} to V_{H1} as

$$\int_{t_1}^{t_2} dt = \int_{V_{L1}}^{V_{H1}} \frac{2CdV_{\rm OUT}}{k(V_{\rm DD}-V_{\rm OUT})(V_{\rm DD}+V_{\rm OUT}-2V_{\rm th})}. \quad (5)$$

Therefore, the relationship between control loop response time T_R and upper bound V_{H1} of voltage ripple is

$$\begin{aligned} &T_{R,\rm overshoot} \\ &= t_2 - t_1 \\ &= \frac{C}{k(V_{\rm DD}-V_{\rm th})} \ln\Big(\frac{V_{\rm DD}-V_{L1}}{V_{\rm DD}-V_{H1}} \cdot \frac{V_{\rm DD}+V_{H1}-2V_{\rm th}}{V_{\rm DD}+V_{L1}-2V_{\rm th}}\Big). \end{aligned} \quad (6)$$

Note that V_{L1} is defined as twice of DED's resolution value based on the worst case analysis.

Similar procedure is applied to undershoot situation from t_0' to t_4 in Fig. 6 when the decoupling capacitor is discharged. In the worst case, the next control loop starts at t_3 and both pull current and maximum load current exist to discharge the decoupling capacitor. The lower bound of the voltage ripple is V_{L2} at t_4 whereas V_{H2} shares the same concept with V_{L1}. The discharge current can be expressed as

$$-[I_{\rm pull}(V_{\rm OUT}) + I_{ML}] = \frac{dQ}{dt} = C\frac{dV_{\rm OUT}}{dt} \quad (7)$$

where $I_{\rm pull}(V_{\rm OUT})$ is the pull current and I_{ML} is the maximum load current. Note that the pull current is a function of $V_{\rm OUT}$ but the load current is assumed to be independent.

The pull device can be in linear or saturation region depending on the output voltage. If the pull device is in linear region, (7) becomes

$$-\Big[\frac{1}{2}kV_{\rm OUT}(2V_{\rm DD}-2V_{\rm th}-V_{\rm OUT})+I_{ML}\Big] = C\frac{dV_{\rm OUT}}{dt} \quad (8)$$

where k and $V_{\rm th}$ are the process transconductance parameter and the threshold voltage of the pull device, respectively. Again (8) is rewritten in differential form and integrated on both sides

$$\int_{t_3}^{t_4} dt = \int_{V_{H2}}^{V_{L2}} \frac{2CdV_{\rm OUT}}{k\Big(V_{\rm OUT}^2 + 2(V_{\rm th}-V_{\rm DD})V_{\rm OUT} - \frac{2I_{ML}}{k}\Big)}. \quad (9)$$

Hence T_R for undershoot in this case can be expressed as

$$\begin{aligned} &T_{R,\rm undershoot,lin} \\ &= t_4 - t_3 \\ &= \frac{2C}{k\sqrt{a^2-4b}} \ln\left[\frac{-1+\frac{2(V_{L2}-V_{H2})}{\sqrt{a^2-4b}}+\frac{(a+2V_{L2})(a+2V_{H2})}{a^2-4b}}{-1+\frac{2(V_{H2}-V_{L2})}{\sqrt{a^2-4b}}+\frac{(a+2V_{L2})(a+2V_{H2})}{a^2-4b}}\right] \end{aligned}$$

TABLE IV
RESPONSE TIME CONSTRAINT FOR DIFFERENT CONFIGURATIONS

	$T_{R,overshoot}$ (ns)			$T_{R,undershoot}$ (ns)		
Decap. Size	1.5nF	3nF	4.5nF	1.5nF	3nF	4.5nF
V_{OUT}=1V	0.684	1.368	2.052	0.407	0.813	1.220
V_{OUT}=0.9V	0.528	1.055	1.582	0.435	0.870	1.305
V_{OUT}=0.8V	0.525	1.049	1.574	0.464	0.927	1.391
V_{OUT}=0.7V	0.539	1.077	1.616	0.492	0.984	1.476
V_{OUT}=0.6V	0.562	1.123	1.685	0.522	1.043	1.565
V_{OUT}=0.5V	0.587	1.174	1.761	0.553	1.106	1.659

$$\begin{aligned} a &= 2(V_{\rm th}-V_{\rm DD}) \\ b &= -\frac{2I_{ML}}{k}. \end{aligned} \quad (10)$$

On the other hand, if the pull device is in saturation region, (7) becomes

$$-\Big[\frac{1}{2}k(V_{\rm DD}-V_{\rm th})^2(1+\lambda V_{\rm OUT}) + I_{ML}\Big] = C\frac{dV_{\rm OUT}}{dt} \quad (11)$$

where λ is the channel length modulation parameter. Through the same procedure, T_R can be expressed as

$$\begin{aligned} T_{R,\rm undershoot,sat} &= \frac{2C}{a\lambda}\ln\Big(\frac{a\lambda V_{H2}+a+2I_{ML}}{a\lambda V_{L2}+a+2I_{ML}}\Big) \\ a &= k(V_{\rm DD}-V_{\rm th})^2. \end{aligned} \quad (12)$$

Based on (6), (10), and (12), the required response time of the digital control loop is related to the size of the decoupling capacitor, the upper/lower bound of the voltage ripple, the maximum load current, the magnitude of the push/pull current, and the output voltage level.

Table IV lists the numerical results of response time constraint for different output voltages and different sizes of the decoupling capacitor. Both the upper and the lower bounds of the voltage ripple are set to be 50 mV. I_{ML} is 100 mA. Note that for the undershoot situation, (10) is used for $V_{\rm OUT} \le 0.7$ V whereas (12) is used for $V_{\rm OUT} \ge 0.8$ V.

It can be observed from Table IV that the response time constraint is relaxed when the decoupling capacitor is larger. It is intuitive since more charge buffers are provided by larger decoupling capacitor. So the reaction time of the control system can be longer.

For overshoot situations with the same size of decoupling capacitor, the response time constraint exhibits a concave curve that the minimum value occurs at $V_{\rm OUT} = 0.8$ V. It is not surprising because the push current is a quadratic function of $V_{\rm OUT}$ according to (3). At higher regulated output voltages the push current decreases rapidly as voltage overshoot increases. Therefore, the response time constraint is looser for 1 and 0.9 V regulated outputs.

On the other hand, the response time constraint shows a progressive decrease for undershoot case as the output voltage increases. The load current is assumed to be constant whereas the pull current is larger at higher regulated output. Therefore, the response time constraint becomes tighter to keep the same undershoot specification.

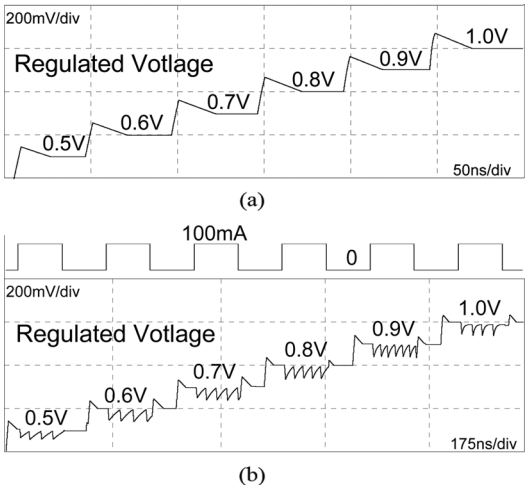


Fig. 7. Simulated waveforms of (a) output mode changing with zero load and (b) step response at full load current.

The constraints of undershoot situations should be considered when designing the regulator since they are tighter compared to overshoot cases according to Table IV. Overall, the response time constraint describes the correlation between the size of decoupling capacitor, the required speed of the digital control system and the output performance. It can be applied to every regulator design that utilizes digital control circuits. It provides the guideline for designing the digital control system and should be carefully considered.

C. Simulation Results

The design uses UMC 65-nm standard CMOS technology with only normal threshold voltage devices. The nominal supply voltage is 1.1 V. The performance of the implemented regulator is examined based on the response time constraint in Table IV.

Waveforms of post-layout simulation are shown in Fig. 7. The size of the decoupling capacitor is 3 nF. Fig. 7(a) illustrates output mode changing of the regulator with zero load. The simulated step responses of the regulated voltage with full load are shown in Fig. 7(b). The rise and fall time of the load current are both 100 ps.

Ideally the regulated voltage should settle at the desired output after the first undershoot. However, multiple overshoots and undershoots can be observed in Fig. 7(b). It is because the push current is designed to be a little larger since the equality to the maximum load current cannot be guaranteed under variations. The decoupling capacitor will be charged over the desired voltage level even in the presence of the load current and then activates another discharge operation. It can also be observed from the figure that charging with no load creates the largest overshoot whereas discharging with full load causes the largest undershoot. It is consistent with the analysis in Section II-B. Overall, the average of the regulated voltage is almost equal to the desired output voltage level.

The DED after layout has a 600 ps trigger period, i.e., the DED detection time T_{V2D} is 0.6 ns. The propagation delay T_D from the decision of the DED to the control of the push/pull devices is about 0.45 ns. Therefore the total response time of the proposed digital controlled voltage regulator in 65-nm technology is 1.05 ns. According to Table IV, the response time of designed circuit only meets the constraint of 0.5 V output (for undershoot case) with 3 nF decoupling capacitor. It is very close to the constraint of 0.6 V output and fails to meet those of all the other outputs. If the size of decoupling capacitor is 4.5 nF, all the response time constraints are satisfied. On the other hand, all the constraints are violated if the size of decoupling capacitor is 1.5 nF.

TABLE V
PERFORMANCE COMPARISON FOR DIFFERENT CONFIGURATIONS (mV)

undershoot (mV)		V_{OUT}					
		1.0V	0.9V	0.8V	0.7V	0.6V	0.5V
Decap. Size	1.5nF	110	114	115	114	80.0	81.1
	3nF	55.8	59.9	60.8	59.4	61.2	45.0
	4.5nF	43.6	44.7	43.1	41.4	43.4	34.3

The minimum error in stable state is 4 mV at 0.5 V output whereas the maximum error is 8.6 mV at 1 V output. The error comes from the resolution of DED. The larger error of 1 V output is a result of voltage divider as well as the voltage averaging effect of DED. The control system consumes an instant maximum of 470 μA as a nature of digital circuits. But in average, the quiescent current is 124 μA.

Table V lists the simulated voltage ripples for different configurations. Only undershoot results are listed since the undershoot constraints are much tighter than overshoot constraints. Note that the response time of the designed regulator is 1.05 ns in 65-nm technology. The voltage undershoots when using 3 nF decoupling capacitor meet the 50 mV ripple requirement if the response time constraints in Table IV are met, otherwise the specification is violated. The specification is well exceeded in the case with 1.5 nF decoupling capacitor since all the constraints are far from being satisfied. On the other hand, the voltage undershoots with 4 nF decoupling capacitor are all below the required 50 mV as a result of relaxed response time constraints.

D. Time Interleaving Control

From the discussion of previous section, the designed digital controlled voltage regulator in 65-nm technology violates the response time constraint for 1.5 and 3 nF decoupling capacitor cases. Increasing the size of the decoupling capacitor is a straightforward solution since it directly relaxes the response time constraint according to Table IV. However, the increased area and gate leakage overhead when integrating decoupling capacitor on-chip are not always acceptable. Therefore, a time interleaving control technique to instead reduce the effectively response time of the digital control system is proposed.

The idea is to make copies of DED as Fig. 8 depicts. The control system interleaved uses the results of different DEDs to control the push/pull devices. The task is achieved with the MUX-based control switch block as in the figure. The duplicated DEDs are triggered by the first DED with a certain delay to make sure that the interleaving period is stable and synchronized without racing issue. The delay is designed to equally divide the original DED detection time. For example, original

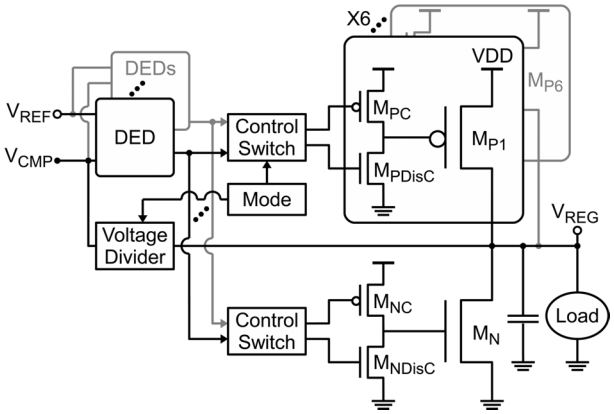


Fig. 8. Block diagram of the proposed time interleaving digital controlled linear regulator.

DED detection time is 600 ps. If three DEDs are used, the delays of the trigger signals are 200 and 400 ps for the second and third DEDs, respectively. Therefore, the effective DED detection time T_{V2D} can be reduced by using DED duplications.

A dual control type is first examined. The effective detection time is 0.3 ns as a result of two interleaved DED operations. The control signal propagation delay increases to 0.58 ns because of the extra logics for the control switch task. The total effective response time of the dual type control is therefore 0.88 ns. This enhanced response time meets more constraints according to Table IV.

Triple type control can also be designed. The effective response time should be around 0.78 ns $(0.6\,\text{ns}/3 + 0.58\,\text{ns})$. However, the inevitable 0.58 ns propagation delay when introducing the interleaving control has already exceeded the required constraints for smaller 1.5 nF decoupling capacitor. The benefit of using three DED blocks is not significant. Therefore, only the simulation results of dual control type are shown here.

When adopting dual type interleaving control, the quiescent current of the control system increases to an average of 375 μA. The duplicated DED and added control switch logics contribute to the increase. Table VI lists the simulated results of dual type control along with previous single type results. These are obtained from step response simulations similar to Fig. 7(b). All the undershoots of 3 nF decoupling capacitor case are below the 50 mV criteria although the 0.88 ns response time of the dual type control is not sufficient for 1 and 0.9 V output according to Table IV. It is because the worst case described in the analysis may not be triggered in the simulation. The undershoot numbers of 1.5 nF case show the improvement despite that the 50 mV requirement is still violated. On the other hand, the results of 4.5 nF case exhibit a significant reduction. The undershoots are even less than a half of the required value. Overall, the proposed interleaving control technique does improve the regulator performance.

III. Digital Control System Accuracy Under PVT Variations

Unlike the correlated operation of error amplifiers and output devices in analog regulators, the DED in the proposed digital voltage regulator is stand alone. It will not be affected by following logics or output devices. The accuracy of the regulated output voltage relies entirely on the DED. Therefore, the accuracy of the digital control system, especially the DED, in the presence of process, voltage, and temperature (PVT) variations is evaluated in this section.

TABLE VI
Time Interleaving Control Performance Comparison (mV)

undershoot (mV)		V_{OUT}					
		1.0V	0.9V	0.8V	0.7V	0.6V	0.5V
1.5nF	single	110	114	115	114	80.0	81.1
	dual	53.2	60.3	65.7	78.7	82.4	63.8
3nF	single	55.8	59.9	60.8	59.4	61.2	45.0
	dual	31.2	25.9	30.8	33.3	35.0	38.6
4.5nF	single	43.6	44.7	43.1	41.4	43.4	34.3
	dual	9.8	14.0	18.5	18.5	19.5	23.8

The differential structure of the proposed DED is similar to the silicon odometer presented in [22]. The author of [22] suggested that the differential structure will cancel out the common-mode PVT variations. However, the digital error detection technique relies on absolute delay difference of two delay lines instead of the relative property as in [22]. This absolute delay difference and the delay of a single inverter together decide the resolution of the DED as described in Section II-A. These properties as well as the resistive voltage divider are still affected by PVT variations.

Process variation Monte Carlo analysis with 10 000 iterations is first performed. The delay difference of two delay lines (denoted as Δdelay) and the resolution (represented by single inverter delay) of the DED are reported. The supply and temperature conditions are fixed at normal 1.1 V and 25 °C, respectively. The measured delay results are rounded to 0.1 ps.

The detection of voltage error by DED requires that Δdelay exceeds DED's resolution. In normal condition the design has a 5 mV resolution. Therefore, the Δdelay of DED under process variation is first evaluated at 5 mV deviation of comparison voltage from the reference voltage. The results are shown in Fig. 9(a). Both Δdelay and inverter delay distributions show an approximate to the normal distribution. The mean values (μ) of Δdelay and inverter delay are 11.40 and 10.29 ps, respectively. It is consistent with that Δdelay exceeds a single inverter delay at 5 mV deviation in normal condition. The coefficient of variation (σ/μ) of Δdelay is larger than that of inverter delay since delay lines are more complicated. Δdelay is therefore not guaranteed to be larger than a single inverter delay at 5 mV deviation under process variation. In other words, the resolution of DED is affected by the process variation.

The promising resolution is the voltage deviation where Δdelay is ensured to exceed a single inverter delay under process variation. The distributions of Δdelay and inverter delay should not overlap each other, i.e., the left 3-σ of Δdelay distribution should be larger than the right 3-σ of inverter delay distribution. Assuming that the coefficient of variation remains the same, the mean value of Δdelay should be larger than 16.88 ps to meet the requirement.

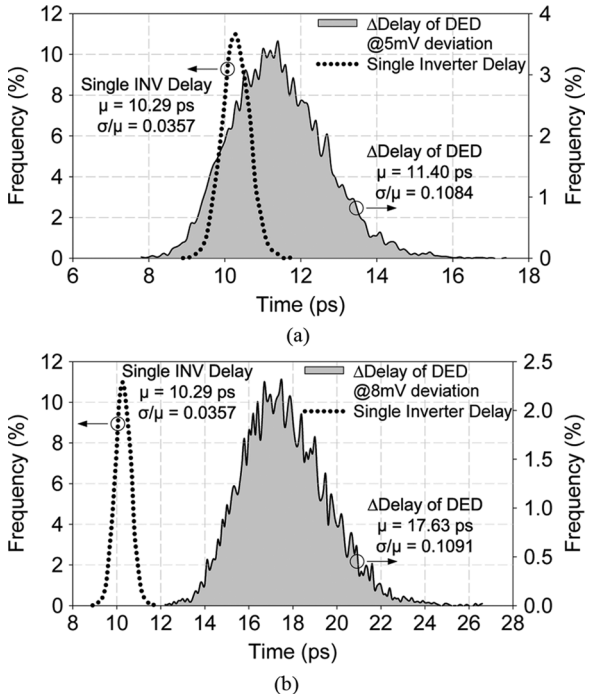


Fig. 9. Monte Carlo analysis of $\Delta\mathrm{delay}$ and resolution (single inverter delay) of DED under process variation (a) at 5 mV deviation and (b) at 8 mV deviation.

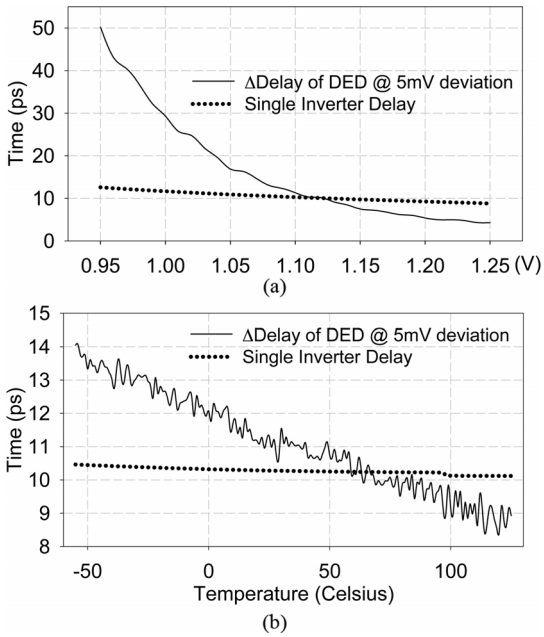


Fig. 10. $\Delta\mathrm{delay}$ and resolution (single inverter delay) of DED (a) under supply voltage variation and (b) under temperature variation.

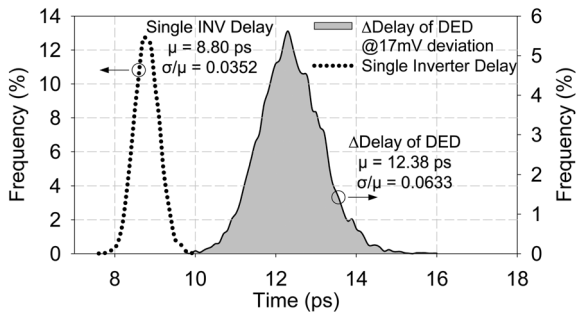


Fig. 11. Worst case Monte Carlo analysis of $\Delta\mathrm{delay}$ and resolution (single inverter delay) of DED at 1.25 V/125 °C.

This property can be achieved when the comparison voltage has an 8 mV deviation from the reference voltage. As shown in Fig. 9(b), the mean of the $\Delta\mathrm{delay}$ distribution is 17.63 ps when the voltage deviation is 8 mV. The coefficient of variation is 0.1091 that is approximately equal to that of 5 mV deviation case. It can be observed from the figure that the distributions of $\Delta\mathrm{delay}$ and inverter delay are separated with no overlap. Therefore, it can be summarized that the resolution of DED is degraded to 8 mV by the process variation.

The $\Delta\mathrm{delay}$ and inverter delay are also evaluated under supply voltage and temperature variations. The normal conditions are TT corner, 1.1 V and 25 °C. Only one of voltage and temperature is treated as a variation variable at a time. Both figures in Fig. 10 report that $\Delta\mathrm{delay}$ exceeds a single inverter delay at 1.1 V/25 °C normal condition. But the DED fails to hold this property at 5 mV deviation as voltage and temperature increase. It means that the resolution of DED is also worsened by voltage and temperature variations. Although the trend of $\Delta\mathrm{delay}$ shows a decrease as temperature increases, the results are not monotonic decreasing. This may result from the imperfection of the transistor model card provided by the foundry. Similar to the analysis for process variation, the resolution is degraded to 12 mV by worst voltage variation. When considering only temperature variation, the resolution is degraded to 7 mV.

It can be summarized from the analyses above that the supply voltage variation has the most effect on the DED accuracy. It degrades the resolution from 5 to 12 mV. The process and temperature variations have less effect since the resolution is degraded by only a few mV.

A worst case scenario Monte Carlo analysis is also performed at 1.25 V/125 °C. Note that the highest supply voltage is used since it worsens the resolution as shown in Fig. 10(a). Fig. 11 shows the distributions of $\Delta\mathrm{delay}$ and inverter delay at 17 mV deviation. The mean values are both reduced because of high supply voltage. The coefficients of variation are also reduced suggesting that the variations of $\Delta\mathrm{delay}$ and inverter delay are smaller in the worst case scenario. The distributions of $\Delta\mathrm{delay}$ and inverter delay are not overlapping. Therefore, the resolution of DED is degraded to 17 mV at worst case. It is approximately the sum of degradations induced by each variation.

The variation of the voltage divider will also produce error of the regulated voltage. Fig. 12 presents the Monte Carlo analysis about dividing ratios under process variations. Distributions of each dividing ratio are shown in the figure with μ and σ/μ results attached. The dividing ratio variations induced by process variation are quite small. For example, there is less than 1% error even at the 3-σ point of 1/2 ratio which has the largest variation. Meanwhile, the dividing ratios show almost no change for voltage and temperature variations. Overall, it can be considered that the voltage divider is resistant to PVT variations since it is a passive element.

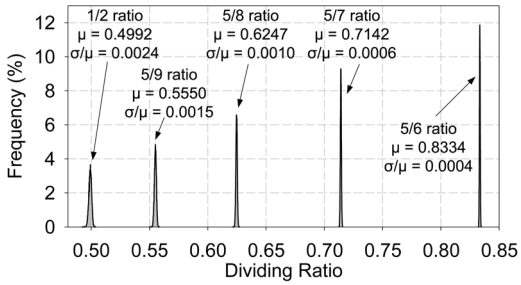


Fig. 12. Monte Carlo analysis of voltage divider's dividing ratios under process variation.

TABLE VII
RESPONSE TIME CONSTRAINTS FOR DIFFERENT TECHNOLOGIES

	$T_{R,undershoot}$ for V_{OUT}=0.8V (ns)				
Decap. Size	1nF	1.5nF	3nF	4.5nF	6nF
UMC 90nm	-	0.478	0.957	1.435	1.913
UMC 65nm	-	0.464	0.927	1.391	-
PTM 45nm	0.309	0.453	0.906	1.359	-
PTM 32nm	0.308	0.451	0.902	1.353	-

The largest error in stable state should occur at 1 V output since it is divided by two before being fed to DED. According to the variation analysis, the resolution of DED is degraded to 17 mV at worst case and the variation of voltage divider is so small that can be ignored. Therefore, the largest error of 1 V output is estimated to be 34 mV and is about 3.4% output error in stable state.

IV. TECHNOLOGY MIGRATION DEMONSTRATION

One of the major advantages of digital circuits is the easiness to migrate between different technology nodes. The proposed digital controlled voltage regulator possesses the same technology migration advantage since it is built from purely digital behavior circuits except the passive voltage divider. Furthermore, the proposed regulator is more beneficial from technology advancing because of the performance gain. The response time constraint discussed in Section II-B are easier to be met by faster circuits in more advanced technology even with low cost small decoupling capacitor.

The migration of the proposed digital controlled voltage regulator only takes a few steps. First, simple logic gates such as INV/NAND/NOR gates that compose most of the control system are constructed for the target technology node. Then the voltage controlled delay cell of DED requires a slight tuning for proper delay versus voltage relationship. Finally, the output devices as well as the drivers are resized to provide the target load current and the migration task is completed.

Table VII lists the theoretic response time constraint numbers with respect to technology nodes and decoupling capacitors. Four technologies are used including UMC 90- and 65-nm standard CMOS technology and Predictive Technology Model (PTM) 45- and 32-nm high-k/metal gate models [23]. Note that the constraint of undershoot for higher output is tighter and the supply voltage suggested by PTM 32-nm model is 0.9 V. So the 0.8 V output case is chosen for comparison. Several cells in the table are leaved blank since those constraints are never (90-/65-nm@1 nF) or always (65-/45-/32-nm@6 nF) met. The theoretic constraints from (12) show little changing for technology nodes.

TABLE VIII
IMPLEMENTED CIRCUIT RESPONSE TIME OF DIFFERENT TECHNOLOGIES

	UMC 90nm (post-layout)	UMC 65nm (post-layout)	PTM 45nm (pre-layout)	PTM 32nm (pre-layout)
T_{V2D}	1.01ns	0.6ns	0.132ns	0.15ns
T_D	0.58ns	0.45ns	0.15ns	0.12ns
T_R	1.59ns	1.05ns	0.282ns	0.27ns

TABLE IX
PERFORMANCE COMPARISON OF DIFFERENT TECHNOLOGIES

	undershoot at V_{OUT}=0.8V (mV)					Quiescent Current
Decap. Size	1nF	1.5nF	3nF	4.5nF	6nF	(μA)
UMC 90nm	-	-	98.7	60.5	49.8	162
UMC 65nm	-	114.8	60.8	43.1	-	124
PTM 45nm	53.1	41.2	21.8	-	-	113
PTM 32nm	58.8	40	24.4	-	-	38

On the other hand, the response time results of implemented circuit in different technology nodes are shown in Table VIII. Note that the results of UMC 90- and 65-nm are post-layout simulation results. It can be observed in the table that both the DED detection time T_{V2D} and control signal propagation delay T_D decrease as technology advances except T_{V2D} of PTM 32-nm model. The decreasing of the response time is a result of faster circuit speed of advanced technology. For the PTM 32-nm model, the gate-source voltage of MP_C of the voltage controlled delay cell in Fig. 4(a) is only 0.4 V. It is less than the threshold voltage of p-type transistor. Therefore, the delay cell operates much slower in 32-nm model than in other technologies that increases the DED detection time.

It can be observed from Tables VII and VIII that the circuit response time of 90-nm node meets constraint of 6 nF decoupling capacitor case. The response time of 65-nm node meets constraint of 4.5 nF decoupling capacitor case. Both PTM 45- and 32-nm node circuits just meet the constraints even with only 1 nF decoupling capacitor. The simulated undershoot results at 0.8 V output for technology nodes are listed in Table IX. The average quiescent current values are also presented. Some cells are leaved blank because it is unnecessary to simulate those cases.

The undershoot results shown in Table IX are consistent with the satisfaction of the response time constraint except 45- and 32-nm at 1 nF decoupling cases. Advanced technology provides better performance under the same size of decoupling capacitor. In other words, smaller decoupling capacitor is needed for the same voltage overshoot/undershoot specification. Moreover, the quiescent current is also reduced in advanced technology. Therefore, the proposed digital controlled voltage regulator benefits from technology advancing in terms of integration cost, regulated voltage ripple and current efficiency.

Note that circuits using PTM 45- and 32-nm models have comparable performance since they have similar response time. Their undershoot results with 1 nF decoupling capacitor exceed

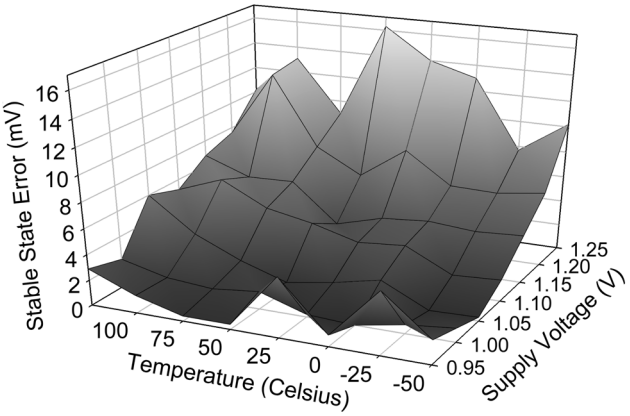


Fig. 13. Output voltage error in 0.5 V stable states versus supply voltage across temperature.

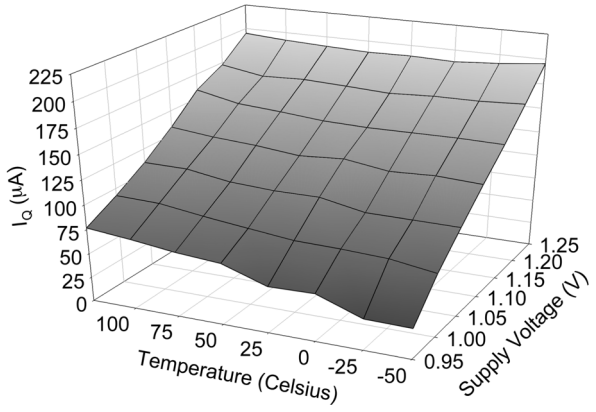


Fig. 14. Quiescent current versus supply voltage across temperature.

50 mV. It is because the migrations of the voltage controlled delay cell to these technology nodes are not optimized for their operation regions. The delay and control voltage relationship of the delay cell should be taken good care of to have better performance. Nevertheless, it is still a minor effort in the simple migration procedure because of its simple structure.

V. Experimental Results

The proposed digital controlled voltage regulator has been implemented with UMC 65-nm standard CMOS technology. Fig. 13 shows the post-layout simulation results of output voltage error in 0.5 V stable states versus supply voltage at different temperatures. Note that the error is not a fixed value in every supply voltage/temperature combination. It may vary in different operation times. However, a trend can still be observed from the figure that the stable state error increases along with supply voltage and temperature. It is consistent with the analysis in Section III that increased supply voltage and temperature both degrade the resolution of DED. The analysis also reveals that the degradation of DED's resolution by supply voltage is larger than that by temperature. Hence, the dependence of the error on supply voltage is much larger than that on temperature as shown in the figure.

The change of the quiescent current versus supply voltage and temperature is shown in Fig. 14. It agrees with the general knowledge that the circuit power increases with supply voltage and temperature. At the largest supply voltage and temperature, the quiescent current increases from 124 μA to about 200 μA.

The layout view of the test chip is shown in Fig. 15(a) along with the chip photo after wire bonding in Fig. 15(b). Basic single control and time interleaving dual control types are both implemented in the test chip that share the same set of output devices to save the chip area. The total area of the test chip is 1158×942 μm^2. The I/O PADs and the metal lines to follow the current density rules contribute to most of the chip area.

The layout view of the single control part of proposed regulator is shown in Fig. 16. The layout area of the output buffers and drivers is 120×7.5 μm^2. Note that the size of the output buffers and drivers is proportional to the output devices. The voltage divider occupies 61×2 μm^2 that has a resistance value of 27 kΩ to reduce the power consumption. The increased area

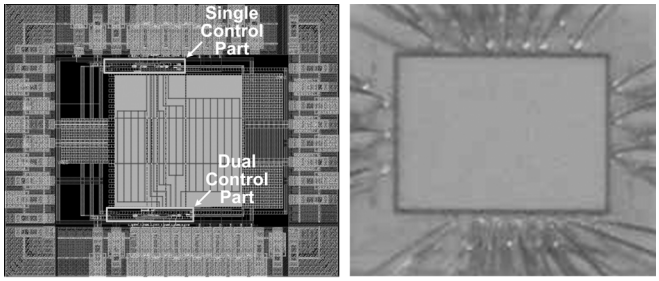


Fig. 15. (a) Layout view of the full test chip and (b) chip photo after wire bonding.

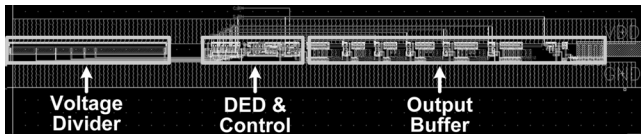


Fig. 16. Layout view of single control part.

also reduces the effect of the PVT variation. The main body of the proposed digital regulator including the DED and the control logics only occupies about 35×5 μm^2 chip area. It is approximately equal to 150 INV cells of UMC 65-nm cell library in a two-row arrangement. Note that the total area can be further compressed since there are spaces reserved for routing convenience.

Table X lists the measured quiescent currents and standby leakage currents of four TT corner and five FF corner test chips. The standby leakage current is measured when all the control circuits are deactivated. Note that in the implementation the circuits of both control types share the same power supply. Consequently, the measured quiescent current of single control type contains the standby current of dual control type and vice versa. The actual quiescent current of each type should be 10 to 20 μA less than that reported in Table X. However, the results reported in the table are used in the following presentation because the precise value of standby current cannot be determined and subtracted.

From Table X, the standby leakages of FF corner chips are larger than those of TT corner chips as expected. The average quiescent currents of the single control type are 164.5 μA for

TABLE X
MEASURED QUIESCENT CURRENT OF TEST CHIPS (μA)

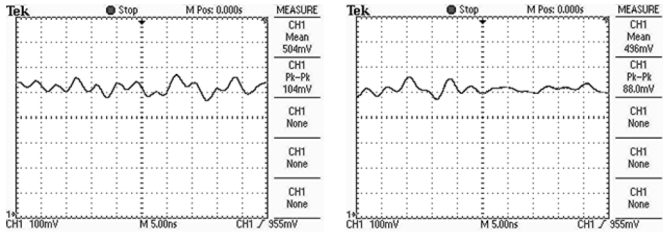
		Single (μA)	Dual (μA)	Standby Leakage (μA)
TT	Chip #1	145	361	32
	Chip #2	165	440	32
	Chip #3	176	410	36
	Chip #4	172	442	42
	Average	164.5	413.25	35.5
FF	Chip #1	206	481	68
	Chip #2	165	452	46
	Chip #3	178	466	50
	Chip #4	172	440	50
	Chip #5	217	497	78
	Average	187.6	467.4	58.4

TT corner and 187.6 μA for FF corner. The quiescent currents of the dual control type are 413.25 and 467.4 μA for TT and FF corners, respectively. The measurement results are consistent with the analysis in Section II-D that the duplicated DED and extra switch logics increase the quiescent current.

The DED detection time (T_{V2D}), i.e., the DED trigger period, of the implemented chip is measured to be 0.75 ns. The measured detection time is slightly larger than the result of post-layout simulation. It is reasonable to speculate that the control signal propagation delay (T_D) is also larger after fabrication. As a result, the (effective) response times of two control types are both expected to exceed the response time constraint of 3 nF decoupling capacitor according to Table IV. Therefore, 4.5 nF is used for the chip measurement.

Fig. 17 shows the measured output transient response at 0.5 V output with full load current. Only full load current condition results are presented because of the limitation of the measuring instruments. But it should be note that the output (push/pull) devices of this work are controlled digitally. There is no intermediate gate biasing as in conventional analog regulators but only on and off states. When both push and pull devices are off, it is similar to step load test condition. Therefore, the output transient response at full load can cover the load step test condition. It also covers the worst case undershoot condition as exhibited in Fig. 6. The transient response of single control type is shown in Fig. 17(a) whereas that of dual control type is shown in Fig. 17(b). The average values of the regulated voltage are both around 0.5 V with error of only several mV. It can be observed in the figures that the fluctuation of regulated output is smaller when using dual control type. The peak-to-peak amplitudes of the regulated output are 104 and 88 mV for single and dual control type, respectively.

Fig. 18 provides more measurement results of the regulator. These are the results of the single control type at full load current for 0.6-1.0 V output. The mean values have errors of 3 to 15 mV. Larger error of mean value is measured for higher output level as a result of voltage divider. The same phenomenon can be observed for the voltage fluctuation results. The supply voltage is changed with 10% variation to observe line regulation property. However, the error is still within 20 mV. It cannot be distinguished from the detection error of DED. There is no observable load regulation for the designed regulator since the output



(a) (b)

Fig. 17. Measured output transient response at full load current at 0.5 V output (a) with single control type and (b) with dual control type.

TABLE XI
PERFORMANCE COMPARISON OF VOLTAGE REGULATORS

	[12] 2005	[14] 2007	[9] 2009	[15] 2010	This work
Technology	90nm	90nm	0.13μm	65nm	65nm
V_{IN}	1.2V	2.4V	1.15V	0.5V	1.1V
V_{OUT}	0.9V	1.2V	1V	0.45V	0.5-1V
I_{OUT}	100mA	1A	25mA	200μA	100mA
ΔV_{OUT}	90mV	120mV	15mV	40mV	120mV
I_Q	6mA	25.7mA	50μA	2.7μA	164.5μA
C_{decap}	0.6nF	2.4nF	4μF	100nF	4.5nF
Current Efficiency	94.3%	97.5%	99.8%	98.7%	99.8%
FOM (pA·s)	4.32	14.8	138	60	0.98
Implementation	analog	digital	analog	digital	digital

devices are decoupled from the control system and the DED. The magnitude of load current will not affect the accuracy of the control system as opposed to conventional analog regulator.

The comparison of the proposed regulator to previous works is presented in Table XI. The results of single control type with 4.5 nF decoupling capacitor at 1 V output are used for comparison in the table. Two of these works aimed for integration with small decoupling capacitor [12], [14]. One is targeting for minimum output ripple with large off-chip capacitor [9]. The last one is a digital implementation with large off-chip capacitor [15]. The quiescent current of the proposed work is much lower than [12], [14] and is comparable with [9]. The 99.8% current efficiency is the highest among these works.

Different regulators can be compared by following figure of merit:

$$\mathrm{FOM} = \frac{C_{\mathrm{decap}} \times \Delta V_{\mathrm{OUT}}}{I_{\mathrm{OUT}}} \times \frac{V_{\mathrm{IN}}}{V_{\mathrm{OUT}}} \times I_Q \qquad (13)$$

where C_{decap} is the decoupling capacitor, ΔV_{OUT} is the output ripple, I_{OUT} is the maximum load current, V_{IN} is the input voltage, V_{OUT} is the output voltage, and I_Q is the quiescent current.

The proposed digital controlled voltage regulator achieves the best (lowest) FOM of 0.98 pA·s for 1 V output. For the dual control type of proposed interleaving control with 4.5 nF decoupling capacitor, the resulting FOM is 1.84 pA·s with 99.6% current efficiency. Small decoupling capacitor, large load current, small dropout voltage, and small quiescent current of this work contribute to the lowest FOM as shown in Table XI. Note that although the work in [15] had a very low quiescent current, it does not have a good FOM evaluation because of relatively large

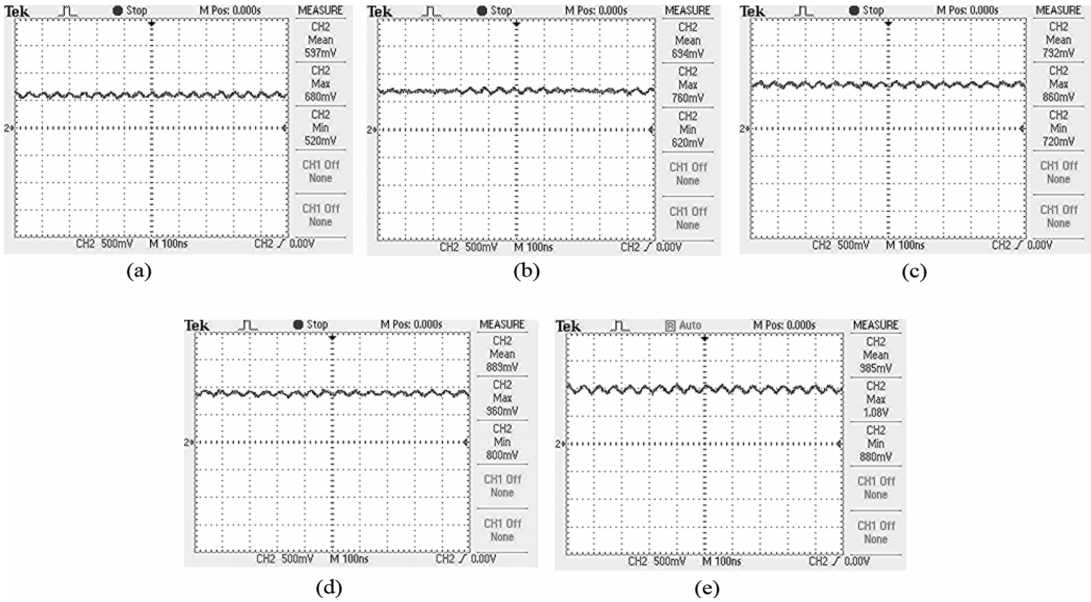


Fig. 18. Measured output transient response of single control type at full load current: (a) at 0.6 V output; (b) at 0.7 V output; (c) at 0.8 V output; (d) at 0.9 V output; and (e) at 1.0 V output.

decoupling capacitor. Besides, the low quiescent current is a result of low switching frequency (1 MHz) under ultra light load condition. If the load current is to be increased, the switching frequency must be increased to respond faster. Then the quiescent current will be increased as clearly shown in [15].

In the presented work, push-pull topology is adopted. Based on the experimental results, the overshoots are around 30 to 100 mV above the target level. Note that the overshoot is irrelevant to the existence of the pull device M_N. Therefore, the pull device is not a necessity if the load circuits can endure a little supply overdrive. Meanwhile, the reported quiescent current (as well as the current efficiency) is calculated under stable state of the regulator as mentioned. Counting in the current pulled away by pull device M_N can degrade the efficiency. But on the other hand, if the pull device is removed as discussed, the efficiency will be even higher than reported because the associated control circuits of M_N are also removed.

The experimental results and the developed response time constraint in this work suggest a wide range of application of the proposed digital controlled voltage regulator. The design parameters of a power supply include the maximum load current, the size of the decoupling capacitor, the output ripple performance, and the quiescent current of the power supply. These parameters are mutual related and the tradeoff is represented by the response time constraint developed in Section II-B.

The proposed digital controlled voltage regulator can be easily configured to have different tradeoffs of these parameters. If smaller output ripple is required, interleaving control technique can be used when the target load current is large. The increased quiescent current will not overdegrade the current efficiency. Otherwise, the size of the decoupling capacitor can be increased at a cost of increasing area. On the other hand, the internal ring oscillator can be modified such that it can adaptively lower the frequency for light load conditions. It can reduce the quiescent current. The internal ring oscillator can even be removed such that the DED is triggered by external slow clock signal in ultra light load conditions. Overall, the presented work has benefits and flexibilities that are contributed by its nature of all digital implementation.

VI. Conclusion

A fully digital controlled voltage regulator is presented. Super- to near-threshold region operation is supported by providing a variable regulated output ranging from 0.5 to 1 V in steps of 0.1 V. The work consists of a digital error detector, a voltage divider, a mode indicator, a pull device and grouped push devices with their own drivers. The maximum load current is designed (but not limited) to be 100 mA for every output voltage. The measurement of the testchips fabricated on UMC 65-nm standard CMOS technology reports a current efficiency of 99.8% with only 164.5 μA quiescent current. A time interleaving control technique is proposed as well to enhance the output performance at the cost of increased quiescent current. The area occupied by the digital control system of the regulator is only about 300 μm^2. A response time constraint that is specific to (all) the digital control system is also presented. It provides the design guideline for required speed of the control system and the size of the decoupling capacitor.

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