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A 250 MHz low voltage low-pass G_m-C filter

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Abstract A high speed and high linearity G_m-C low-pass filter is presented. The proposed OTA is designed under low power supply voltage consideration while its gain, excess phase, and linearity are well maintained. The common-mode control system, including common-mode feedback and common-mode feedforward circuits, is added to ensure stability of the proposed filter. Measurement results show that the inter-modulation distortion of −40 dB can be achieved with 250 MHz 400 mV_{pp} balanced differential input signals. The filter works in 1 − V supply voltage and its power consumption is 32 mW.

Keywords Operational transconductance amplifier (OTA) · Filter · Ultra-wide band system

1 Introduction

As there is a great demand for lighter hand-held mobile phones and longer battery lifetime, low-voltage integrated circuit design solutions must be developed. Traditionally in CMOS technology, the baseband filters are realized with switched-capacitor (SC) techniques, but the SC filters are limited to low speed applications due to the sampling procedure and the high power requirement of the OPAMP. On the other hand, continuous-time G_m-C filter realizations can be easily implemented for the high speed applications and tend to be less power consuming. Furthermore, the filters do not require extra processing steps compared with Active-RC structures, and their frequency tuning can be easily achieved. Thus, the G_m-C filter appears to be a better candidate for the UWB wireless application, which uses pulse signals at a high speed.

For G_m-C filter implementation, the high performance operational transconductance amplifier (OTA) would be the most important building block [1–4]. In the design of OTAs, the transconductance should be tuned for compensation for process tolerances and temperature variations without degrading the entire circuit performance. Besides, low power supply voltage implementation should be adopted for the trend of a system-on-a-chip strategy. The performance of digital circuits does not degrade when using lower power supply voltage. On the other hand, for analog circuits, the circuit performance is strongly affected by the low power supply voltage. The linearity performance of the OTA will become worse at low supply voltage, so novel OTA circuit design should be investigated.

In this article, the design of a high speed, low distortion and low supply voltage G_m-C filter for UWB wireless application is presented. The structure of the high linearity OTA with the pseudo-differential pair is discussed in Sect. 2. The common-mode control system with guaranteed stability is shown in Sect. 3. In Sect. 4, the design of fourth-order equiripple linear phase low-pass filter and the measurement results are discussed. Some final conclusions are presented in Sect. 5.

2 Proposed OTA

To design a high performance OTA, the concept of voltage attenuation is taken in our circuit. Figure 1 shows the block

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diagram of the technique. The factor ζ is smaller than 1. We can see that the input voltage is attenuated by the value ζ and the output current is given by

$$io = a_1(\zeta v_i) + a_2(\zeta v_i)^2 + a_3(\zeta v_i)^3 \quad (1)$$

We can prove that the third-order harmonic distortion term (HD3) gets a value of ζ^2 smaller than the original one. The natural attenuation could be obtained from the designed capacitor ratio, and thus the multiple input floating-gate (MIFG) technique can be a good approach [5, 6]. However, large capacitors limit the operation speed and technique requires extra fabrication processes. In this article, the high speed OTA, which operates under the concept of voltage attenuation to achieve high linearity in standard CMOS process, is presented.

A pseudo-differential structure [7–9] is also used in our circuit for low voltage operation. The absence of the tail current source allows lower power supply voltage and higher signal swing ranges. For large device length, the pseudo-differential pair with the source terminals connected to ground obtains more linear performance in contrast with the fully-differential architecture. However, in the technology down to smaller feature sizes, the short channel effect occurs owing to the fact that the effective carrier mobility is a function of both the longitudinal and transversal electric fields, and thus the short channel effect and channel length modulation will degrade the linearity of the pseudo-differential structure.

Figure 2 shows the proposed OTA circuit. Resistor R_{tune} is connected between current mirrors M3 and M4. By using the resistor, we can obtain a voltage attenuation factor of $\zeta = gm_{(1,2)} \times R_{tune}/(2 + gm_{(3,4)} \times R_{tune})$ from the gate terminal to the drain terminal of transistors M1 and M2, where $1/gm_{(3,4)}$ is the output impedance of diode-connected transistors. If we have a small value of $gm_{(3,4)} \times R_{tune}$, a high attenuation factor can be achieved. In order to obtain the linearity performance, we adopt the usual mobility equation $\mu_{n,p} = \mu_0/(1 + \theta V_{ov})$, where μ_0 is low-field mobility, θ is the mobility reduction coefficient, and V_{ov} is the MOS over-drive voltage. By taking the output current equation into a Taylor series expansion, the third-order harmonic distortion component of the OTA is given by

$$HD_3 \cong \frac{\theta}{16V_{ov(1,2)}\left(1+\theta V_{ov(1,2)}\sqrt{\frac{BK_{(3,4)}}{K_{(1,2)}}}\right)^2\left(2+\theta V_{ov(1,2)}\sqrt{\frac{BK_{(3,4)}}{K_{(1,2)}}}\right)\sqrt{\frac{K_{(1,2)}}{BK_{(3,4)}}}\left(\frac{K_{(1,2)}}{K_{(3,4)}}\zeta V_p\right)^2} \quad (2)$$

where K_i is the device parameter of transistor M_i, V_p is the peak voltage of a sinusoid input signal, and B is the current mirror ratio of M3–M5 and M4–M6.

The gain performance of the OTA should be maintained as well. Usually, the gain of larger than 30 dB is sufficient for low Q low-pass filter design for correct signal transformation [10], and it could be maintained by designing a small aspect ratio of load transistors. Unfortunately, the use of R_{tune} would highly degrade the overall gain. Cascode circuit could be a possible solution, but it would not suitable for the low voltage design.

By taking the gain performance into consideration, the modified OTA circuit is shown in Fig. 3. Transistor M11 has the same size as transistors M1 and M2, and thus it has the same drain current by giving the same input common-mode voltage at the gate terminal. Transistors M9 and M10, which work in the saturation region with α times aspect ratio with respect to M12, are utilized to share part of DC drain current from M1 and M2. The increased gain would be expressed as

$$A_{enhanced} = \left(\frac{2\sqrt{(1-\alpha)} + g_{m(3,4)}R_{tune}}{2 + g_{m(3,4)}R_{tune}}\right)\left(\frac{1}{1-\alpha}\right) \quad (3)$$

For example, if the value of α is 3/4, we can obtain that $1 - \alpha$ would be equal to 1/4, and thus an enhanced gain in the range of 2–4 can be achieved. We should note that the

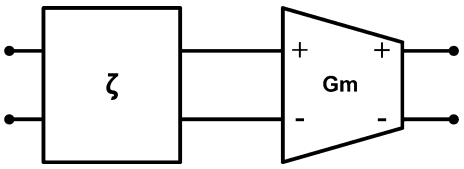

Fig. 1 Concept of voltage attenuation

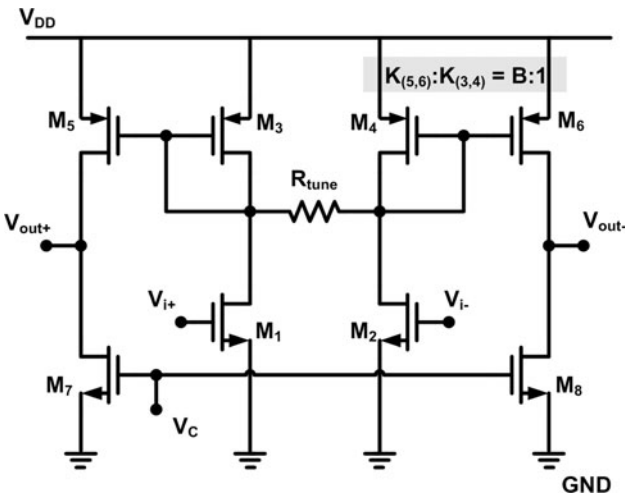

Fig. 2 Linearized low voltage OTA circuit

structure also increases the linearity performance because the value of $gm_{(3,4)}$ in Fig. 3 has a factor of $\sqrt{(1-\alpha)}$ then the value of $gm_{(3,4)}$ in Fig. 2, and thus a smaller value of ζ can be obtained. In other words, it could relax the required sizes of transistors M3 and M4, and the value of R_{tune}. Moreover, transistors M9 and M10 would not affect the linearity performance owing to their high output impedance Therefore, the OTA gain could be expressed as where C_X and C_L are the capacitance at nodes $V_{X(a,b)}$ and $V_{out(+/-)}$, respectively. The term λ accounts for the effect of channel length modulation. The non-dominant pole should be carefully designed for smaller excess phase so that the OTA can connect load capacitance C_L at the output to implement an integrator. The higher excess phase of the OTA will cause deviation to the −3 dB cutoff frequency of the resulting filter. We can see from (3) that the non-dominant pole would be affected by the value of α so as to contribute excess phase. Thus, the tradeoff among stability, gain, and linearity should be considered simultaneously.

$$A(s) = \sqrt{\frac{K_{(1,2)}K_{(3,4)}}{1-\alpha}}\left(\frac{R_{tune}}{2+\sqrt{K_{(1,2)}K_{(3,4)}(1-\alpha)}V_{ov(1,2)}R_{tune}}\right)\frac{1}{\lambda_{(5,6)}\left(1+s\frac{C_L}{2\lambda_{(5,6)}B(1-\alpha)K_{(1,2)}V_{ov(1,2)}^2}\right)} \quad (4)$$

$$\frac{1}{\left(1+s\frac{R_{tune}C_X}{2+\sqrt{K_{(1,2)}K_{(3,4)}(1-\alpha)}V_{ov(1,2)}R_{tune}}\right)}$$

3 The common-mode control system

The differential-output OTA requires proper common-mode control which not only stabilizes DC common-mode output voltage, but suppresses input common-mode signal at the output stage. For the fully-differential structure, the common-mode feedback (CMFB) circuit is used as a negative feedback loop that fixes the output common-mode voltage. The tail current source in the fully-differential structure would restrict the input common-mode signal from variation. For the pseudo-differential structure, the way of suppressing the input common-mode signal is to include a common-mode feedforward (CMFF) circuit. Figure 4 illustrates an efficient common-mode control system, which is implemented by the CMFF circuit combined with the CMFB circuit. The CMFF circuit is composed by transistors MFFP1, MFFP2, and MFFN. The resistor R_{tune} is replaced by two MOS transistors operating in the linear region, and thus the output common-mode voltage can be simply sensed by next OTA in the cascaded biquadratic structure. The value of R_{tune} is equal to $1/(K_{(r1)} \times V_{ov(r1)}) + 1/(K_{(r2)} \times V_{ov(r2)})$, where $V_{ov(r1,r2)}$ is equal to $V_{tune} - V_{X(a,b)} - Vt$ and depends on V_{tune}. We should design the transistor sizes that $K_{(5,6)} = K_{(FFP1,FFP2)}$, $2 \times K_{(7,8)} = K_{(FFN)}$, $K_{(1,2)} = K_{FBN}$, and $K_{(3,4)} = K_{FBP}$. In the figure, the CMFB loop is drawn in bold lines.

The CMFB circuit senses the output common-mode voltage from next OTA and produces corrected current to the CMFF circuit. Like in the previous discussion, the

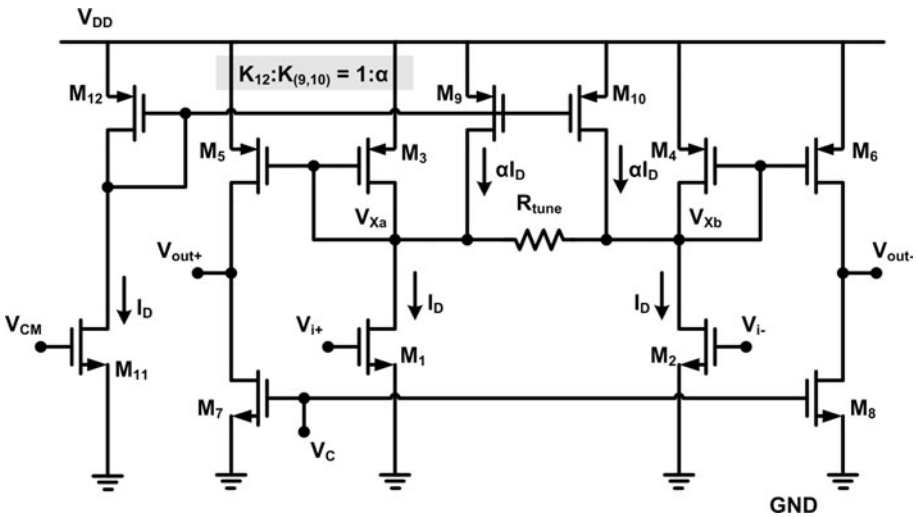

Fig. 3 Modified low voltage OTA circuit

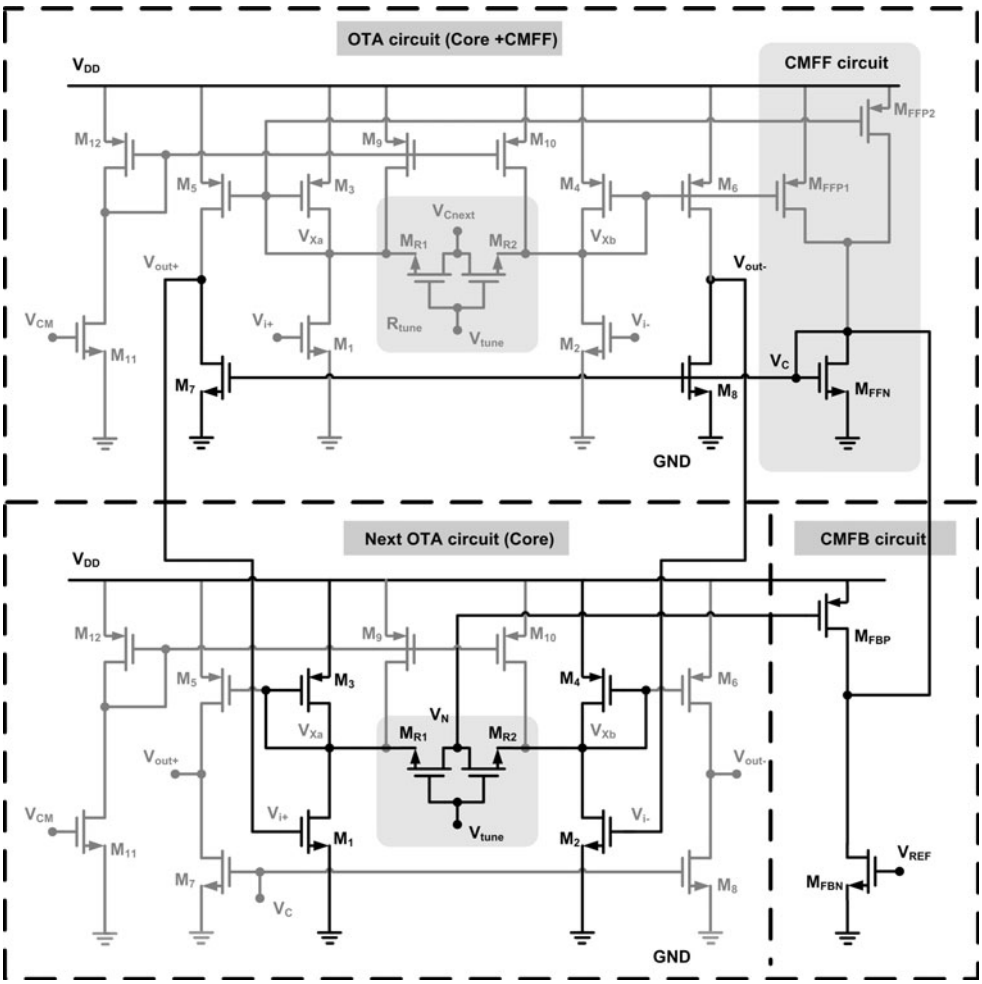

Fig. 4 The common-mode control system

common-mode control system is also designed under the consideration of high speed with stable phase margin. The open loop gain of the CMFB circuit is given by

$$A_{CMFB}(s) \approx g_{CMFB}(s)\frac{1}{(g_{o5,6}+g_{o7,8})} = \frac{g_{m(1,2)}}{(g_{o5,6}+g_{o7,8})} \frac{1}{\left(1+s\frac{R_{tune}C_N}{2}\right)\left(1+s\frac{C_C}{g_{mFFN}}\right)\left(1+s\frac{C_L}{g_{o5,6}+g_{o7,8}}\right)} \tag{5}$$

where C_C and C_N is the capacitance at nodes V_C and V_N, respectively. Again, the modified structure increases the gain of the CMFB as well. The dominant pole of the circuit is $(g_{o5,6} + g_{o7,8})/C_L$ and the non-dominant high frequency poles are at g_{mFFN}/C_C and $2/R_{tune} \times C_N$. It is necessary to ensure that the frequency of the non-dominate poles would be larger than the unity-gain bandwidth.

The CMFF circuit uses replica current mirror of M5 and M6. It senses the input common-mode signal from two terminals of the resistor and cancels the common-mode signal variation. For the common-mode control operation, the error value will be sent from the CMFB part as an adaptive bias signal and combined with the CMFF part for overall stability. The input common-mode gain in our design can be also calculated as

$$A_{cm}(s) \approx \frac{(g_{o5,6}+g_{o7,8})}{g_{CMFF}(s)+g_{CMFB}(s)} \text{ where } g_{CMFF}(s) = Bg_{m(1,2)} \times \frac{1}{\left(1+s\frac{BR_{tune}C_N}{2}\right)\left(1+s\frac{C_C}{g_{mFFN}}\right)\left(1+s\frac{C_L}{g_{o5,6}+g_{o7,8}}\right)} \tag{6}$$

The result of smaller than one can be obtained at low frequency owing to the large values of g_{CMFB} and g_{CMFF}, and thus a higher CMRR can be expected.

4 Filter implementation and measurement results

In the integrator design, the unity-gain frequency would be an important factor for future filter synthesis. The unity-gain frequency is dependent on the transconductance and the loading capacitor. Adjustable transconductor or capacitor is

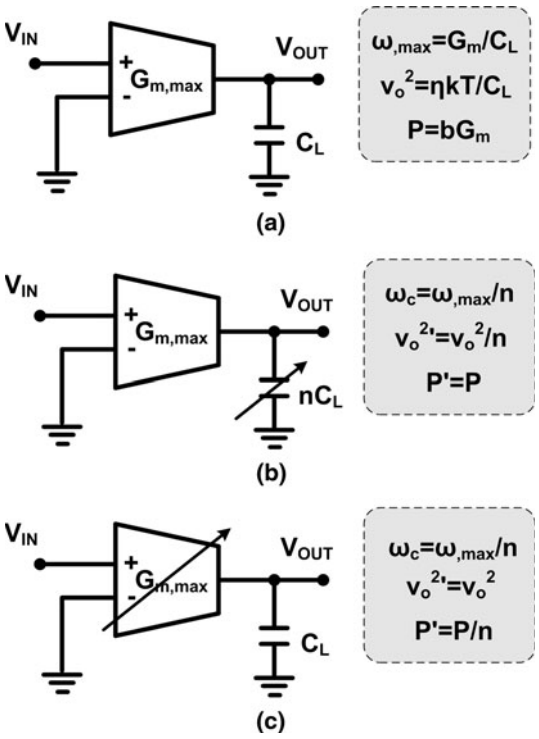

Fig. 5 Integrators: **a** integrator with maximum unity-gain frequency, **b** integrator with constant-Gm design, **c** integrator with constant-C_L design

required to compensate process corner variation. Thus, we can keep transconductance constant and vary the capacitance or vice versa. These approaches are called constant-G_m and constant-C_L, respectively. For these approaches, the performance of noise, area, and power dissipation is different.

Figure 5 shows the implementation of the programmable integrator. In Fig. 5(a), the unity-gain frequency is defined by the largest transconductance. The output noise current power spectral density v_o^2 is defined to be $4kT\eta G_m$, where η is the excess noise factor of the transconductor. The power dissipation is assumed to be proportional to the transconductance with a factor b. For a given v_o^2, the value of C_L is defined and then we obtain a largest value, ω_{max}, through the largest transconductance.

Figure 5(b) and (c) shows the corresponding value when the unity-gain frequency is adjusted. Thus, the noise, capacitor area, and the power will vary accordingly. For the constant-G_m design, a large capacitor area is required and it is not suitable for high frequency applications. The low noise performance is not very helpful since only the highest noise contribution is needed to be defined over the frequency tuning range. In contrast, the constant-C_L design decreases the transconductance, which implies lower power consumption. The noise performance is equal throughout the frequency tuning range without any overdesign. Therefore, the constant-C_L approach is preferred in our filter design.

In this article, the fourth-order Gm-C low-pass filter based on the biquadratic section is designed. The requirement of the equiripple linear phase fashion is due to the high speed pulse signal in UWB wireless application to reduce inter-symbol interference (ISI) effect. The implementation of the OTA building block is shown in Fig. 6. The proposed OTA circuit is used for all of the transconductor cells. The number of the CMFB circuits is reduced due to the shared low impedance nodes of lossy integrators.

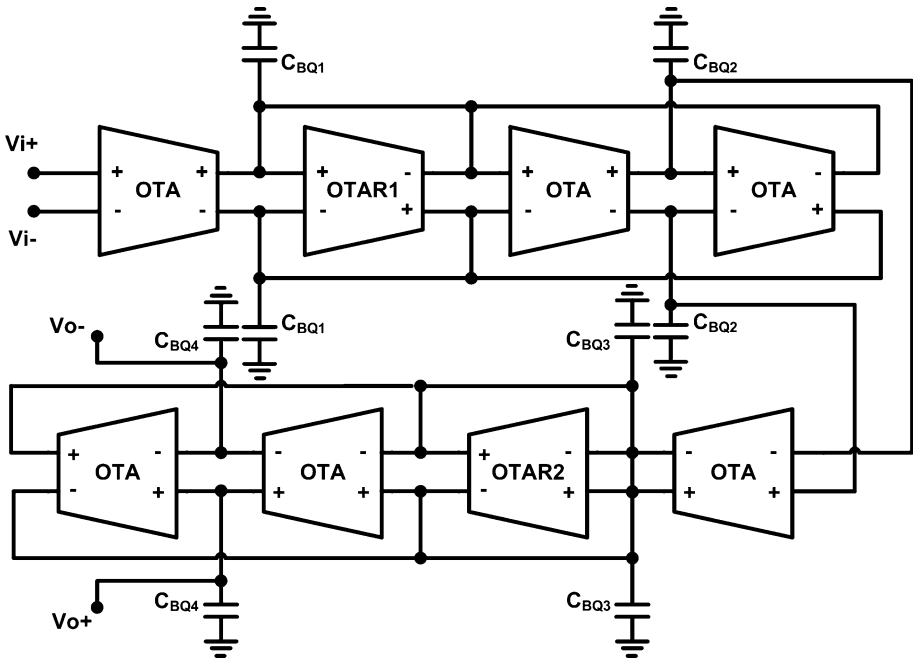

Fig. 6 The fourth-order equiripple linear phase filter

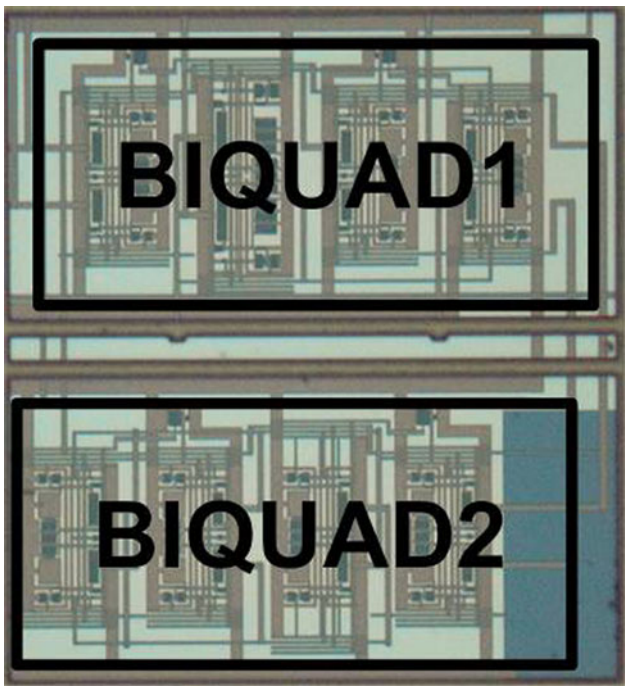

Fig. 7 Die micrograph

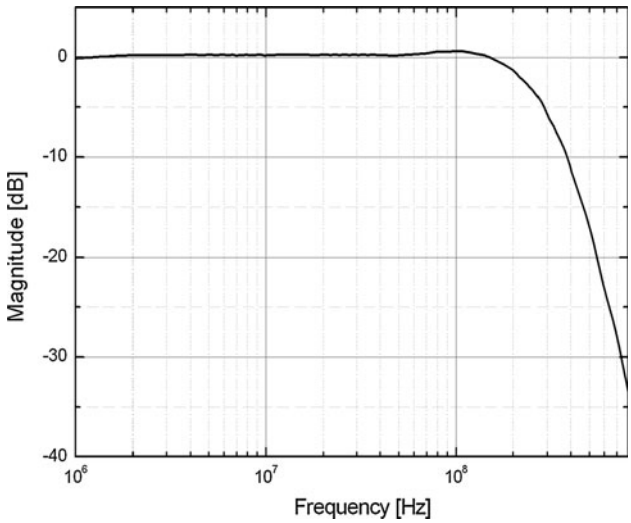

Fig. 8 Measured frequency response of the fourth-order Gm-C filter

The tuning strategy can be achieved by changing the voltage Vtune through the use of the MOS transistor operating in the linear region, and the maximum tuning voltage range of $\mathrm{Vov}(1,2) \times \sqrt{[(1-\alpha)\mathrm{K}(1,2)/\mathrm{K}(3,4)]}$ can be obtained.

The G_m-C filter is designed by using TSMC 0.18-μm CMOS process. The die photograph is shown in Fig. 7, where the active area is 2.4×10^{-2} mm^2. Parasitic capacitances and metal resistances are extracted to simulate

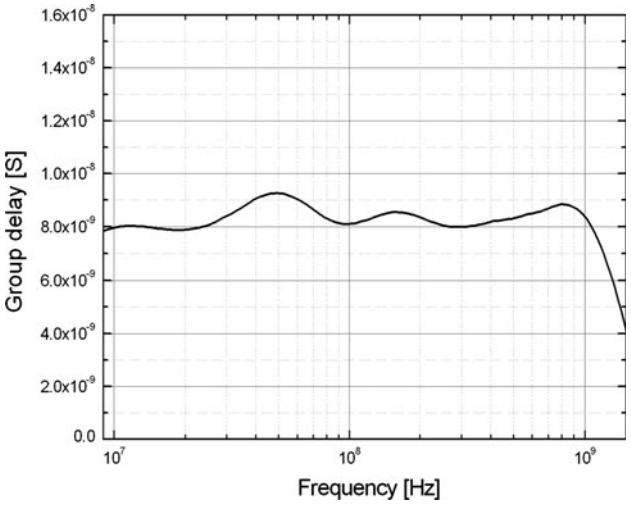

Fig. 9 Measured group delay response of the fourth-order Gm-C filter

the realistic environment. The OTA circuit is simulated by connecting 1 pF capacitance at the output to work as an integrator. The gain of the OTA is nearly 30 dB with 89° phase margin, and the unity-gain frequency is 230 MHz. The current mirror factor α is chosen to be 20/21 and the current mirror ratio B is set to nearly 2. Figure 8 shows the measured magnitude response of the filter. The magnitude response is normalized owing to attenuation from the output buffer. The −3 dB cutoff frequency (fc) of the low-pass G_m-C filter is 250 MHz and the low frequency CMRR is 35 dB. The group delay is almost constant over fc and the group delay ripple is less than 2 ns over the range up to fc, as shown in Fig. 9. The third-order inter-modulation (IM3) distortion with two sinusoidal tones of 400 mV_{pp} is shown in Fig. 10. The IM3 is shown to be less than −40 dB at the speed of 250 MHz.

5 Conclusions

A G_m-C filter implementation with an enhanced-linearity CMOS OTA has been presented, and the design is targeted for UWB wireless application. For the entire filter, the common-mode voltage of the pseudo-differential topology can be well defined by employing suitable CMFB and CMFF circuits. The circuit was fabricated by the TSMC 0.18-μm CMOS process in 1 − V power supply voltage with power consumption of 32 mW. Measurement results show that high speed and excellent linearity can be achieved. Table 1 summarizes the performance of this work with recently reported filters.

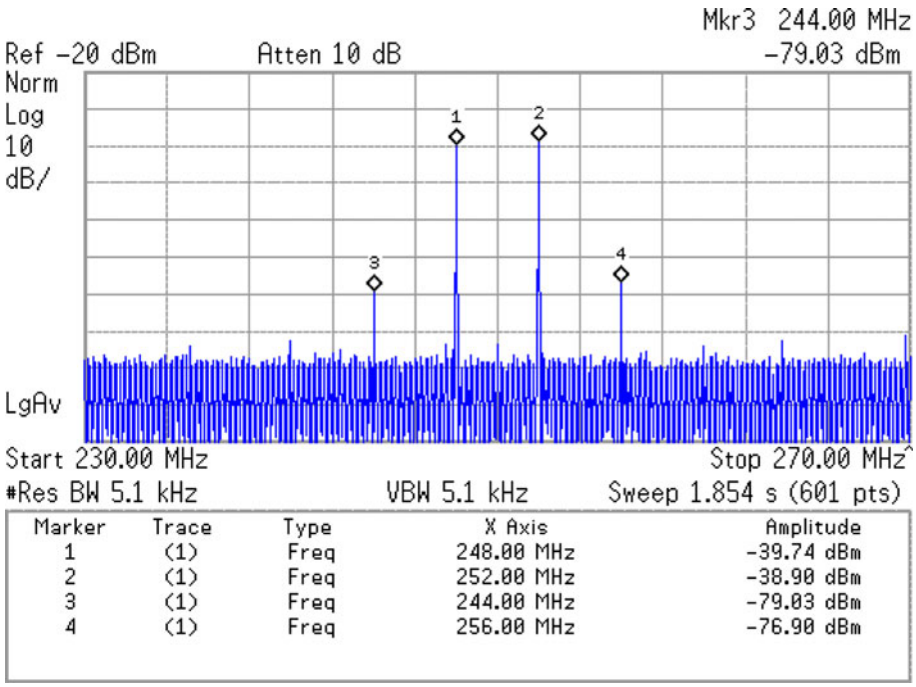

Fig. 10 Measured two tone inter-modulation distortion

Table 1 Comparison of previously reported works

Reference	[11] ESSCIRC 2006	[12] A-SSCC 2006	[13] ISSCC 2007	This work
Technology	0.12-μm CMOS	0.18-μm CMOS	0.13-μm CMOS	0.18-μm CMOS
Filter order	3	8	5	4
−3 dB frequency (MHz)	235	250	240	250
IM3[a]/HD3	−43 dB HD3 @ 50 MHz	−37 dB HD3 @ 150 MHz	–	−40 dB IM3 @ 250 MHz
IIP3	–	–	– 4.82 dBV	3 dBV
Supply voltage	1.5	1.8	1.2	1

[a] Usually IM3 shows the worst case condition to the measurement

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