Random Work-Function-Induced Threshold Voltage Fluctuation in Metal-Gate MOS Devices by Monte Carlo Simulation

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***Abstract*—In this paper, we estimate the effect of random work function (WK) on the threshold voltage fluctuation (σV_{th}) of 16-nm-gate metal-oxide-semiconductor field-effect transistors (MOSFETs) with metal-gate materials. To examine the random WK induced σV_{th}, nanosized metal grains with different gate materials are considered in a large-scale statistical simulation. An analytical expression of the WK induced σV_{th} is proposed based on the Monte Carlo simulation results which can outlook different extents of fluctuation resulting from various metal gates and benefit the device fabrication. Devices with a two-layer metal-gate are further studied for fluctuation suppression; the finding of this paper indicates the first layer of the gate structure plays the most significant role in the suppression of the WK induced σV_{th}, compared with the second layer. This paper provides an insight into random work-function-induced threshold voltage fluctuation, which can, in turn, be used to assess metal gate characteristics of MOSFETs.**

***Index Terms*—Averaged work function, metal gate, Monte Carlo, MOS devices, threshold voltage fluctuation simulation, work function (WK).**

I. Introduction

CHARACTERISTIC fluctuation is a crucial issue for nanometer-scale (nanoscale) metal-oxide-semiconductor field-effect transistors (MOSFETs) [1]. For state-of-the-art nanoscale devices, the intrinsic parameter fluctuations resulting from line edge roughness, random dopants, and other causes have substantially affected device's characteristics [2]. Diverse approaches have recently been presented to investigate intrinsic parameter fluctuations in semiconductor devices [2]–[10]. Among these approaches, the high-κ/metal gate is one of the key technologies for suppressing intrinsic parameter fluctuations; it has been recognized as a key to sub-45-nm transistor technology due to the small gate leakage current with an increased gate capacitance. The sheet resistance is also reduced with the use of metal as gate material. Comparing with the poly-gate technology, the metal gate material will not react with high-k dielectric; therefore, there exists a less pinning effect of threshold voltage (V_{th}). Moreover, the phonon scattering effect is significantly reduced due to the less quantum resonance effect [11], [12].

However, the grain orientation of metal is uncontrollable during growth period. Metal grains will be grown up to a few nanometers in size under temperatures that normally used in semiconductor device fabrication [2], [11]. The gate area of 16-nm devices will contain only a small number of grains. The use of metal as gate material will result in the work function fluctuation (WKF) due to the dependence of work function on nanosized metal grain orientations [13]. A simulation study of WKF is, thus, necessary for us to understand the threshold voltage fluctuation (σV_{th}) in 16-nm devices. In this paper, we present a Monte Carlo simulation to evaluate the effect of WKF on 16-nm MOSFET devices. Both the metal grain size and the metal gate material are considered in the statistical simulation to examine the effect of WKF on device's V_{th}. Among four examined gate materials, titanium nitride (TiN) possesses the smallest σV_{th}. A device with a multilayer metal gate material is further simulated; it is found that the first layer plays the most important role in suppressing σV_{th}.

This paper is organized as follows. In Section II, we introduce the simulation procedure for studying the WKF induced σV_{th}. In Section III, we study and model the fluctuations with respect to different device gate area, size of metal grains, and gate materials. We further advance the method to explore the WKF induced σV_{th} for devices with multilayer metal gate-stacks. Finally, we draw conclusions and suggest the future work.

II. Statistical Simulation Technique

We explore the planar MOSFET device with amorphous-based HfSiON gate-stacks and different metal materials; TiN and tantalum nitride (TaN) are considered in the n-type MOSFET (N-MOSFET), and tungsten nitride (WN) and molybdenum nitride (MoN) are used for the p-type MOSFET (P-MOSFET) [2], [12]. The nominal device characteristics of the examined TiN-gate N-MOSFET and the MoN-gate P-MOSFET devices are mainly according to the projection of ITRS roadmap for low operating power applications. Fig. 1(a) indicates the gate area (A) containing many metal grains

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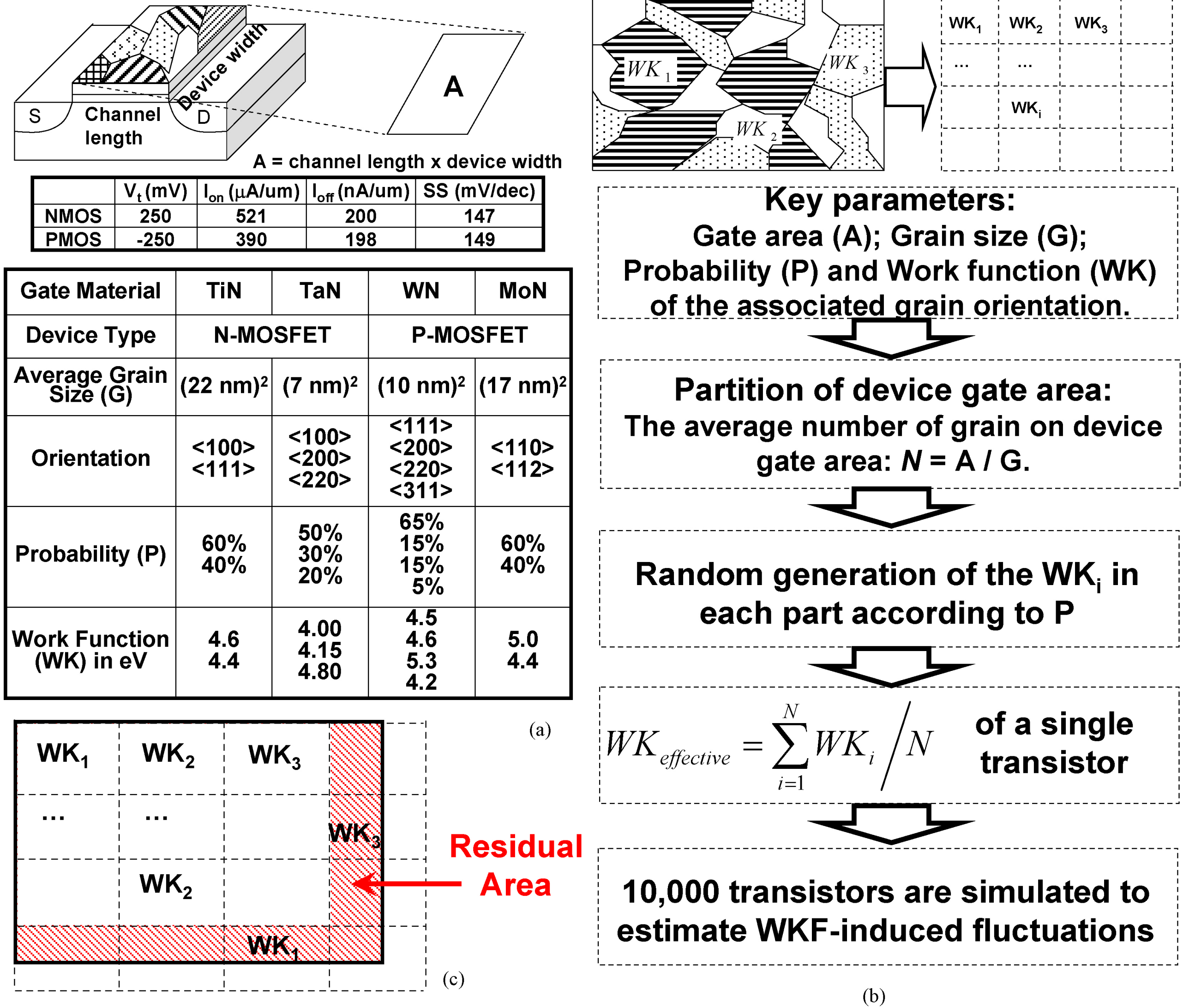

	V_t (mV)	I_{on} (μA/um)	I_{off} (nA/um)	SS (mV/dec)
NMOS	250	521	200	147
PMOS	-250	390	198	149

Gate Material	TiN	TaN	WN	MoN
Device Type	N-MOSFET		P-MOSFET	
Average Grain Size (G)	(22 nm)^2	(7 nm)^2	(10 nm)^2	(17 nm)^2
Orientation	<100> <111>	<100> <200> <220>	<111> <200> <220> <311>	<110> <112>
Probability (P)	60% 40%	50% 30% 20%	65% 15% 15% 5%	60% 40%
Work Function (WK) in eV	4.6 4.4	4.00 4.15 4.80	4.5 4.6 5.3 4.2	5.0 4.4

(a) (b) (c)

Fig. 1. (a) Device gate area is A which composes many nanosized metal grains; the average grain size (G), the probability (P), and the work function (WK) of each grain orientation for different metal materials used in this paper are listed. The performances shown here are the N-MOSFET with a TiN gate and the P-MOSFET with a MoN gate, where $V_{\rm th}$ is the threshold voltage, $I_{\rm on}$ and $I_{\rm off}$ are the on-state and off-state currents, and SS is the subthreshold swing. (b) Proposed simulation flow to study the WKF induced $\sigma V_{\rm th}$, the grain shape is assumed to be square without loss of generality. (c) In the simulation procedure, residual areas are also considered to provide the best accuracy of statistical simulation.

for a given material, the average grain size (G) which is adopted from experimental observations in [11], for example, the probability (P), and the work function (WK) of grain orientation for different metal materials used in the Monte Carlo simulation [12]. Since each random grain orientation has different WK which should be treated as a probabilistic distribution rather than a deterministic value, the Monte Carlo simulation is advanced to account for such a probabilistic distribution. Fig. 1(b) shows the simulation procedure. First, the gate area of a 16-nm transistor is partitioned into several square subareas according to the average grain size. The WK of each partitioned subarea is randomly generated according to its probability; and the effective WK of the metal gate is equal to an averaged value of all WKs. We calculate the effective work function of 10 000 randomly generated gates to estimate the WKF induced $\sigma V_{\rm th}$. Notably, the approach appearing in [12] does not consider the residual of gate area. Without including residual of gate area may underestimate $\sigma V_{\rm th}$. In order to consider the residual of gate area, as shown in Fig. 1(c), we also randomly generate WK for each residual grain in the Monte Carlo simulation and take account of the corresponding weight of these residual areas when calculating the total effective WK.

III. Results and Discussion

First, we compare the difference of $\sigma V_{\rm th}$ in the proposed method with and without considering residual areas because the device's gate area will not always contain integer grains. As shown in Fig. 2(a), for N-MOSFETs with (16 nm)^2 TiN gate, for a 4-nm length of metal grain, the threshold voltage fluctuation is the same ($\sigma V_{\rm th}$ = 24.3 mV) for the method with and without considering residual area because the device area of (16 nm)^2 divided by the grain size of (4 nm)^2 is

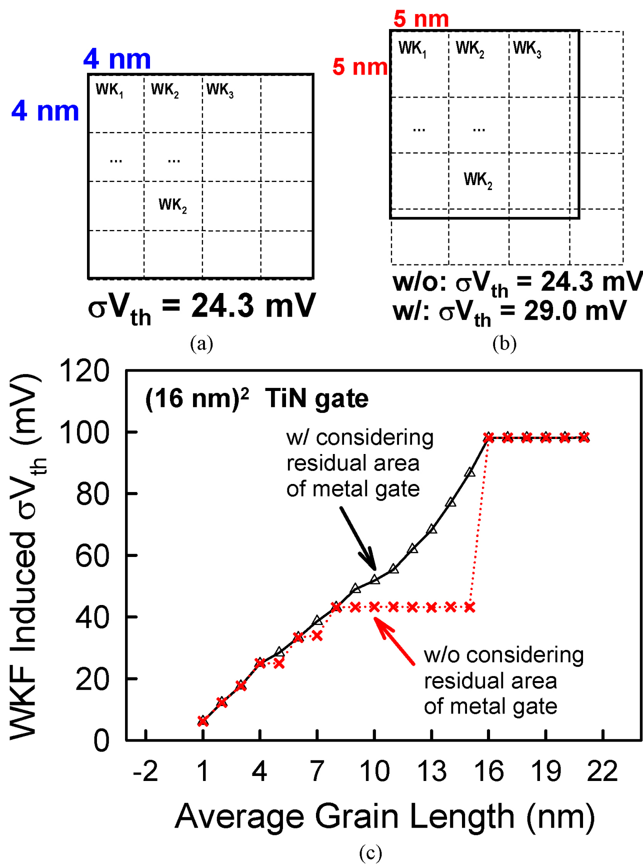

Fig. 2. Plot of device with a $(16\,\text{nm})^2$ TiN gate, where each grain size is (a) $(4\,\text{nm})^2$ and (b) $(5\,\text{nm})^2$. (c) Plot of the WKF induced σV_{th} as a function of the average grain size for the method with (w/) and without (w/o) considering the residual areas of metal gate.

an integer. For a 5-nm length of metal grain, as shown in Fig. 2(b), the fluctuation of threshold voltages calculated with considering residual area ($\sigma V_{\text{th}} = 29.0\,\text{mV}$) is greater than that of without considering residual area ($\sigma V_{\text{th}} = 24.3\,\text{mV}$). The device area of $(16\,\text{nm})^2$ divided by the grain size of $(5\,\text{nm})^2$ is not an integer and it has a fractional part, and such a residual area is not considered into the calculation without considering residual area; consequently, the fluctuation of threshold voltages calculated with considering is greater than that of without considering residual area. As shown in Fig. 2(c), the WKF induced σV_{th} increases continuously as the average grain length (i.e., the square root of averaged grain size) increases when the Monte Carlo calculation with considering the residual areas. If we do not consider the residual area properly the change of σV_{th} behaves as a step-like function when the average grain length increases. Estimation of σV_{th} will be underestimated and compared with the result of Monte Carlo simulation with considering residual area of metal gate because sizeable residual areas will be ignored in this scenario. For example, for the device area of $(16\,\text{nm})^2$, the device maintains σV_{th} the same and is less than the fluctuation of threshold voltages calculated with considering residual areas because the residual areas are not counted into the calculation without including residual areas for the grain sizes varying from $(8\,\text{nm})^2$ to $(15\,\text{nm})^2$.

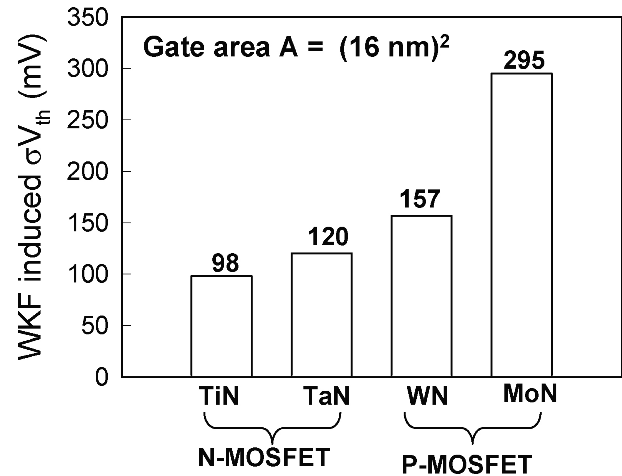

Fig. 3. WKF induced σV_{th} with respect to different material whose properties are listed in Fig. 1(a). The gate area of devices is $(16\,\text{nm})^2$.

Fig. 3 shows the WKF induced σV_{th} for the property of metal, as shown in Fig. 1(a). We find that the gate with TiN material exhibits the smallest σV_{th} among four different gate materials and the device with MoN gate shows the largest σV_{th}. To find the key factor of WKF, we further compare the σV_{th} with respect to different materials and gate areas (A = channel length $\times$ device width), where the grain size $(4\,\text{nm})^2$ is fixed, as shown in Fig. 4. The device with TiN gate induces the smallest σV_{th} due to few grain orientations and small WKF of each orientation. As shown in Fig. 5, among TiN, TaN, WN, and MoN gate materials, we compare the WKF induced σV_{th} versus the size of metal grains, where the gate area of $(16\,\text{nm})^2$ is fixed. The results indicate that the value of σV_{th} increases as the grain size increases. It is because when the grain size is large, the gate area may contain only one grain, and thus the effective WK of a single transistor could be either 4.4 or 4.6 eV; consequently, it induces two quite different threshold voltages, as shown in Fig. 6(a). As a result, it will result in a relatively large standard deviation of the threshold voltage in the simulated 10 000 devices. On the other hand, when the metal gate's grain size is small (e.g., amorphous-like material), the gate area contains many nanosized metal grains and the averaged WK approaches a Gaussian distribution, as shown in Fig. 6(b). From a device fabrication point of view, metal deposition at a low temperature or adding composite materials could be considered to obtain small size of metal grains. Additionally, when the grain size is larger than the device's gate area, the σV_{th} will saturate at a specific value due to the unchanged number of grains in the device's gate area (i.e., it contains only one grain which totally covers the gate area). We observe that the WKF induced σV_{th} is strongly affected by the gate area, the size of metal grains, and the adopted gate material, according to the results of aforementioned Monte Carlo simulation. Therefore, an analytical expression is empirically proposed to model the WKF induced σV_{th}

$$\sigma V_{\text{th}} = \alpha \sigma_{\Phi m} \sqrt{\frac{G}{A}} \tag{1}$$

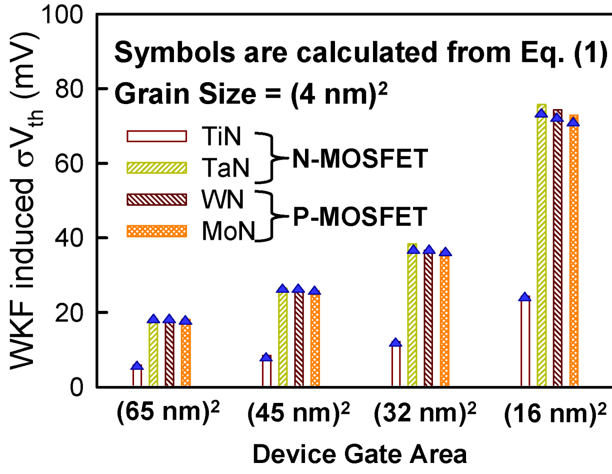

Fig. 4. Comparison of the WKF induced σV_{th} among four different gate materials with respect to different device gate areas (the area A = channel length $\times$ device width). A minimal grain size of (4 nm)^2 is assumed for all metal grains. Each symbol is analytically calculated by using (1).

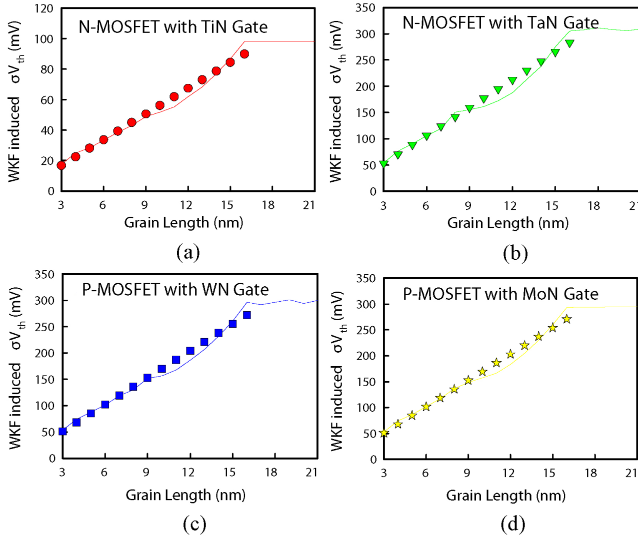

Fig. 5. WKF induced σV_{th} as a function of grain length for the N-MOSFET with the (a) TiN and (b) TaN gates, and the P-MOSFET with the (c) WN and (d) MoN gates, respectively, where the gate area is (16 nm)^2 and the grain length is the square root of grain size. The line is the Monte Carlo simulation result and the symbol is analytically calculated by using (1).

where G and A are the grain size and the device gate area, respectively, and $\sigma_{\Phi m}$ is the work function deviation calculated from the probability P and the work function of metal grain's orientation. The α is a fitting coefficient, which is independent of the probability P and gate area A, and could be validated from silicon data experimentally. According to metal's property, as shown in Fig. 1(a), the extracted values of $\sigma_{\Phi m}$ for TiN, TaN, WN, and MoN are 0.098, 0.305, 0.296, and 0.294, respectively. The symbols, as shown in Figs. 4 and 5, are the calculated σV_{th} using (1) with the coefficient $a = 920$; as shown in Fig. 4, the calculated σV_{th} using (1) versus the device gate area show acceptable approximations to the Monte Carlo simulation. Notably, for the results before the saturation, the calculations by using (1) with respect to four

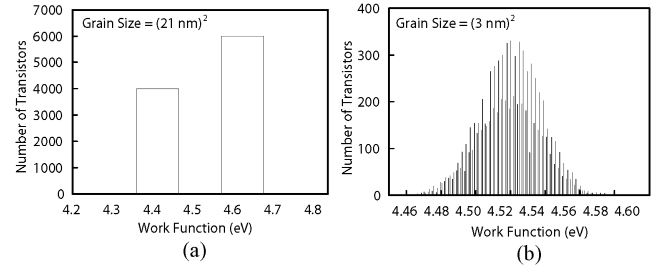

Fig. 6. Work-function distribution for the grain size of (a) (21 nm)^2 and (b) (3 nm)^2.

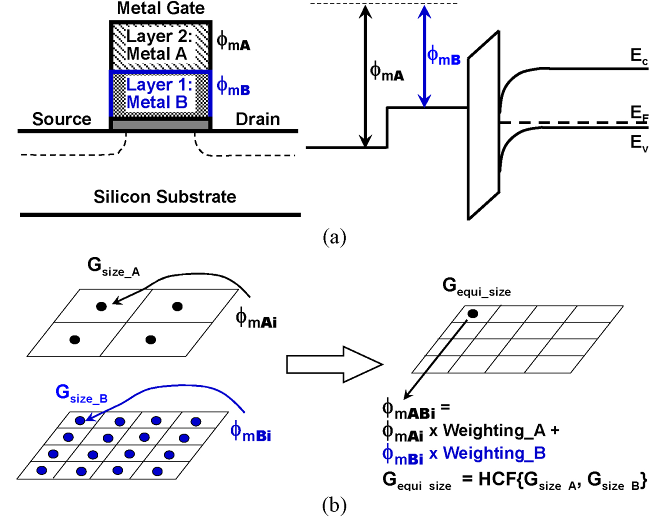

Fig. 7. (a) Schematic plot of the simulated two-layer metal-gate structure and its band diagram, ϕ_{mB} and ϕ_{mA} are WKs of metal with respect to different grain orientation at the first and second layers, respectively. (b) Illustration of the method used to determine the equivalent grain size ($G_{\text{equi_size}}$) and the associated WK (ϕ_{mAB}) for the Monte Carlo simulation of the WKF induced σV_{th} of the device with two-layer metal-gate structure. Notably, the adopted weightings of all WKs in partitioned grain areas are determined from device simulation. ϕ_{mBi} and ϕ_{mAi} are WKs at each point i within the local gate area of the metal B (layer 1) and the metal A (layer 2), respectively.

TABLE I

COMPARISON OF THE THRESHOLD VOLTAGE FLUCTUATION OF THE 16-NM N-MOSFET WITH DIFFERENT TWO-LAYER METAL-GATE STRUCTURES

Material	Minimal Grain Size	Device Gate Area	σV_{th} (mV)
TiN (layer1)	(4 nm)^2	(16 nm)^2	22.9
MoN (layer2)	(4 nm)^2		
MoN (layer1)	(4 nm)^2	(16 nm)^2	65.9
TiN (layer2)	(4 nm)^2		

Compared with the results of devices with single-layer metal gate, the device with TiN as the first layer of the two-layer metal-gate configuration TiN + MoN has a minimal σV_{th} of 22.9 mV.

different materials are in good agreement with the Monte Carlo simulations. Equation (1) is validated for those grain sizes which are smaller than the device's gate area; for the grain size larger than the gate area, the WKF induced σV_{th} is saturated, as mentioned above. Equation (1) works for both N-MOSFET and P-MOSFET devices which could be used as first-order estimation for the effect of WKF on metal-gate devices.

Device with a multilayer metal gate structure is one of the process techniques to reduce the WK induced σV_{th}. The Monte Carlo simulation technique discussed in this paper can also predict the tendency of σV_{th} owing to a multilayer metal gate. Fig. 7(a) illustrates a two-layer metal-gate structure and its band diagram; as shown in Fig. 7(b), we introduce a mapping method to estimate the WKF resulting from the structure of multilayer metal gate. We first independently and randomly generate the WK of each grain for different metal layers by following the procedure, as shown in Fig. 1(b). Thus, each layer has its own distribution of WK. To calculate the averaged WK for the device with the two-layer metal-gate structure, we first find the highest common factor, also known as the greatest common divisor, of each grain size between two layers; and then, the WK at each point within the local gate area is a combination of the ϕ_{mB} and ϕ_{mA} with a given weight, as shown in Fig. 7(b), and the ϕ_{mABi} is the effective WK in the given partitioned area. The weight of each layer could be determined by the device simulation; for example, by alternating the metal layers as the first layer on the gate, we can get different threshold voltages. Then the weight of each layer can be determined by the percentage of the total sum of those threshold voltages, where the device characteristic is estimated by using a 3-D device simulation [2], [8], [9].

Based upon this mapping method, we examine the device with a two-layer metal-gate structure, where devices with two layers TiN and MoN denoted as TiN + MoN, and MoN and TiN denoted as MoN + TiN are studied. The adopted weight of the first layer is 90% and that of the second layer is 10%. Table I lists the σV_{th} comparison for the device using two different materials as the first layer of the two-layer metal-gate structures. Considering the device area of $(16\,\text{nm})^2$, for example, for the given materials TiN and MoN with the grain size of $(4\,\text{nm})^2$, as the first layer of the two-layer metal-gate structure, the results of this paper suggest that the first layer dominates the σV_{th}. It is because physically the first layer of metal gate plays the most significant controllability to the surface of device channel. Compared with the results of 16-nm device with TiN and MoN gate materials as shown in Fig. 4, we find that the σV_{th} is reduced from 24.3 mV to 22.9 mV for the device with TiN as the first layer of the two-layer metal-gate structure. For the device with MoN as the first layer of the two-layer metal gate materials, the reduction is from 72.9 mV to 65.9 mV, as summarized in Table I.

IV. Conclusion

In this paper, a simple Monte Carlo simulation was performed to estimate the effect of WKF on the threshold voltage of 16-nm devices. The results of this paper have shown that the large size of metal grains and small device's gate area will induce sizeable σV_{th}. However, the fluctuation will be saturated if the grain size is larger than the device's gate area. Devices with TiN gate have shown interesting behavior against WKF due to few grain orientations and small WK deviation of each orientation. For the device with a multilayer metal gate structure, the first layer plays the most important role in suppressing the WK fluctuation. The Monte Carlo simulation method has also been implemented for random WK induced σV_{th} in 16-nm FinFETs. The results predicted with this model could be in good agreement with the experimental data [14], thus proving the reliability of this method. Instead of the statistically averaged WK method presented here, studying WKF with a realistic 3-D device simulation will bring more rich physical insights. In addition, the grain size may obey a probability distribution; instead of an average value assumed in this paper, a probability distribution to generate sizes of different grains covering the gate should be used in the future work. Notably, we do not consider the random-dopant fluctuation with the WKF simultaneously and this should be subject to further investigation for more accurate estimation and engineering findings.

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