Low-Temperature Growth of Silicon-Boron Layer as Solid Diffusion Source for Polysilicon Contacted p^+-n Shallow Junction

Tan Fu Lei, Tung Po Chen, Horng-Chih Lin, *Member, IEEE,* and Chun-Yen Chang, *Fellow, IEEE*

Abstract— **A new material, Si-B, is proposed as a solid diffusion source for fabrication of poly-Si contacted p^+-n shallow junctions. The junction depth of the Si-B source diode has been measured and compared with that of a BF_2^+-implanted poly-Si source diode. It was found that the Si-B source diode had a much shallower junction and was less sensitive to thermal budget than the BF_2^+ source diode. This was attributed to the smaller surface concentration and diffusivity of boron in the silicon in Si-B source diodes. Regarding electrical characteristics of diodes with a junction depth over 500 Å, a forward ideality factor of better than 1.01 over 8 decades and a reverse-current density lower than 0.5 nA/cm^2 at −5 V were obtained. As the junction depth shrank to 300 Å, the ideality factor and reverse current density of diodes increased slightly to 1.05 and 1.16 nA/cm^2, respectively. These results demonstrated that a uniform ultra-shallow p^+-n junction can be obtained by using a thin Si-B layer as a diffusion source.**

I. Introduction

In order to obtain high-performance devices, heavily doped poly-Si films were used as a diffusion source to fabricate the elevated source/drains of CMOS devices and poly-Si emitter bipolar transistors [1], [2]. The advantages of using a heavily doped poly-Si film as a diffusion source are increased packing density and switching speed, and elimination of aluminum spiking through p-n shallow junctions [1]–[4]. Therefore, the study of poly-Si contacted p^+-n shallow junctions is important for p-n-p poly-Si emitter bipolar transistors and CMOS device applications.

Poly-Si contacted p^+-n shallow junctions can be fabricated using several techniques.

1) The p^+ poly-Si films are often doped by BF_2^+ implantation, and boron atoms diffuse into the Si substrate to form p^+-n shallow junctions [5], [6]. However, due to the rapid diffusion of boron atoms, the emitter-base junction depth was sensitive to the thermal budget [5]–[8]. It was also reported that a lower implantation dose at the poly-Si contacted window sidewall, and the shadowing effect may lead to a nonuniform junction [9]. As expected, the effects were more pronounced for as-deposited poly-Si with an anisotropic structure [6]. It was also found that incorporation of fluorine atoms in the poly-Si films had the effect of accelerating the break-up of poly-Si/Si interfacial oxide, and formation of fluorine bubbles at the poly-Si/Si interface [7], [10], [11]. It is well known that the morphology of the poly-Si/Si interface plays an important role in the impurity diffusion profile and the electrical properties of polysilicon-emitter bipolar transistors [2], [3]. The break-up of interfacial oxide affects the transport of majority and minority carrier in the emitter region [12].
2) The use of B-implanted poly-Si as diffusion sources has been investigated in the poly-Si/Si system [13], [14]. It was found the boron profile and the junction depth were dependent on the dopant dose. Moreover, a high dopant dose requires undesirably long implantation time.
3) In-situ boron doped poly-Si diffusion sources were also investigated in the poly-Si/Si system [14]. It was reported that the junction depth and the morphology of poly-Si/Si interfaces were related to boron concentration [14].

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The authors are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, and National Nano Device Laboratory, Hsinchu 300, Taiwan, R.O.C.

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As devices are scaled downward, it is necessary to scale the vertical doping profile and base width downward. A new process that forms very shallow and uniform junctions is required. In previous studies, we have shown that an Si-B layer can be deposited in an UHV/CVD system at low temperature (550°C) [15]. After thermal annealing, we found some boron atoms diffused from the Si-B layer into the poly-Si, but most boron atoms were immobilized in the Si-B layer. These results indicated that the Si-B layer can be regarded as an infinite diffusion source of boron atoms. The previously mentioned problems in forming poly-Si contacted p^+-n shallow junctions can be avoided by using this technique. Furthermore, a high throughput can be obtained in a multi-wafer UHV/CVD system. In this paper, we report on the characteristics of poly-Si contacted p^+-n shallow junctions formed with a thin Si-B layer as a diffusion source (Si-B source). For comparison, shallow junctions were also fabricated using a conventional BF_2^+-implanted poly-Si as a diffusion source (BF_2^+ source). The boron profiles and electrical characteristics of the Si-B- and BF_2^+-source diodes were analyzed and compared.

II. Experimental

The poly-Si contacted p^+-n diodes were fabricated on n-type, (100), Si wafers, with a resistivity of 0.5–2 Ω · cm.

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A 6300 Å-thick field oxide was grown and patterned. Prior to poly-Si deposition, all wafers were dipped in a dilute HF solution to remove surface native oxide, a deionzed-water rinse followed deoxidizing. Then, poly-Si films with a thickness of 3500 Å were deposited in an LPCVD system at 625°C using SiH_4 gas. All wafers were recleaned and a polycrystalline Si-B layer with a thickness of 350 Å was deposited in UHV/CVD system at 550°C. After Si-B layer deposition, all wafers were annealed in the temperature range of 875–1000°C. During the drive-in stage, some boron atoms diffused from the Si-B layer into the poly-Si and Si to form p^+-n shallow junctions. In order to remove the Si-B layer, it was completely oxidized in wet O_2 ambient for a short oxidation time during the drive-in stage. The oxidation time was chosen to match the drive-in temperature. After removing the oxide layer, aluminum film was evaporated and patterned. Finally, all devices were sintered at 400°C for 30 min in an N_2 ambient. For comparison, devices fabricated via BF_2^+ implant (80 KeV, 6×10^{15} cm^{-2}) into poly-Si, with drive-in in the temperature range of 850–1000°C forming p^+-n diodes were made. The cross-sectional structure of a poly-Si contacted diode is shown in the inset of Fig. 6(a). The boron and fluorine depth profile were measured by secondary ion mass spectroscopy (SIMS) using O_2^+ primary ion bombardment. The current-voltage characteristics of the diodes were measured with an HP4145B parameter analyzer. Reverse current temperature dependence was measured from room temperature to approximately 200°C on a thermal chuck to study the junction leakage current mechanism.

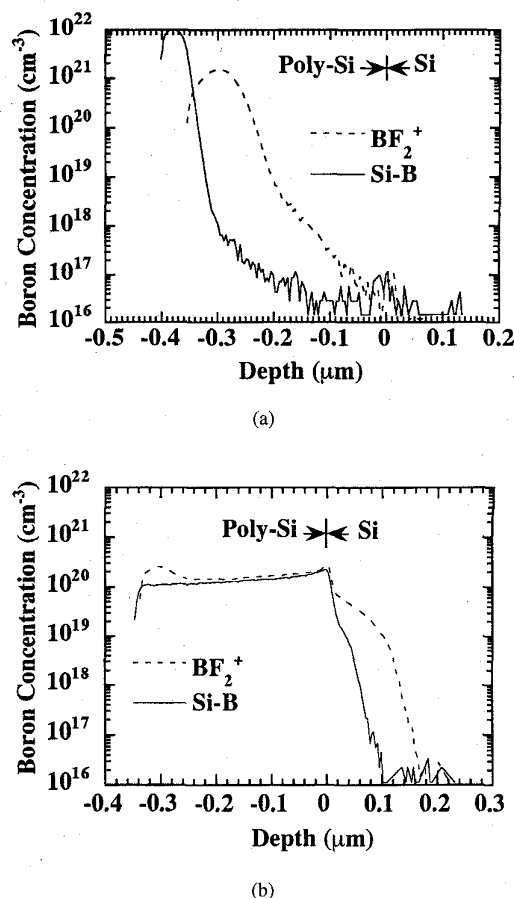


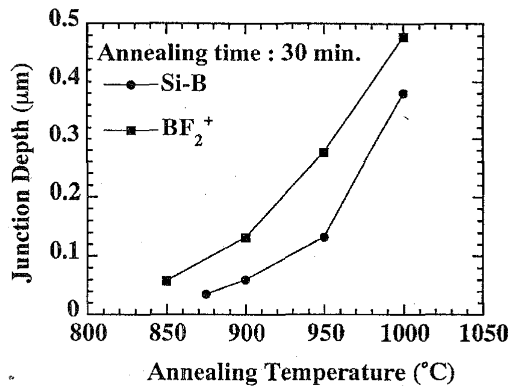
Fig. 1. (a) SIMS boron profiles of as-deposited Si-B layers on poly-Si and BF_2^+ as-implanted poly-Si. (b) SIMS boron profiles in diodes from Si-B and BF_2^+ sources after drive-in at 900°C for 30 min.

III. Results and Discussions

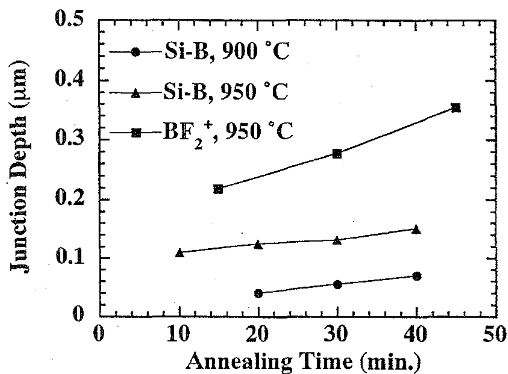
A. SIMS Boron Profile and Junction Depth

Fig. 1(a) shows the SIMS boron depth profiles of as-deposited Si-B layer on poly-Si and BF_2^+-implanted poly-Si. It is seen that the boron concentration in the Si-B layer is extraordinarily high. The XTEM micrograph showed that the Si-B/poly-Si interfaces were free of oxide [8], [15]. The oxygen depth profile determined by the SIMS using Cs^+ primary ion bombardment also showed that there is no significant peak at the UHV/CVD layer/LPCVD layer interface. Transition electron diffraction pattern analysis showed that the silicon-hexaboride (SiB_6) phase was present in the as-deposited Si-B layer [15]. By contrast, the boron profile of BF_2^+ as-implanted poly-Si was broader and had a boron peak 750 Å beneath the poly-Si surface. The XTEM micrograph revealed that the poly-Si surface layer was completely amorphized to a depth about 1000 Å by BF_2^+ implantation. Fig. 1(b) shows the SIMS boron depth profiles in the poly-Si/Si diodes made with both diffusion sources, after drive-in at 900°C for 30 min. It can be seen that the Si-B layer was completely removed after the drive-in step. The boron profiles for diodes made with both diffusion sources in single-crystal silicon were characterized by Gaussian-like profile. Moreover, the boron profile of Si-B source in the silicon substrate was much shallower than that of BF_2^+ source. The junction depth of diodes made with Si-B and BF_2^+ sources were estimated to be 500 and 1300 Å, respectively. Fig. 2(a) shows the junction-depth curves, deduced from the SIMS profiles, versus the annealing temperature for diodes from both diffusion sources. It can be seen that the BF_2^+ diode junction depths increased rapidly as annealing temperature was increased. In contrast, the junction depths of diodes from the Si-B source were less sensitive to temperature at annealing temperatures below 950°C. When the annealing temperature rose above 950°C, however junction depth also increased rapidly for Si-B source diodes. The junction depths of Si-B source diodes were about 800 Å to 1300 Å shallower than BF_2^+ source diodes at the same annealing temperature. Fig. 2(b) shows junction depth curves versus annealing times at different temperatures for diodes from both diffusion sources. The junction depths of Si-B source diodes increased slowly for longer annealing times. In contrast, the junction depths of BF_2^+ source diode increased rapidly with increasing annealing times. At 950°C, the slope of BF_2^+ source diode is 3.45 times higher than that of BF_2^+ source diode. These results demonstrated that the junction depths of Si-B source diodes were less sensitive to the thermal budget than those of BF_2^+ source diodes.

As mentioned previously, the Si-B/poly-Si interfaces were free of oxide, therefore, the diffusion of boron atoms was



(a)



(b)

Fig. 2. (a) Junction depth versus annealing temperature for Si-B- and BF_2^+-source diodes. (b) Junction depth versus annealing time for Si-B and BF_2^+ sources.

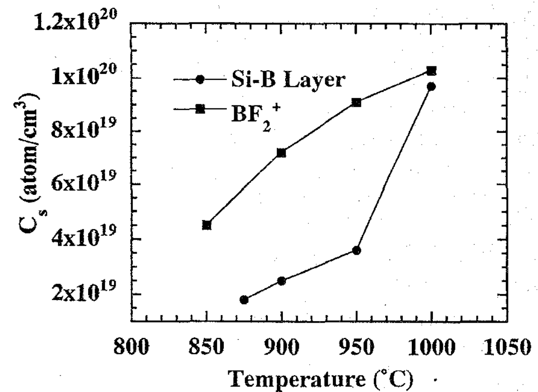


Fig. 3. Surface boron concentration versus annealing temperature for Si-B- and BF_2^+-source diodes.

not limited by the Si-B/poly-Si interface. In addition, the much deeper junction depth in BF_2^+ source diodes cannot be attributed to the deeper boron profile in Fig. 1(a) because the diffusivity of the boron in poly-Si was 50 to 220 times greater than in Si [5]. The heavily poly-Si films could be considered a constant diffusion sources due to the rapid diffusion of boron in poly-Si. Referring to Fig. 1(b), it should be noted that the surface concentration of BF_2^+ source diodes was much greater than that of Si-B source diodes. The surface concentration C_s, was obtained by linear extrapolation of boron profiles in the Si to the original poly-Si/Si interface [14]. For a constant diffusion source, the junction depth X_j is usually approximated by

$$X_j = K(D_s^t)^{1/2} \quad (1)$$

where K is a numerical constant, and D_s is the effective boron diffusivity for $C = C_s$. This indicate that the junction depth is strongly related to the surface concentration C_s. Fig. 3 shows the variations of C_s with annealing temperatures for both diffusion sources. The C_s values of Si-B source diodes increased slightly with annealing temperature but to a much lesser degree than the BF_2^+ source diodes at annealing temperatures below 950°C. As annealing temperature rose above 950°C, C_s values increased rapidly with temperature reaching nearly the C_s value of BF_2^+ source diodes. The C_s values trend is consistent with the variation of junction depths shown in Fig. 2(a). It has been reported that C_s values can be increased with the increasing boron concentration in the poly-Si [13]. It was thought that the break-up of interfacial oxide was dependent on the dopant dose [16]. The break-up of interfacial oxide leads to an enhancement of dopant emissivity at the poly-Si/Si interface. However, as shown in Fig. 1(a), boron concentrations in the poly-Si films were nearly the same for diodes from both diffusion sources in our study. Fig. 4(a) and 4(b) shows the XTEM micrographs of poly-Si/Si for Si-B-and BF_2^+-source diodes after drive-in at 900°C for 30 min, respectively. For BF_2^+-source diodes, the poly-Si films were epitaxially aligned with silicon substrate and the fluorine bubbles were present at the original poly-Si/Si interface. In contrast, the epitaxial regrowth of poly-Si film does not occur in Si-B source diodes. For BF_2^+-source diodes, the SIMS fluorine profiles showed a large fluorine atom pile-up at the poly-Si/Si interface after annealing. The pile-up of fluorine at the poly-Si/Si interface leads to an enhancement of epitaxial regrowth of poly-Si films and the formation of fluorine bubbles. The faster break-up of interfacial oxide and the formation of fluorine bubbles in BF_2^+ source diodes may lead to enhancement of dopant emissivity at the poly-Si/Si interface and a larger C_s value. For Si-B source diodes, a rapid increase in C_s values at annealing temperatures of 950°C to 1000°C was also attributed to the break-up of interfacial oxide.

Fig. 5 shows the Arrhenius plots of boron diffusivity against reciprocal absolute temperature for diodes from both diffusion sources. D_s was calculated from the SIMS measurements according to (1) with $K = 2.4$ [17]. The boron diffusivity in BF_2^+-source diodes was found to be much larger than that in Si-B-source diodes. The activation energy values of boron diffusion in Si for Si-B- and BF_2^+-source diodes were determined to be 4.69 and 3.71 eV, respectively. As compared with the activation energy of boron diffusion in Si (3.42 eV) [18], the larger activation energy value of boron diffusion in Si for diodes from both diffusion sources was attributed

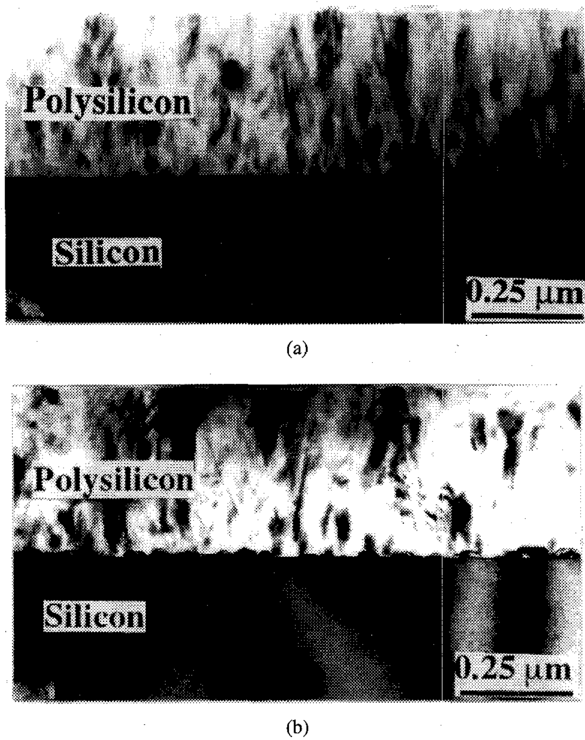


Fig. 4. XTEM micrographs of poly-Si/Si for (a) Si-B-source diodes, and (b) BF_2^+-source diodes after drive-in at 900°C for 30 min.

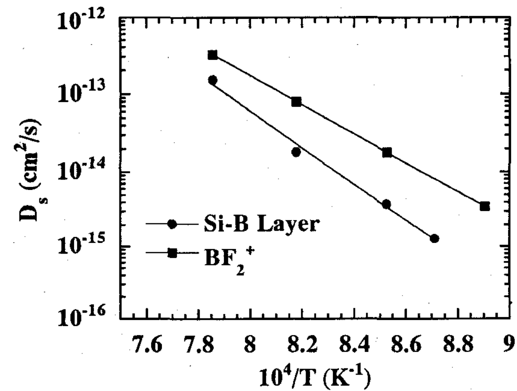


Fig. 5. Boron diffusivity versus reciprocal absolute temperature for Si-B- and BF_2^+-source diodes.

to a diffusion barrier at the poly-Si/Si interface. As the oxidation enhanced boron diffusion [18], the smaller boron diffusion activation energy in BF_2^+-source diodes than in Si-B-source diodes may have been caused by the injection of Si self-interstistials, [I], into the Si substrate. The [I] could be generated in several ways.

1) The break-up of interfacial oxide was a source of [I] which enhanced the diffusion of boron in the poly-Si/Si [16]. It has also been reported that interfacial oxide can act as a diffusion barrier to the diffusion of boron in the poly-Si/Si, and the injection of [I] into the Si substrate [19]. As mentioned previously, the break-up of interfacial oxide was enhanced by the presence of fluorine atoms. Therefore, deeper junctions were obtained for BF_2^+ source diodes.
2) Injection of point defects can be caused by implantation defects in poly-Si [19]. It has been demonstrated that the diffusion of boron in poly-Si/Si is enhanced by implantation defects. For BF_2^+ implantation, the poly-Si surface layer was completely amorphized to a depth of about 1000 Å. The injection of implantation defects could lead to deeper junctions in diodes from BF_2^+ source.
3) The pile-up of fluorine atoms at the poly-Si/Si interface could lead to the formation of fluorine bubbles at the poly-Si/Si interface in diodes from BF_2^+ sources after annealing [11]. Fluorine bubbles were found to increase in size with higher annealing temperatures and longer times. The formation and growth of fluorine bubbles at the poly-Si/Si interface possibly acted as a source of point defects.
4) In diodes from Si-B sources, the [I] could be generated by wet oxidation of the Si-B layer. Because the interfacial oxide effectively acted as a diffusion barrier to injection of interstitial into the Si substrate. The diffusion of boron in the poly-Si/Si was obviously not affected by wet oxidation of the Si-B layer at annealing temperatures below 950°C. As annealing temperature rose above 950°C, the diffusivity of boron was enhanced by the break-up of interfacial oxide.

These results indicate that the fluorine atoms play an important role in creating deeper junctions in diodes from BF_2^+ source. In contrast, the much shallower junctions depth in diodes from Si-B sources was attributed to smaller surface concentrations and boron diffusivity.

B. Electrical Characteristics

The electrical characteristics of poly-Si contacted diodes from Si-B sources were also studied. For comparison, poly-Si contacted diodes from both sources were driven-in at 900°C for 30 min. As shown in Fig. 1(b), the junction in diodes from Si-B source were much shallower than those in diodes from BF_2^+ source. The XTEM micrograph revealed that epitaxial regrowth of poly-Si film does not occur in Si-B-source diodes. In contrast, poly-Si films were epitaxially aligned with silicon substrates in BF_2^+-source diodes. Fig. 6(a) and 6(b) shows the forward and reverse *I–V* characteristics of poly-Si contacted diodes from both sources. It can be seen that the Si-B-source diodes had more ideal *I–V* characteristics than the BF_2^+-source diodes. The ideality factor of Si-B-source diodes was better than 1.01 over 8 decades. The saturation current density J_o was found to be 6.53×10^{-12} and 3.5×10^{-12} A/cm² for BF_2^+- and Si-B-sources diodes, respectively. The larger J_o for BF_2^+-source diodes was due to the increasing of recombination velocity of minority carriers at the poly-Si/Si interface caused by the presence of fluorine bubbles. At high current levels, BF_2^+-source diodes had a smaller forward current and a larger series resistance than Si-B-source diodes. The larger series resistance for BF_2^+-source diodes could be caused by the

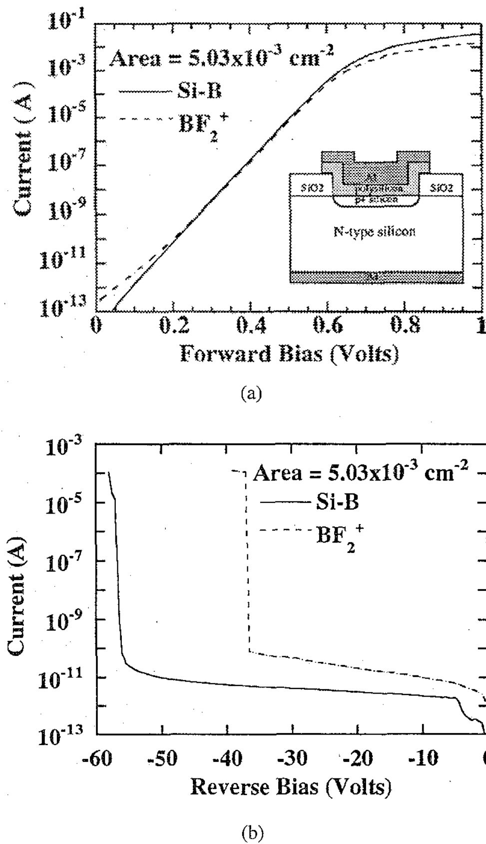


Fig. 6. The typical (a) forward, and (b) reverse I–V characteristics of Si-B- and BF_2^+-source diodes. The cross-sectional structure of poly-Si contacted diode is shown in the inset.

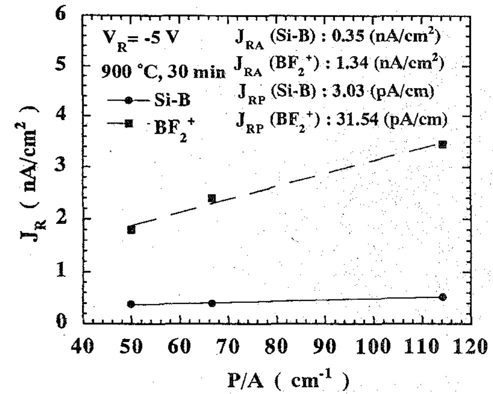


Fig. 7. J_R plotted against the P/A ratio of diodes driven-in at 900°C, where J_R is the reverse current density of diodes measured at −5 V.

deeper junctions, the smaller poly-Si grain size [8], and the presence of fluorine bubbles at the poly-Si/Si interface.

In the reverse-bias region, the Si-B-source diodes had a reverse current density of less than 0.5 nA/cm^2 at −5 V, and a kink in the reverse current. Moreover, the reverse current was nearly independent of the reverse voltage in the range of −5 to −50 V. In contrast, the BF_2^+-source diodes had a large reverse current. From the Arrhenius plots of $\log_e(I_R/T^3)$ versus $1/T$ for the reverse currents, we found that the reverse current mechanism at room temperature was dominated by generation current in diodes from both sources. The kink in the reverse current was considered to be field-induced surface-generation current [20]. The surface-generation current is written as:

$$I_{gen,\,s} = \tfrac{1}{2}\left(qn_i s_o A_s\right) \tag{2}$$

where A_s is area where of poly-Si overlays the field oxide, $s_o \equiv \sigma v_{th} N_{st}$ is the surface recombination velocity, N_{st} is the density of surface recombination-generation centers, and σ is the capture cross-section. When the surface under field oxide is inverted, the surface generation current will be independent of the reverse voltage.

The reverse leakage current J_R can be separated into two components; the area component J_{RA} (nA/cm^2) and the periphery component J_{RP} (nA/cm)

$$J_R = J_{RA} + \frac{P}{A} \cdot J_{RP} \tag{3}$$

where A is the diode area and P is the diode perimeter length. Fig. 7 shows the plots of J_R versus the P/A ratio for diodes from both sources, where J_R is the reverse-current density measured at −5 V. The values of J_{RA} and J_{RP} derived from these plots are also shown in Fig. 7. It can be seen that the values of J_{RA} and J_{RP} for Si-B-source diodes were much smaller than that of the BF_2^+-source diodes. The larger J_{RA} and J_{RP} for BF_2^+-source diodes was due to a less uniform junction caused by the epitaxial regrowth of poly-Si films, the faster diffusion of boron, and the implantation effects. These results demonstrate that a more uniform junction can be obtained by using an Si-B layer as a diffusion source.

Fig. 8(a) shows the leakage current distribution histogram plot for diodes from both diffusion sources. The histogram was made by measuring at least 30 diodes. The value of leakage current for Si-B-source diodes was concentrated around 0.1 and 0.5 nA/cm^2. However, a larger fluctuation of leakage current distribution was obtained for BF_2^+-source diodes. This is explained by the less uniform junction of BF_2^+-source diodes. Fig. 8(b) shows the breakdown voltage distribution histogram for Si-B- and BF_2^+-source diodes. All diodes exhibited hard breakdown behavior, and the breakdown voltages range from −5 to −60 V. From the preliminary data, it would appear that the breakdown voltage of Si-B-source diode is higher than that of BF_2^+-source diodes. Uniform shallow junctions in Si-B source-diode lead to a reduction in the electrical field at the corners of the junctions and a higher breakdown voltage. These results demonstrate that the electrical characteristics and the uniformity of Si-B-source diodes are better than that of conventional BF_2^+-source diodes.

Fig. 9 shows the reverse leakage current density (J_R) at −5 V plots and the forward ideality factor versus the annealing temperatures Fig. 9(a) and times Fig. 9(b) for the Si-B-source diodes. From Figs. 9(a) and (b) and 2(a) and (b), we can see that the diodes with junction depths above 500 Å exhibited a forward ideality factor of better than 1.01 and reverse current density lower than 0.5 nA/cm^2. As the junction

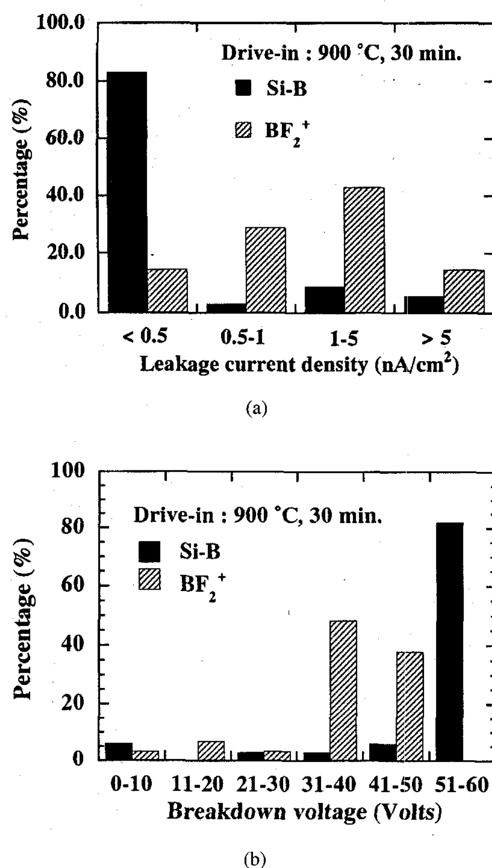


Fig. 8. (a) Histogram plot of leakage current density distribution for Si-B- and BF_2^+-source diodes. (b) Histogram plot of breakdown voltage distribution for Si-B- and BF_2^+-source diodes.

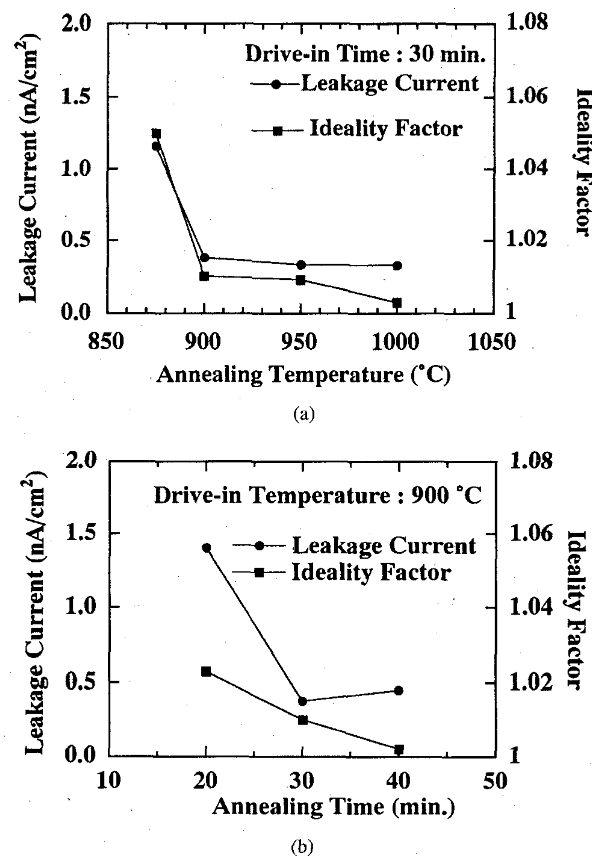


Fig. 9. Plots of the reverse leakage current density (J_R) at −5 V and the forward ideality factor against (a) annealing temperatures, and (b) annealing times for Si-B-source diodes.

depth shrank to 300 Å, the ideality factor and reverse current density increased slightly to 1.05 and 1.16 nA/cm^2 (875°C, 30 min), respectively. The increase in reverse current was caused by an increase in periphery current.

IV. Conclusions

In this paper, we have presented a report on the high-performance poly-Si contacted p^+-n shallow-junction made using an Si-B layer as a diffusion source. The advantages of using the Si-B source are as follows:

1) The deposition temperature of the Si-B layer is low.
2) A high throughput can be obtained with a multi-wafer UHV/CVD system.
3) Si-B-source diodes have much shallower junctions that are less sensitive to the thermal budget than conventional BF_2^+-source diodes.
4) A large poly-Si grain size can be obtained from Si-B source.
5) The I–V characteristics and uniformity of Si-B-source diodes are better than conventional BF_2^+-source diodes. This is considered to be a more uniform junction for the Si-B source.
6) The diodes with a junction depth above 500 Å exhibited a forward ideality factor better than 1.01 and reverse current density lower than 0.5 nA/cm^2 at −5 V. As the junction depth shrank to 300 Å, the ideality factor and reverse current density of diodes increased slightly to 1.05 and 1.16 nA/cm^2.

These results demonstrate that a high-performance poly-Si contacted p^+-n ultra-shallow junction can be obtained by using an Si-B layer as a diffusion source.

References

[1] M. H. El-Diwany, M. P. Brassington, P. Tuntasood, R. R. Razouk, and M. W. Poulyer, "Use of the polysilicon gate layer for local interconnect in a CMOS technology incorporating LDD structures," *IEEE Trans. Electron Devices,* vol. 35, p. 1556, 1988.

[2] G. L. Patton, J. C. Bravman, and J. D. Plummer, "Physics, technology, and modeling of polysilicon emitter contacts for VLSI bipolar transistors," *IEEE Trans. Electron Devices,* vol. ED-33, p. 1754, 1986.

[3] T. Kamins, *Polycrystalline Silicon for Integrated Circuit Applications.* Boston: Kluwer, 1988.

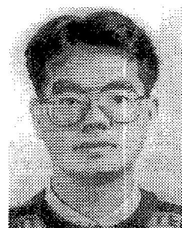
[4] A. K. Kapoor and D. J. Roulston, Eds., *Polysilicon Emitter Bipolar Transistors.* New York: IEEE Press, 1989.

[5] I. R. C. Post and P. Ashburn, "Investigation of boron diffusion in polysilicon and its application to the design of p-n-p polysilicon emitter bipolar transistor with shallow emitter junctions," *IEEE Trans. Electron Devices,* vol. 38, p. 2442, 1991.

[6] S. L. Wu, C. L. Lee, T. F. Lei, and H.-C. Chang, "Characteristics of polysilicon contacted shallow junction diode formed with a stacked-amorphous-silicon film," *IEEE Trans. Electron Devices,* vol. 40, p. 1797, 1993.

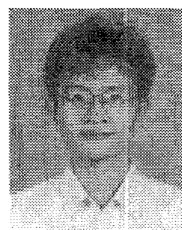
[7] S. L. Wu, C. L. Lee, T. F. Lei, C. F. Chen, L. J. Chen, K. Z. Ho, and Y. C. Ling, "Enhancement of oxide break-up by implantation of fluorine in the poly-Si emitter contacted p^+-n shallow junction formation," *IEEE Electron Devices Lett.*, vol. 15, p. 120, 1994.
[8] T. P. Chen, T. F. Lei, H. C. Lin, and C. Y. Chang, "Characteristics of boron diffusion in the polysilicon/silicon with a thin Si-B layer as diffusion sources," *J. Electrochem. Soc.*, vol. 142, p. 532, 1995.
[9] J. N. Burghartz, J. Y. C. Sun, C. L. Stanis, S. R. M. Ader, and D. Warnock, "Identification of perimeter depletion and emitter plug effects in deep-submicrometer, shallow-junction polysilicon emitter bipolar transistors," *IEEE Trans. Electron Devices*, vol. 39, p. 1447, 1992.
[10] J. D. Williams and P. Asburn, "Epitaxial regrowth of n^+ and p^+ polycrystalline silicon layer given single and double diffusions," *J. Appl. Phys.*, vol. 72, p. 3169, 1992.
[11] T. P. Chen, T. F. Lei, C. Y. Chang, W. Y. Hsieh, and L. J. Chen, "Investigation on the distribution of fluorine and boron in polycrystalline silicon/silicon systems," *J. Electrochem. Soc.*, vol. 142, p. 2000, 1995.
[12] J. S. Hamel, D. J. Roulston, and C. R. Selvakumar, "Trade-off between emitter resistance and current gain in polysilicon emitter bipolar transistors with intentionally grown interfacial oxide layers," *IEEE Electron Device Lett.*, vol. 13, p. 1332, 1992.
[13] H. Schaber, R. V. Criegen, and I. Weitiel, "Analysis of polycrystalline silicon diffusion sources by secondary ion mass spectrometry," *J. Appl. Phys.*, vol. 58, p. 4036, 1985.
[14] B. Garben, W. A. Orr-Arienzo, and R. L. Lever, "Investigation of boron diffusion from polycrystalline silicon," *J. Electrochem. Soc.*, vol. 133, p. 2152, 1986.
[15] T. P. Chen, T. F. Lei, H. C. Lin, C. Y. Chang, W. Y. Hsieh, and L. J. Chen, "Low-temperature growth of Si-B layer by ultra high vacuum chemical deposition," *Appl. Phys. Lett.*, vol. 64, p. 1853, 1994.
[16] F. Lau, "Modeling of polysilicon diffusion sources," *IEDM Tech. Dig.*, p. 737, 1990.
[17] S. F. Guo, "A simple model for the diffusion of boron in silicon by using a BN diffusion source," *J. Electrochem. Soc.*, vol. 127, p. 2506, 1980.
[18] D. A. Antoniadis, A. G. Gonzalez, and R. W. Dutton, "Boron in near-intrinsic ⟨100⟩ and ⟨111⟩ silicon under inert and oxidizing ambient-diffusion and segregation," *J. Electrochem. Soc.*, vol. 125, p. 813, 1978.
[19] A. Berthold, A. V. Felde, M. Biebl, and H. V. Philipsborn, "The role of point defect sources in the formation of boron polyemitters," *IEDM Tech. Dig.*, p. 509, 1994.
[20] A. S. Grove, *Physics and Technology of Semiconductor Devices.* New York: Wiley, 1967.

Tan Fu Lei, for a photograph and biography, see p. 1246 of the July issue of this TRANSACTIONS.



Tung Po Chen was born in Nan-Tou, Taiwan, R.O.C., on August 25, 1967. He received the B.S. degree in physics from the Tunghai University, Taichung, Taiwan, in 1989, the M.S. degree in electrophysics and the Ph.D. degrees in electrical engineering from the National Chiao Tung University, Hsinchu, Taiwan, in 1991 and 1995, respectively. His research for the doctoral dissertation was on the growth of Si-B layer for ULSI application.

He joined the United Microelectronics Corporation (UMC), Hsinchu, Taiwan, in September 1995.



Horng-Chih Lin (S'91–M'95) was born in I-Lan, Taiwan, R.O.C., on August 1, 1967. He received the B.S. degree in physics from Central University, Chung-Li, Taiwan, in 1989, and the Ph.D. degree in Institute of Electronics from National Chiao-Tung University, Hsinchu, Taiwan, in 1994.

In 1994, he joined the National Nano Device Laboratory, Hsinchu, Taiwan, as an Associate Researcher. His current research interests include fabrication and characterization of polycrystalline thin transistors, plasma etching, and reliability of CMOS devices.

Chun-Yen Chang (S'69–M'70–SM'81–F'88), for a photograph and biography, see p. 1509 of the August issue of this TRANSACTIONS.