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A Novel Cost Effective Double Reduced Surface Field Laterally Diffused Metal Oxide Semiconductor Design for Improving Off-State Breakdown Voltage

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In this work, double reduced surface field (RESURF) laterally diffused metal oxide semiconductor (LDMOS) device combines a new implant technology without using additional mask in standard 0.18 μm technology has been proposed and successfully fabricated. The breakdown voltage (BV) can be improved significantly with simply changing the implanted region length in this implant technology. Firstly, hydrodynamic transport simulations which analyze the high bias condition electric field distributions are examined to predict and explain the increase of breakdown voltage. Then the fabricated devices process flow is demonstrated, the structures are performed, and the breakdown voltages increase with different n-type double diffusion (NDD) photoresistor (PR) size using the change of PR exposure dose are investigated. The measurement results show that maximum NDD PR size achieves BV improvement of 6.3%, and 5% increase of figure of merit (FOM) evaluation. Throughout the whole fabrication process, no additional mask and device area show the potential of cost effective with the proposed technique. Such devices with good off-state breakdown voltage and specific on-resistance are very competitive with similar technologies and show good promising in system on chip (SOC) applications.

1. Introduction

Recently, complementary metal–oxide–semiconductor (CMOS) technology which integrates logic circuit, radio frequency (RF) circuit and power switch on the same chip require the power devices with reduction of specific on-resistance ($R_{on,sp}$), improvement of breakdown voltage (BV) and current driving capability. The development of suitable power devices using CMOS is necessary to achieve its goal for system on chip (SOC) realization,[1–11] particularly in the low voltage range such as 30 V rating for RF wireless system, display driver, and DC–DC converter applications.[12–17,24–28] Laterally diffused metal oxide semiconductor (LDMOS) with double reduced surface field (RESURF) technology using low thickness of epitaxial layer or n-well implant has utilized for designing high-voltage devices with a low $R_{on,sp}$.[18–23] Many studies show that high breakdown voltages can be maintained, while drift region doping concentration is increased by twice as much as that in single RESURF devices realizing a good trade-off between off-state BV and $R_{on,sp}$.[18–23] In addition, there were many studies improve characteristics of lateral devices with CMOS-compatible process including silicon-on-insulator (SOI)[26–28] and bipolar CMOS (BiCMOS)[29,30] technologies; they still remain additional mask design, complex processes and device area, which increase the cost of fabrication.[24–30]

In this work, we propose a novel p-buried layer implant methodology in double RESURF LDMOS devices to improve off-state breakdown voltage and attain low specific on-resistance without adding any new hard mask in standard 0.18 μm CMOS technology, the characteristics increase with the lengths of photo resistor (PR) are explored and discussed. The paper is organized as follows. In §2, we describe the simulation technique and study the simulation results. In §3, we show the device structure and fabrication process flow. In §4, we examine the breakdown voltage and specific on-resistance with different length of p-buried region. Finally, we draw conclusions and suggest future work.

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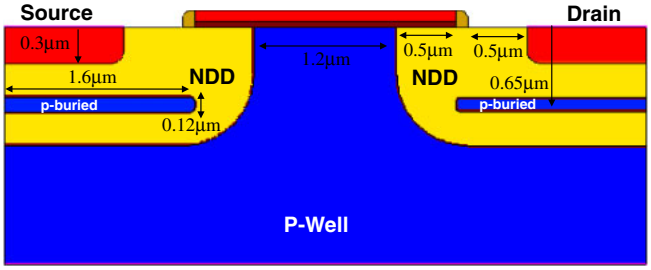

Fig. 1. (Color online) The simulated high-voltage NMOS device structure, the size of channel, source, drain, NDD, and p-buried region are indicated.

2. Numerical Simulation

The n-type MOS device structure in our simulation is shown in Fig. 1. The p-well doping concentration of the explored devices is 1×10^{17} cm^{-3}. Outside the channel, the doping concentrations in the source, drain and poly-gate are all 1×10^{20} cm^{-3}. The n-type double diffusion (NDD) doping concentration in the drift region is 1×10^{17} cm^{-3}. They have a 1.2 μm effective channel length, a gate oxide thickness of 45 nm, 300 nm source/drain junction depths, and NDD depth of 1 μm. The p-buried implant layer length, depth, and thickness are 1.6 μm, 0.65 μm, and 120 nm, respectively. To accurately examine the numerical results with high voltage condition, device simulation is performed by solving hydrodynamic transport equation coupled with drift-diffusion equations[31–33] using commercial tool Synopsys DESSIS.[34] Figures 2(a) and 2(b) show the potential and electric field distributions in the device at the bias condition $V_g = 0$ V and $V_d = 25$ V. Due to the different type of p-buried implant introduces additional negative charges and divides the NDD drift region into two parallel conduction path, the electric field near channel surface and NDD drift region edge are reduced significantly, and produce an uniform distribution of potential, which are beneficial for impact ionization reduction and result in the improvement of breakdown voltage. Figure 3 compares the drain-voltage/drain-current (I_d–V_d)

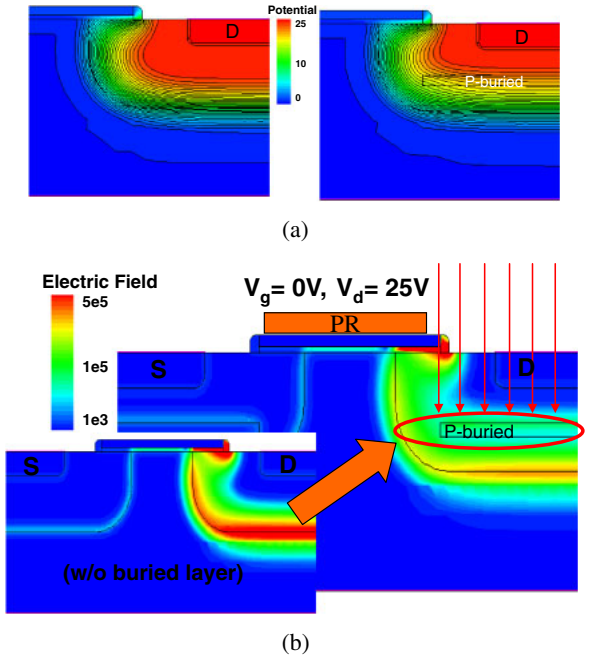

Fig. 2. (Color online) The simulated (a) potential and (b) electric field distributions with and without p-buried layer at bias condition $V_g = 0$ V and $V_d = 25$ V, the potential in the device with p-buried implant becomes more uniform and electric field is significantly reduced.

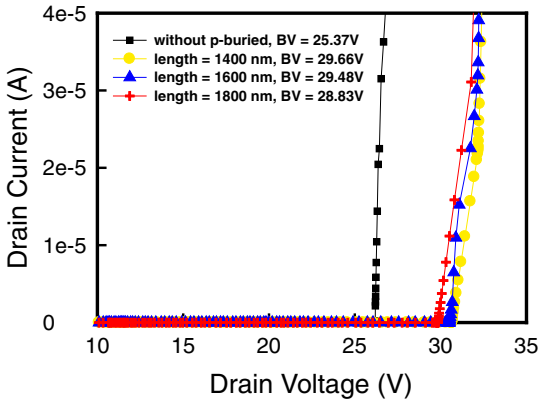

Fig. 3. (Color online) The simulated I–V curves with different p-buried layer length.

characteristics of devices with different p-buried layer length, by calculation of Poisson's equation with full depletion condition, optimized dose and energy is very important to provide better on-resistance and breakdown voltage.[18–23] Moreover, changing the length of p-buried layer also introduce different number of negative charges, which can control and optimize the device breakdown voltage.

3. Device Structure and Fabrication

In this section, the device fabrication process flow and structure are demonstrated. Our LDMOS transistor fabrication process of defining p-buried layer is based on a 0.18 µm high voltage (HV) CMOS technology developed by Vanguard International Semiconductor Corporation without any additional masks. The HV LDMOS with different photoresistor length and conventional devices without p-buried

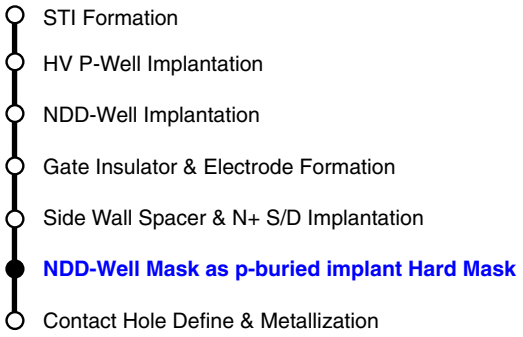

Fig. 4. (Color online) The fabrication process flow of standard 0.18 µm LDMOS device. To implement p-buried layer, we use an additional implant process with old NDD mask before metallization.

layer are both available in this technology. Fabrication process flow is shown in Fig. 4. The starting wafer is a (100) oriented p-type wafer with doping concentration of 1×10^{15} cm^{-3}, and the fabrication process begins with active region defined and is followed by shallow trench isolation (STI) formation. Subsequently, HV p-well ion implantations are performed. Owing to the RESURF conditions,[18–23] total charges in drift region require accurate charge control and sensitive to charge balance, careful control of dose and junction depth is essential. Therefore, the NDD ion implantation in drift region is carried out after the p-well drive-in. Gate lithography and etch, gate oxidation, polycrystalline silicon (poly-Si) deposition, poly-silicon gate etch, and doping annealing are then carried out to form the gate electrode. Then nitride spacer side wall and source/drain annealing are performed. The old mask of NDD with PR is adopted to form the different p-buried layer length with boron ion implantation. The p-buried dose of 1×10^{12} cm^{-2} at 210 keV are served as double RESURF conditions.[19] A thick inter level oxide deposition of tetraethylsilane (TEOS) is followed by contact lithography and oxide etching to form the contact window. Finally, metallization and passivation are carried out to complete the LDMOS transistor fabrication sequence. Figures 5(a) and 5(b) present the layout design, cross-section and secondary ion mass spectrometry (SIMS) profile in the drift region of the conventional LDMOS. The thickness of gate oxide is 45 nm. The width and effective channel length are 20 and 1.2 µm. The doping concentration of NDD is about 1×10^{17} cm^{-3}. Figure 6(a) shows the cross-section LDMOS with p-buried layer and Fig. 6(b) shows the top-view scanning electron microscope (SEM) image of device with maximum NDD PR length. The side wall spacer, gate and PR lengths can be observed and their sizes are about 100 nm, 2.6 µm and 1.4 µm, respectively.

4. Results and Discussion

To investigate the effect of p-buried implant layer length, we use different PR exposure dose to control the PR length with the same hard mask. As the size of PR is increased, the length of p-buried layer decreases. Figure 7(a) displays the measured off-state ($V_g = 0$ V) characteristic of the LDMOS transistor with different PR length. The PR length of standard conventional device is served as the reference. The result shows the longer NDD PR length (shorter p-buried layer length) perform the better off-state breakdown

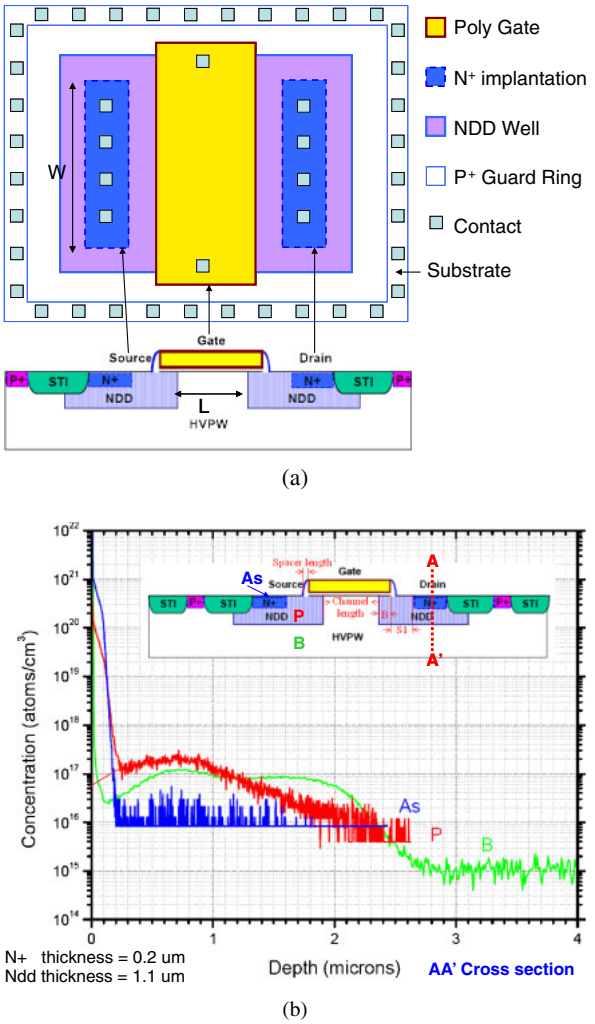

Fig. 5. (Color online) (a) The layout design and cross-section of our conventional LDMOS and (b) The SIMS profile of drift region.

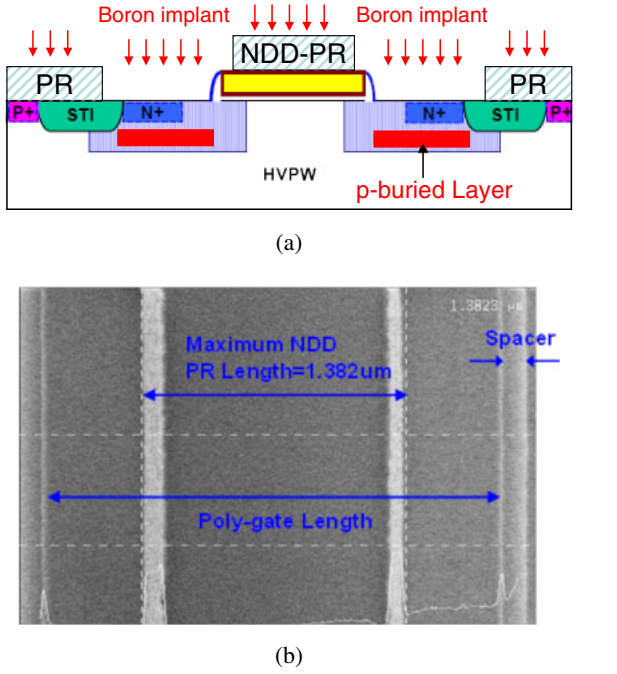

Fig. 6. (Color online) (a) Cross section LDMOS with p-buried implant layer. (b) Top view SEM image of the maximum NDD PR length.

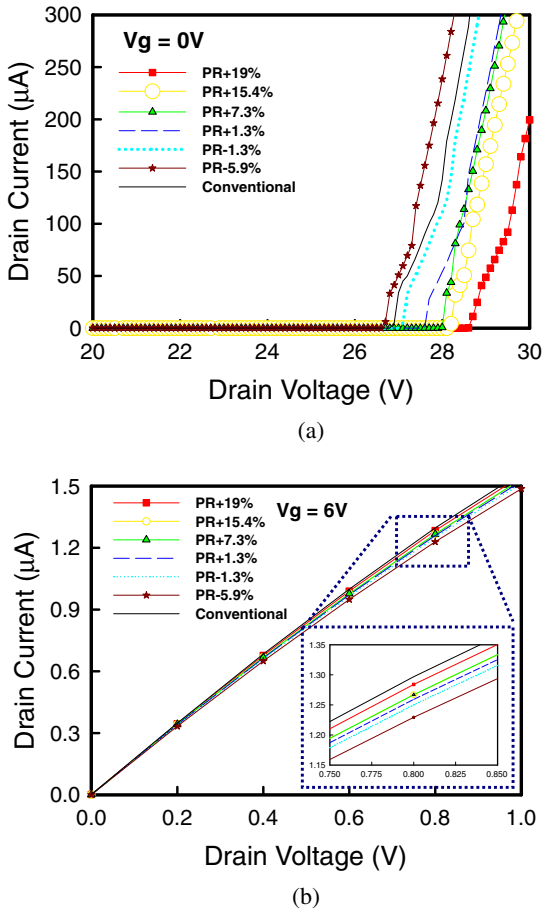

Fig. 7. (Color online) Measured (a) off-state ($V_g = 0\,V$) and (b) on-state ($V_g = 6\,V$) I–V characteristic of the LDMOS with different PR length.

voltage in our implant condition. The breakdown voltage improves 6.3% compare with conventional LDMOS. The double RESURF is an effective way to balance the electric field in the NDD region than single RESURF methodology and therefore the breakdown voltage can be improved. Using NDD-Well PR served as the hard mask of p-buried layer is a good way to reduce the fabrication cost. However, for longer p-buried layer length, the followed annealing temperature such like silicide or other high temperature processes will result in the dramatically diffusion of p-buried layer toward the channel. The p-buried layer will easily connect with HV p-well to degrade the breakdown voltage. Hence, the PR exposure dose and time control affect the PR length and electrical characteristics. Figure 7(b) shows the comparison of on-state ($V_g = 6\,V$) characteristics of LDMOS with different PR size. The results shows the longer NDD PR length perform the better the $R_{on,sp}$ of the double RESURF devices. The larger p-buried layer length introduces more holes in the electron conduction path which degrades the on-resistance. The comprehensive comparison of electrical characteristics is summarized in the Table I. The figure of merit (FOM) which defined by $BV/R_{on,sp}$ is addressed for device efficiency evaluation. The best FOM of our devices is 2.07, which has 5% improvement compare to the conventional device. Figure 8 compares the $R_{on,sp}$ vs BV of several LDMOSs in recent years,[13–17] in which the devices in literatures provide various rated of breakdown voltage. It is a

Table I. Summary of devices electrical characteristics for different NDD PR length. The BV and $R_{on,sp}$ are extracted from forward sweeping I_d–V_d curves at $V_g = 0$ V, $I_d = 1$ μA and $V_g = 6$ V, $V_d = 0.1$ V shown in Figs. 6 and 7.

LDMOS	NDD-PR length (μm)	$R_{on,sp}$ at $V_d = 0.1$ V (mΩ mm^2)	BV at $I_d = 1$ μA (V)	BV improvement (%)	FOM (BV/$R_{on,sp}$)
PR + 19%	1.382	13.89	28.71	6.33	2.07
PR + 15.4%	1.320	14.00	28.20	4.44	2.01
PR + 7.3%	1.229	13.99	28.00	3.70	2.00
PR + 1.3%	1.160	14.09	27.61	2.26	1.96
PR − 1.3%	1.126	14.18	27.05	0.19	1.91
PR − 5.6%	1.078	14.40	26.61	−1.44	1.85
Conventional[a)]	1.145	13.80	27.00	0.00	1.96

a) No p-buried layer.

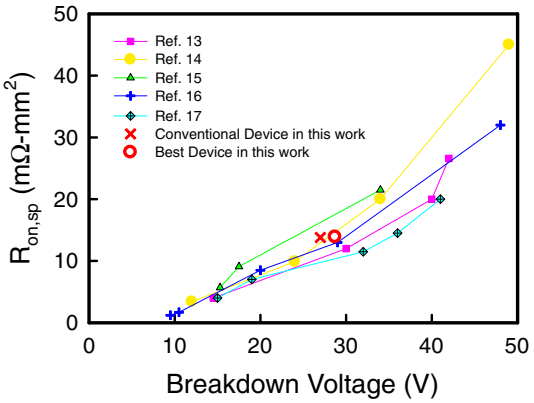

Fig. 8. (Color online) Comparison of $R_{on,sp}$ vs BV between our devices and similar technologies.

trade-off between breakdown voltage and specific on-resistance. The devices in this work show competitive with respect to similar technologies and device with maximum NDD PR size improve BV significantly which maintain the similar $R_{on,sp}$.

5. Conclusions and Future Work

Double RESURF LDMOS device combine with a new p-buried layer implant in standard 0.18 μm technology has been proposed and successfully demonstrated. The fabricated device of maximum NDD PR size achieves BV improvement of 6.3% and maintain the similar $R_{on,sp}$ by simply changing the PR exposure dose. Throughout the whole fabrication process, no additional mask and device area are required. Our devices which have good off-state BV and $R_{on,sp}$ show promising potential for SOC applications. We are currently working on studying the depth effects of p-buried layer, which may further improve and optimize the device characteristics.

Acknowledgments

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