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Flexible One Diode–One Resistor Crossbar Resistive-Switching Memory

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We report the first demonstration of a flexible one diode–one resistor (1D1R) resistive-switching (RS) memory cell capable of high-density crossbar array implementation at an extremely low cost. A Ti/TiO_2/Pt diode with a large rectifying ratio and a stable Ni/HfO_2/Pt unipolar RS memory element have been fabricated on a polyimide substrate using only room-temperature processes. No significant degradation of the rectifying ratio of the TiO_2 diode and the cycling variations, retention, and read disturb immunity of the HfO_2 memory was observed in the bending state. The series 1D1R cell shows highly reproducible unipolar RS because of the low reset current of the HfO_2 memory, which greatly mitigates the adverse effect of diode series resistance. Furthermore, the 1D1R cell can effectively suppress read interference and realize a crossbar array as large as 512 kbit.

1. Introduction

Flexible electronics have received increasing attention because of their advantages of low cost, light weight, flexibility, and capability of large-area process. However, traditional Si technology requiring high-temperature processes is incompatible with the low glass transition temperature of flexible substrates. In contrast, oxide-based materials deposited at a low temperature have shown promising characteristics for flexible electronics applications, such as indium–gallium–zinc oxide for thin-film transistors in the flexible active matrix backplane.[1)] To realize another fundamental building block of flexible electronics, namely, nonvolatile memory, considerable efforts are being made to develop resistive-switching random access memory (RRAM) on flexible substrates, exploiting the nonvolatile variable resistance in transition metal oxides.[2–4)] In addition to its superior memory characteristics, RRAM is highly attractive for flexible nonvolatile memory because of its simple crossbar architecture and low-temperature fabrication.[5)] However, a passive crossbar array is known to suffer from the so-called sneak current problem, and thus it is difficult to scale up beyond 64 bits because of severe read interference.[6,7)] The development of low-temperature selection devices in series with resistive-switching (RS) memory elements on flexible substrates is critical, but significantly less emphasized. Recently, we have successfully demonstrated the fabrication of both RS memories and rectifying oxide diodes on Si substrates at room temperature.[8,9)] The TiO_2-based metal–insulator–metal (MIM) devices with a Pt bottom electrode exhibited excellent rectifying, bipolar RS, and unipolar RS characteristics, which were realized by choosing appropriate top-electrode materials. The rectifying oxide diode is applicable to the compact one diode–one resistor (1D1R) crossbar architecture, which suppresses read interference in high-density memory arrays.[10–12)] In comparison with the conventional one transistor–one resistor (1T1R) architecture, 1D1R with a $4F^2$ unit cell size not only significantly increases bit density, but also enables a simple implementation of the low-temperature and low-cost flexible memory.

In this study, we fabricated 1D1R memory cells, consisting of a Ti/TiO_2/Pt diode element and two different types of RS memory elements, namely, Pt/TiO_2/Pt and Ni/HfO_2/Pt. The TiO_2-based diode and RS element are interesting because of their potential for a monolithic TiO_2 1D1R cell, but a high reset current (I_{RESET}) of the TiO_2 RS element (over 10 mA) led to unstable unipolar RS in the 1D1R cell. On the other hand, when the TiO_2-based diode was integrated with the HfO_2 RS element with a low I_{RESET} (less than 1 mA), stable unipolar RS characteristics can be realized. Additionally, the excellent rectifying characteristics with a high resistance ratio at reverse and forward biases enabled the realization of a compact 512 kilobit (kb) crossbar memory array with an at least 10% readout margin. Because the entire device fabrication was completed at room temperature, the proposed 1D1R cell was successfully fabricated on a polyimide (PI) substrate and was found to be promising for flexible and high-density memory applications using roll-to-roll processing at an extremely low cost in the future.

2. Experimental Procedure

Prior to the device fabrication, 75-μm-thick Kapton® polyimide (PI) substrates were cut and ultrasonically cleaned in acetone for 10 min to remove particles and contamination, followed by baking at 100 °C for 30 min. The cleaned PI substrates were then electrostatically attached to silicon wafers. Because the PI substrate is susceptible to water absorption, a buffer layer of SiO_2 with a thickness of 300 nm was deposited by plasma-enhanced chemical vapor deposition (PECVD). Platinum bottom electrodes of 80 nm with a thin Ti adhesion layer were deposited onto substrates by electron beam evaporation. To fabricate the TiO_2 oxide diode and RS memory element, the TiO_2 active layers with a thickness of 50 nm were deposited by electron beam evaporation at room temperature, and then 100-nm-thick Ti and Pt top electrodes with an area of 10^4 μm^2 were patterned using a shadow-mask technique for the Ti/TiO_2/Pt diode and the Pt/TiO_2/Pt RS element, respectively. To fabricate the HfO_2 RS memory element, HfO_2 active layers with a thickness of 80 nm were prepared by dc magnetron reactive sputtering using a Hf target (99.5%) in a mixture of Ar and O_2 at room temperature, and then 100-nm-thick Ni top electrodes with an area of 10^4 μm^2 were patterned using a shadow-mask technique for the Ni/HfO_2/Pt RS element. All devices reported in this study were fabricated completely at room temperature without any

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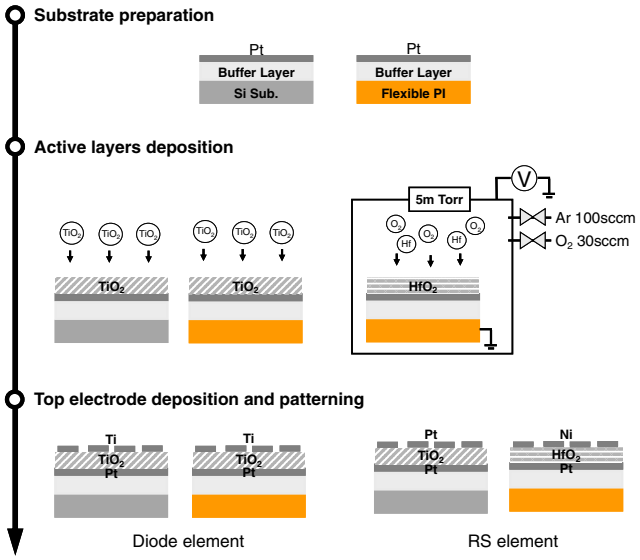

Fig. 1. (Color online) Fabrication of $Ti/TiO_2/Pt$, $Pt/TiO_2/Pt$, and $Ni/HfO_2/Pt$ devices on PI and silicon substrates.

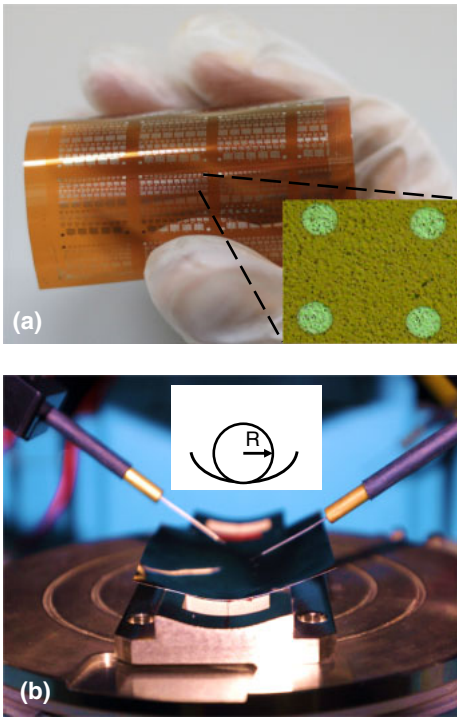

Fig. 2. (Color online) (a) Photograph of a fabricated flexible device under bending condition. The insert shows the microscope image of the device on the PI substrate. (b) Measurement setup using a concave stage with a radius of 30 mm to characterize devices in the bending state.

additional thermal treatment. In addition to the flexible devices, conventional devices on silicon substrates were also prepared using the same process. The detailed process flow is shown in Fig. 1. Figure 2(a) shows a photograph of a fabricated flexible device that was highly robust under mechanical strain. Figure 2(b) shows the measurement setup using a concave stage with a radius of 30 mm to characterize

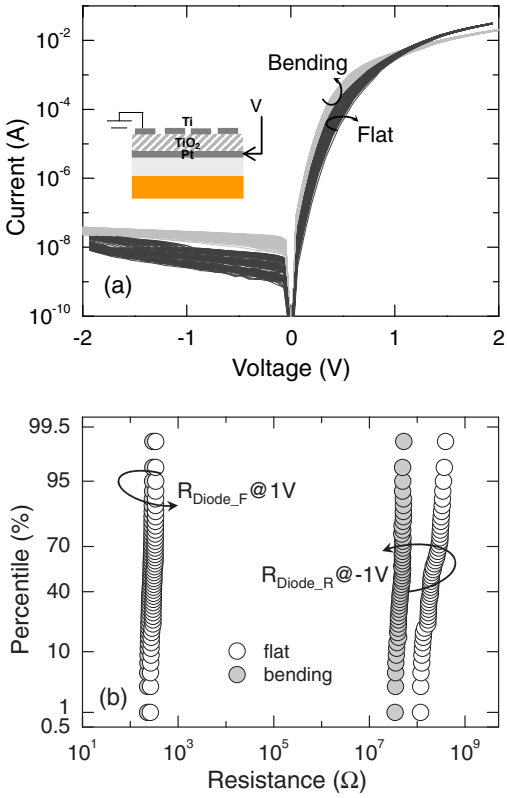

Fig. 3. (Color online) (a) 100 successive ±2 V dc sweeps, and (b) cumulative plot of forward/reverse resistances at 1 V/−1 V of the flexible $Ti/TiO_2/Pt$ diodes in both flat and bending states.

devices in the bending state. All electrical measurements were performed using a HP-4156B semiconductor analyzer. The 1D1R cells were externally connected and voltage was applied to the Ni or Pt top electrode of the RS memory element while the Ti top electrode of the TiO_2 diode element was grounded.

3. Results and Discussion

3.1 $Ti/TiO_2/Pt$ diode

Figure 3 shows the rectifying characteristics of the $Ti/TiO_2/Pt$ diode under both flat and bending conditions. Even though fabricated on the flexible substrate, $Ti/TiO_2/Pt$ diodes exhibit a large rectifying ratio of 10^6 at ±1 V, an ideality factor of 1.2, and a robust endurance up to hundreds of successive DC sweeps without dielectric breakdown. The results are comparable with those of the diodes fabricated on Si,[9] showing a minimal substrate effect. A rectifying ratio of more than 10^5 at ±1 V can be maintained in the bended devices, indicating negligible degradation of the diode characteristics under bending condition. The asymmetry of current–voltage (I–V) curves was explained by the different Schottky barrier heights at the Ti/TiO_2 and the TiO_2/Pt interfaces.[9] When applying a negative voltage to the Pt electrode, electrons were injected from Pt to TiO_2, but encountered a substantial Schottky barrier. When applying a positive voltage to Pt, electrons were injected from Ti to TiO_2. Current increased exponentially with bias voltage and was eventually limited by the smaller barrier at the Ti/TiO_2 interface and parasitic series resistance.

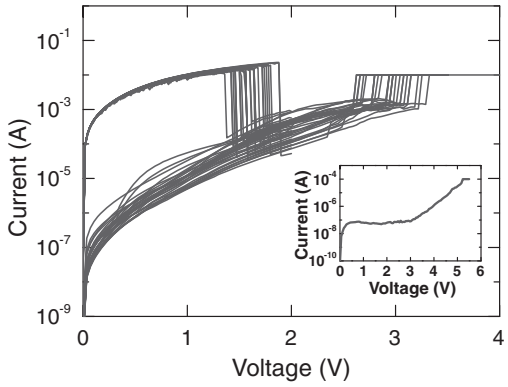

Fig. 4. Typical unipolar RS characteristics of the Pt/TiO_2/Pt memory element with I_{RESET} over 10 mA. Inset shows the typical forming I–V curve with a forming voltage of approximately 5 V.

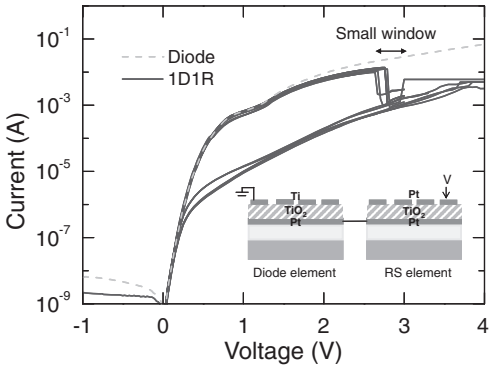

Fig. 5. Unstable unipolar RS in the monolithic TiO_2 1D1R cell because of the small programming margin.

3.2 Pt/TiO_2/Pt RS memory element and monolithic TiO_2 1D1R cell

In contrast to the Ti/TiO_2/Pt bipolar RS memory element,[9] the Pt/TiO_2/Pt RS memory was nonpolar after the initial forming process and applicable to the 1D1R crossbar array utilizing unipolar RS. The oxygen-deficient filament was believed to be responsible for the observed RS.[8] Figure 4 shows the typical unipolar RS curves of the Pt/TiO_2/Pt RS memory for positive SET (V_{SET}) and RESET (V_{RESET}) voltages. Although the unipolar RS was stable, the I_{RESET} was over 10 mA, comparable to the maximum current a TiO_2 diode can provide. The high I_{RESET} not only resulted in excessive switching power undesirable for low-power operation, but also deteriorated the stability of RS in a 1D1R cell. Because of the comparable currents in the diode and RS element, the diode series resistance was not negligible in the 1D1R cell when the RS element was in the low resistance state (LRS). Hence, V_{RESET} significantly increased. In contrast, V_{SET} was less sensitive to diode series resistance because of the considerably larger resistance of the RS element in the high resistance state (HRS). As a result, the programming margin between unipolar V_{SET} and V_{RESET} diminished and unipolar RS became less stable, as shown in Fig. 5, that the TiO_2 1D1R cell exhibits only a few stable switching cycles without programming error. Figure 6 further shows the predicted programming margin as a function of I_{RESET} at a fixed diode on-current of 10 mA. For a RS memory element with V_{RESET} of 0.5 V and V_{SET} between 2 to 4 V considering cycling variations, I_{RESET} below 1 mA would be required for a stable unipolar RS in the 1D1R cells.

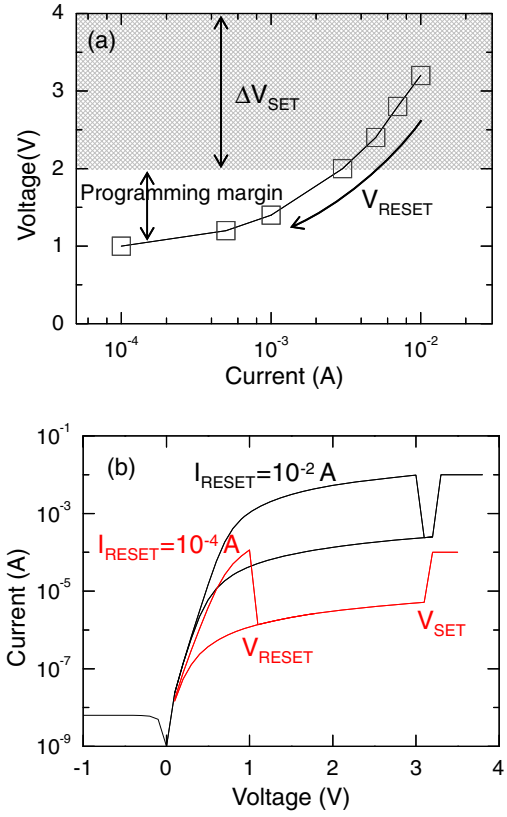

Fig. 6. (Color online) (a) Programming margin of a 1D1R cell as a function of I_{RESET}. The diode on-current was fixed at 10 mA. A R_{HRS}/R_{LRS} ratio of 100, V_{RESET} of 0.5 V, and V_{SET} between 2 to 4 V considering cycling variations were assumed for the RS element. (b) Simulated 1D1R unipolar switching curves for RS elements with I_{RESET} of 0.1 and 10 mA, respectively.

3.3 Ni/HfO_2/Pt RS memory element and heterogeneous HfO_2–TiO_2 1D1R cell

The RS in the Ni/HfO_2/Pt memory fabricated on the flexible PI substrate was also nonpolar after the initial forming process. The RS may be attributed to the formation of Ni filaments through HfO_2 by Ni ion migration from the top electrode after electrical forming, and rupture and connection of Ni filaments by Joule heating and ion migration.[13,14] Other studies suggested a different mechanism by Joule-heat-induced redox of NiO_x at the interface of Ni and HfO_2.[15,16] Further studies in the future are required to clarify the origin of the RS in more detail. The unipolar RS with positive V_{SET} and V_{RESET} was highly reproducible, as shown in Fig. 7(a), with a resistance ratio of HRS to LRS (R_{HRS}/R_{LRS}) of approximately 10^2 and I_{RESET} less than 1 mA even under bending condition. Figure 7(b) shows the cumulative plot of HRS and LRS resistance in both the flat and bending states with markedly tight distributions. Figure 8 shows superior immunity to read disturb and retention characteristics of the HfO_2 RS element regardless of whether the substrate was flat or bended. The reproducible and reliable unipolar RS in the bending state demonstrates

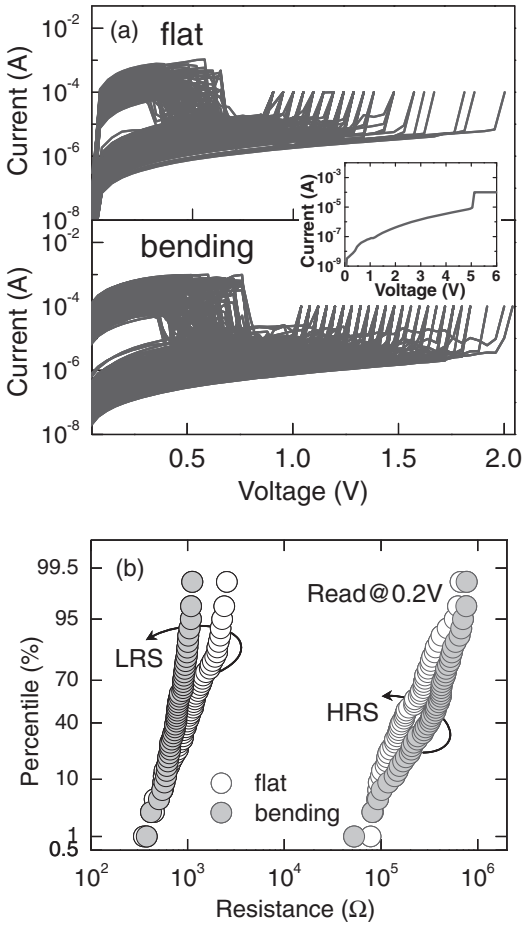

Fig. 7. (a) 100 successive unipolar RS cycles with I_{RESET} less than 1 mA, and (b) cumulative plot of HRS and LRS resistance at 0.2 V of the flexible $Ni/HfO_2/Pt$ memory element in both flat and bending states. Inset in (a) shows the typical forming I–V curve with a forming voltage of approximately 5 V.

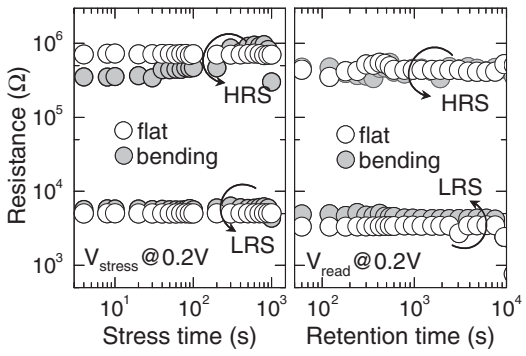

Fig. 8. Read disturb and retention characteristics of the flexible $Ni/HfO_2/Pt$ memory element in both flat and bending states.

the feasibility of RS memory for flexible electronics applications. In Fig. 9, by connecting the HfO_2 RS memory with low I_{RESET} and the TiO_2 diode in series, a highly reproducible unipolar RS with a substantial R_{HRS}/R_{LRS} ratio was realized at a positive bias, whereas the current at a negative bias remained extremely low owing to the reverse-biased diode even when the RS memory was in LRS. The high rectifying ratio shown here is among the best ever

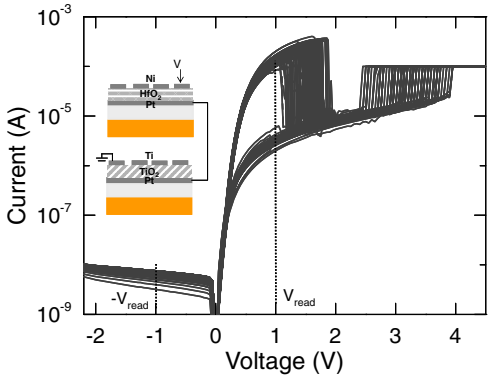

Fig. 9. (Color online) More than 200 successive unipolar RS cycles with a high rectifying ratio at ±1 V in the heterogonous TiO_2–HfO_2 1D1R cell.

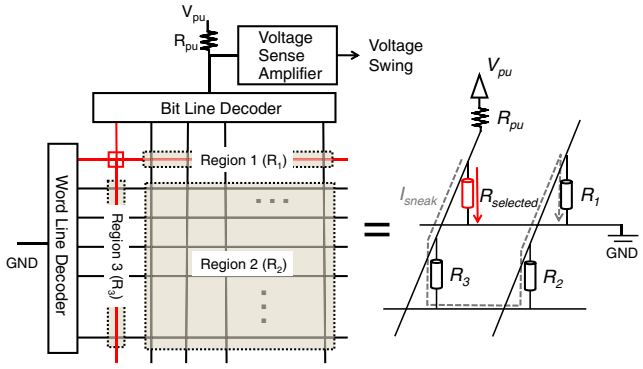

Fig. 10. (Color online) Schematic of an $N \times N$ crossbar memory array and its equivalent circuit in the worse-case read scenario where all unselected cells are in LRS. The sneak current through R_1, R_2, and R_3 results in severe read interference.

reported for 1D1R cells, including those fabricated on Si substrates.[10–12]

3.4 Prediction of read margin in 1D1R crossbar array

In this section, the prediction on the read margin of 1D1R crossbar array is explained using the device parameters extracted from the standalone 1D1R cell in Fig. 9. Figure 10 depicts the equivalent circuit of an $N \times N$ crossbar memory array in the worse-case scenario of read interference where all unselected cells are in LRS.[6,17] Considering a one bit-line pull-up read scheme,[6] the sneak current can flow through the unselected cells, represented by the parallel resistor networks of R_1, R_2, and R_3 in Fig. 10, which leads to read error when the selected cell is in HRS ($R_{selected} = R_{HRS}$). In the 1D1R crossbar array as shown in Fig. 11, R_2 contributed by all unselected cells at unselected word/bit lines in parallel is considerably larger than the sum of R_1 and R_3 because of the reverse biased diodes. Therefore, the resistance in the sneak current path can be approximated by $R_{LRS\_R}/(N-1)^2$, where R_{LRS_R} is the resistance of the standalone 1D1R cell in LRS dominated by the reverse biased diode at the negative read voltage $-V_{read}$, as shown in Fig. 11. R_{LRS_F} and R_{HRS_F} are also defined as the resistances of the standalone 1D1R cell in LRS and HRS, respectively, when read at V_{read}. When $R_{LRS\_R}/(N-1)^2$ decreases as N increases and eventually becomes comparable to R_{LRS_F} of the selected bit, the sneak current begins to

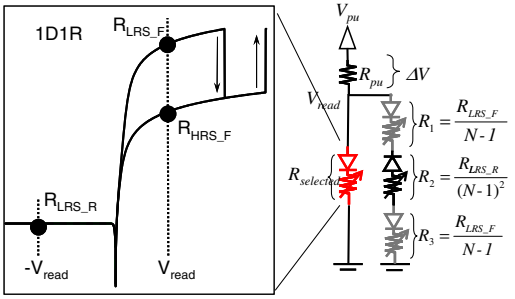

Fig. 11. (Color online) Equivalent circuit of a 1D1R crossbar array at read. The total resistance of the sneak current path is dominated by R_2 because of the reverse-biased diodes.

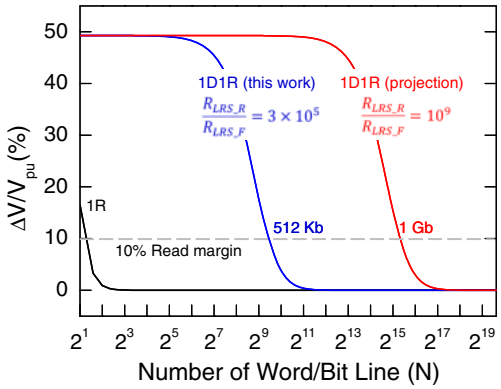

Fig. 12. (Color online) Normalized readout margin $\Delta V/V_{\mathrm{pu}}$ as a function of the number of word/bit lines in an $N \times N$ crossbar array. The maximum allowed array size with an at least 10% readout margin can be markedly increased in 1D1R arrays compared with 1R passive arrays.

interfere with the read process in the large 1D1R array. Thus, the ratio of $R_{\mathrm{LRS\_R}}$ to $R_{\mathrm{LRS\_F}}$ is a good measure of the maximum crossbar array size with a tolerable read margin.

The readout voltage on the pull-up resistor R_{pu} can be calculated when $R_{\mathrm{selected}} = R_{\mathrm{LRS\_F}}$ and $R_{\mathrm{selected}} = R_{\mathrm{HRS\_F}}$, using an equivalent circuit method similar to that applied for a complementary resistive switch (CRS) crossbar array[18] and a one selector–one resistor (1S1R) crossbar array.[19] When R_1 and R_3 are omitted in Fig. 11, the readout voltage swing ΔV normalized to the pull-up voltage V_{pu} can be quantitatively estimated using the resistor voltage divider equation as follows:

$$\frac{\Delta V}{V_{\mathrm{pu}}} = \frac{R_{\mathrm{pu}}}{\left[R_{\mathrm{LRS\_F}} \parallel \frac{R_{\mathrm{LRS\_R}}}{(N-1)^2}\right] + R_{\mathrm{pu}}} - \frac{R_{\mathrm{pu}}}{\left[R_{\mathrm{HRS\_F}} \parallel \frac{R_{\mathrm{LRS\_R}}}{(N-1)^2}\right] + R_{\mathrm{pu}}}, \quad (1)$$

where R_{pu} is set to $R_{\mathrm{LRS\_F}}$ for the maximum read margin. For a 10% readout margin, Fig. 12 shows that the maximum allowed word lines in a square crossbar array increased dramatically from 2 in a passive array to 750, which is equivalent to approximately 512 kb, in a 1D1R array utilizing the parameters extracted from Fig. 9. The 1D1R array can be further scaled up to 1 Gb with an improved $R_{\mathrm{LRS\_R}}/R_{\mathrm{LRS\_F}}$ ratio of 10^9.

4. Conclusions

A rectifying Ti/TiO_2/Pt oxide diode and a unipolar RS Ni/HfO_2/Pt memory element have been fabricated on a flexible PI substrate with excellent characteristics using only room-temperature processes. No significant device degradation was found in the bending state. Additionally, the impact of I_{RESET} on the programming margin of unipolar RS has been examined. The heterogeneous TiO_2–HfO_2 1D1R cell not only demonstrates a more stable unipolar RS than a monolithic TiO_2 1D1R cell because of the lower I_{RESET} in the HfO_2 memory element, but also effectively suppresses the sneak current. The maximum allowed array size with an at least 10% read margin is predicted to exceed 512 kb using a simple equivalent circuit model. Therefore, the proposed 1D1R cell is extremely attractive for implementing high-density nonvolatile memory in future low-cost flexible electronics.

Acknowledgments

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