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Random Interface-Traps-Induced Electrical Characteristic Fluctuation in 16-nm-Gate High-κ/Metal Gate Complementary Metal–Oxide–Semiconductor Device and Inverter Circuit

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This work estimates electrical and transfer-characteristic fluctuations in 16-nm-gate high-κ/metal gate (HKMG) metal–oxide–semiconductor field effect transistor (MOSFET) devices and inverter circuit induced by random interface traps (ITs) at high-κ/silicon interface. Randomly generated devices with two-dimensional (2D) ITs at HfO_2/Si interface are incorporated into quantum-mechanically corrected 3D device simulation. Device characteristics, as influenced by different degrees of fluctuation, are discussed in relation to random ITs near source and drain ends. Owing to a decreasing penetration of electric field from drain to source, the drain induced barrier lowering (DIBL) of the edvice decreases when the number of ITs increases. In contrast to random-dopant fluctuation, the screening effect of device's inversion layer cannot effectively screen potential's variation; thus, devices still have noticeable fluctuation of gate capacitance (C_G) under high gate bias. The cutoff frequency decreases as increasing the number of ITs owing to the decreasing transconductance and increasing C_G. Decreasing on-state current and increasing C_G further result in increasing intrinsic gate delay time (τ) when the number of ITs increases. The fluctuation magnitude of DIBL, cutoff frequency, and τ above is increased as the number of ITs increases. Even for cases with the same number of random ITs, noise margins (NMs) of the 16-nm-gate complementary metal–oxide–semiconductor inverter circuit are still quite different due to the different distribution of random ITs. The NMs of inverter circuit increase as the number of random ITs increases; however, the NMs' fluctuations are increased due to the more sources of fluctuation at HfO_2/Si interface of HKMG devices.

1. Introduction

Silicon-based devices are scaled down continuously according to Moore's law.[1)] More and more challenges have to be overcome for advanced device technologies; one of them is the management of process variation and random fluctuation.[2)] With device scaling, various randomness effects resulting from the random nature of manufacturing process, such as ion implantation, diffusion, and thermal annealing, have induced significant characteristic fluctuations in nanometer scale complementary metal–oxide–semiconductor (nano-CMOS);[3–7)] in particular, threshold voltage (V_{th}) fluctuation is crucial for design window, noise margin, yield, stability, and reliability of nano-CMOS integrated circuits. High-κ/metal gate (HKMG) technology for maintaining device characteristics and suppressing device's intrinsic parameter fluctuation is introduced.[8–19)] However, emerging fluctuation source, the random interface traps (ITs) at high-κ/silicon interface degrades device characteristic.[20–31)] Recently, one-dimensional (1D) and 2D random ITs at high-κ/silicon interface were proposed for DC characteristic fluctuation simulation of sub-45-nm CMOS devices.[9,16,21)] But much less attention has been paid to device's AC and transfer-characteristic fluctuations of a nano-CMOS inverter circuit caused by random ITs. In addition, randomness of IT's positions in devices makes the fluctuation of gate capacitance of a device nonlinear.

In this work, DC/AC and transfer-characteristic fluctuations, induced by random ITs at HfO_2/Si interface, of 16-nm-gate HKMG metal–oxide–semiconductor field effect transistor (MOSFET) device and inverter circuit are studied by using an experimentally calibrated 3D device simulation. Because random ITs exhibit a spike of local energy barrier and trap majority carriers, for the N-MOSFETs, electrons are trapped by acceptor-like traps and result in high V_{th}. Therefore, all fluctuated drain current–gate voltage (I_D–V_G) curves are shifted right; similarly, the fluctuated I_D–V_G curves are shifted left for the P-MOSFETs. The fluctuation of drain current is pronounced resulting from random ITs at sub-threshold regions; however, it is reduced as V_G increases due to inversion charges filling the interface states and minimizing their impact. Nevertheless, the existing random ITs at the HfO_2/Si interface weakens the screening effect, in contrast to random dopant fluctuation (RDF).[5)] For the same number of ITs, simulated device samples with similar I_{on} but different I_{off} may disclose the effect of random ITs' position on the off-state potential; in particular, ITs near source end alter potential barrier significantly. Large number of random ITs not only implies high density of ITs at HfO_2/Si interface but also scatters high-field transport of inversion-layer carriers; consequently, it raises V_{th} and impacts the on-state conducting current path, in spite of maintaining similar off-state current. In addition, drain-induced barrier lowering (DIBL), transconductance (g_m), output resistance (r_o), and gate capacitance (C_G)[1)] are governed by random ITs; the cutoff frequency decreases owing to the decreasing g_m and increasing C_G. The intrinsic gate delay time (τ) increases because of decreasing the on-state current and increasing C_G, as the number of ITs increases. The noise margin fluctuation (σNM) of a CMOS inverter circuit is thus analyzed and compared with the results of RDF. Even for cases with the same number of random ITs, NMs are still quite different due to the different distribution of random ITs. Both NM high (NM_H) and NM low (NM_L) increase as the number of random ITs increases. Because σNM is directly proportional to σV_{th}, σNM is also increased due to the more sources of fluctuation at HfO_2/Si interface of HKMG devices. Compared with the results of RDF, the random ITs-induced NM_L fluctuation, $\sigma NM_{L,ITs}$, is about 20.3 mV which is less than the RDs-induced NM_L fluctuation, $\sigma NM_{L,RDs}$ of 35.0 mV. Similarly, RDs-induced NM_H fluctuation, $\sigma NM_{H,RDs}$, is 20.1 mV which is also less than $\sigma NM_{H,RDs}$ of 30.0 mV. Furthermore, the findings of combined RDs and random ITs (denoted as RDs+ITs) simulation indicate RDF is a major part of σNM of 16-nm-gate HKMG CMOS inverter circuit.

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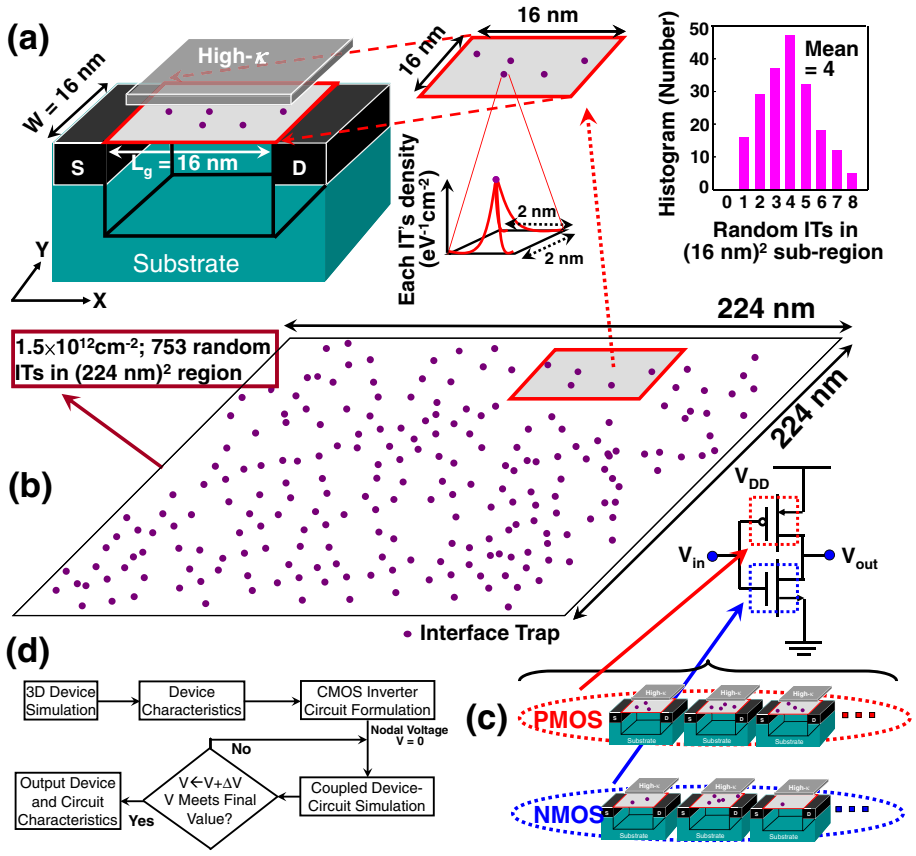

Fig. 1. (Color online) (a) The simulated structure and source of random interface traps (pink dots: each IT has $2 \times 2\,\mathrm{nm}^2$ size) appearing at the interface of HfO_2/Si film. (b) Simulation setting for fluctuation of random ITs. We first generate 753 acceptor-like traps for N-MOSFETs in a large plane, where the corresponding trap's concentration in the plane is around $1.5 \times 10^{12}\,\mathrm{cm}^{-2}$ and the total number of generated traps follows the Poisson distribution. The energy of each random interface trap on the plane is assigned according to a distribution of trap's density.[9,22,23] Then, the entire plane is partitioned into sub-planes (size: $16 \times 16\,\mathrm{nm}^2$), where the number of random interface traps in every sub-plane may vary from 1 to 8 and the average number is 4. Consequently, the density of interface traps at the $16 \times 16\,\mathrm{nm}^2$ interface of HfO_2/Si film is varying from 0.8×10^{10} to $6 \times 10^{11}\,\mathrm{eV}^{-1}\,\mathrm{cm}^{-2}$. (c) The totally random generated N- and P-MOSFET devices are simulated for noise margin calculation of 16-nm CMOS inverter circuit using coupled device-circuit simulation. (d) Flow of coupled device-circuit simulation.

This paper is organized as follows. In §2, we brief the random ITs fluctuation (ITF) simulation procedure. In §3, we discuss DC/AC and transfer-characteristic fluctuations of the studied device and circuit. Finally, we draw conclusion and suggest future work.

2. ITF Simulation Procedure

The devices we studied are the 16-nm-gate MOSFETs (width: 16 nm) with amorphous-based titanium nitride/hafnium oxide (TiN/HfO_2) gate stacks and an effective oxide thickness (EOT) of 0.8 nm, as shown in Fig. 1(a). We first calibrate the nominal DC characteristic of the studied HKMG devices according to ITRS roadmap for low operating power, which was experimentally quantified in our recent study.[32] Note that all adopted material properties, device settings, and characteristics follow our recent study,[8] where the threshold voltage of the 16-nm-gate N-MOSFETs is equal to 250 mV (−250 mV for P-MOSFETs). For ITF simulation, we first randomly generate 753 ITs in a large 2D plane, where the size of plane is $(224\,\mathrm{nm})^2$, as shown in Fig. 1(b); thus, the concentration in the entire plane is about $1.5 \times 10^{12}\,\mathrm{cm}^{-2}$ and the equivalent total number of generated traps follows the Poisson distribution. The entire plane is then partitioned into many sub-planes (the size of each sub-plane is $16 \times 16\,\mathrm{nm}^2$), where the number of random traps in all sub-planes (area: $16 \times 16\,\mathrm{nm}^2$) may vary from 0 to 8 and the average number is 4. To perform 3D device simulation with 2D ITF for each randomly generated device sample, we assume each IT has same area of $(2\,\mathrm{nm})^2$, as shown in Fig. 1(a), and assign each individual IT's density within its area. Each IT's density on the sub-plane is randomly assigned according to the relation of trap's density versus trap's energy.[9,22,23] The procedure is repeated until all sub-regions are assigned; thus, the entire IT's density at HfO_2/Si interface of each device vary from 0.8×10^{10} to $6 \times 10^{11}\,\mathrm{eV}^{-1}\,\mathrm{cm}^{-2}$.[24,25,33–36] Therefore, 196 randomly generated 3D device samples with 2D random ITs at HfO_2/Si interface are simulated to assess the influence of ITF.

Owing to lack of well-established compact models for the 16-nm-gate CMOS devices, by using the coupled device-circuit simulation technique,[3–5] the circuit level fluctuations are estimated for the CMOS inverter circuit, as shown in Fig. 1(c), where the flowchart of coupled device-circuit simulation is shown in Fig. 1(d). To estimate the inverter's NM property, electrical characteristics of each randomly generated device in the tested circuit are first calculated by the 3D device simulation. The obtained result is then used as devices' terminal characteristics in the coupled device-

Table I. Comparison of σV_{th} and σC_G calculated by 1D IT's method and our approach for the 16-nm N-MOSFETs.

	σV_{th} (mV)	σC_G ($\times 10^{-3}$ fF)	
		at $V_G = 0.4$ V	at $V_G = 0.8$ V
1D ITs Method	15	0.02	0.22
This work	26.3	0.21	0.28

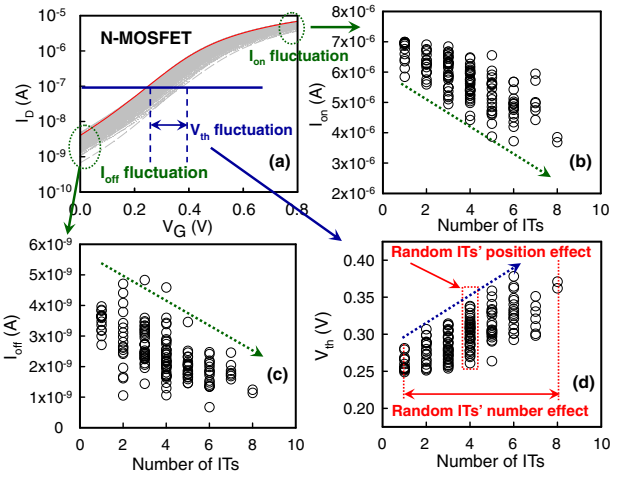

Fig. 2. (Color online) (a) The totally random ITs-induced fluctuations of I_D–V_G curves of the 16-nm-gate N-MOSFET, where the red solid line indicates the nominal case and the gray dashed lines are all fluctuated cases. (b) I_{on}, (c) I_{off}, and (d) V_{th} are extracted fluctuations as a function of the number of ITs, where each symbol shows each random IT-fluctuated result.

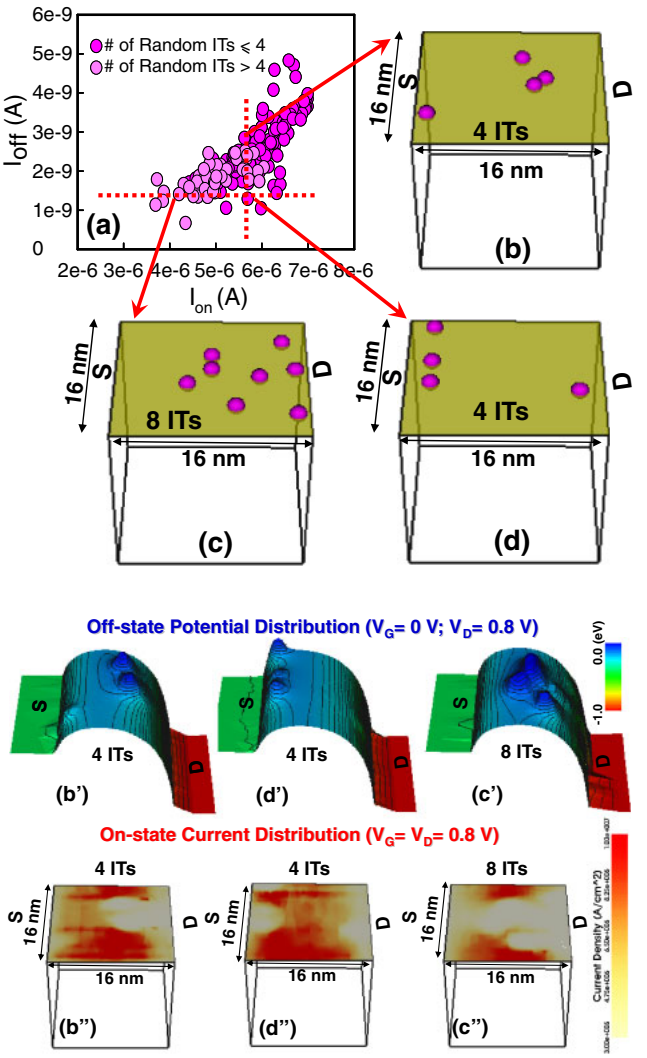

Fig. 3. (Color online) (a) Plot of I_{off}–I_{on} of the 16-nm-gate N-MOSFET induced by random ITs. Light pink dots are for the number of random ITs is equal or greater than 4 and the rest parts are marked as dark pink. Three cases are selected among 196 simulations to show different random number and position effects. (b) Among four ITs, one IT near source end. (c) Eight ITs are randomly distributed at the interface of HfO_2/Si film and they are a little bit away from source end. (d) Among four ITs, three ITs are near source end. (b′)–(d′) are their off-state surface potential ($V_G = 0$ V and $V_D = 0.8$ V) with respect to (b)–(d), respectively. (b′)–(d′) are their corresponding on-state surface current density ($V_G = V_D = 0.8$ V).

circuit steady-state simulation. The nodal equations of the tested inverter circuit are formulated and then directly coupled to the device transport equations (in the form of a large matrix that contains both circuit and device equations), which are solved simultaneously to obtain the circuit transfer characteristics. We notice that the device characteristics obtained by device simulation, such as distributions of potential and current density, are input in the inverter circuit simulation through device's contact terminals. Notably, to explore influences of combined RDs and random ITs on NMs of CMOS inverter circuit, the random dopants and random ITs are generated respectively, and then randomly positioned into device channel at HfO_2/Si interface of each device simultaneously. Simulation method of RDF follows the details appearing in our earlier work.[3–5,32)]

3. Results and Discussion

We first compare the random ITs-induced σV_{th} ($\sigma V_{th,ITs}$) calculated by the 1D and 2D approaches, as listed in Table I, the 1D calculation ($\sigma V_{th,ITs} = 15$ mV) is lower than that of our calculation owing to without considering random distribution of ITs along finite width direction in the 1D simulation. Figure 2(a) shows the totally random ITs-induced fluctuations of I_D–V_G curves of the 16-nm-gate N-MOSFETs, where the red solid line indicates the nominal case (i.e., the 3D device simulation with zero random ITs) and the gray dashed lines are all fluctuated cases. Figures 2(b) and 2(c) are extracted on-state current (I_{on}) and off-state current (I_{off}) as functions of the number of ITs, where each symbol shows each random IT-fluctuated result. As shown in Fig. 2(d), the value of V_{th} is determined from a current criterion that the drain current larger than $10^{-7} \times (W/L)A$, where L and W are the gate length and width, respectively. The V_{th} increases (and then the on-/off-state current decreases accordingly) as the number of ITs increases. The simulated $\sigma V_{th,ITs}$ is 26.3 mV which is smaller than the results of RDF ($\sigma V_{th,RDs} = 43$ mV). The random ITs-position-induced different fluctuations of characteristics in spite of the same number of ITs, as marked by open bar in inset of Fig. 2(d), where the magnitude of the spread characteristics increases as the number of ITs increases. To focus on the impact of random ITs on physical characteristic, Fig. 3(a) shows I_{off}–I_{on} plot of the 16-nm-gate N-MOSFETs induced by random ITs; light-pink dots are for device whose number of random ITs is equal or greater than 4, and the rest

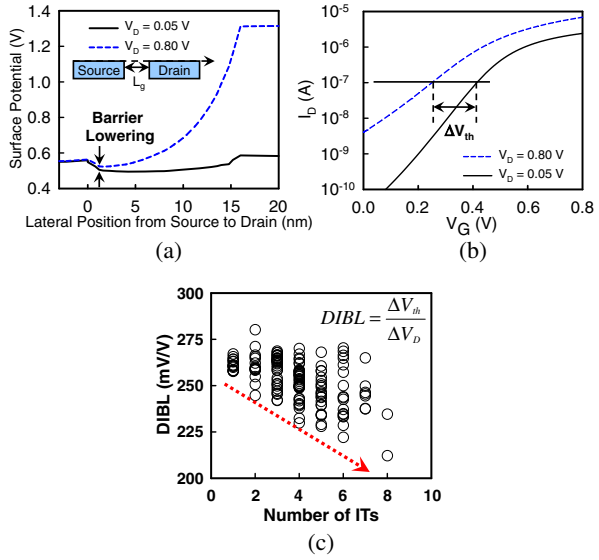

Fig. 4. (Color online) (a) Plot of the surface potential of 16-nm-gate nominal N-MOSFET for $V_G = 0.8$ V and $V_D = 0.05$ and 0.8 V (linear and saturated cases). (b) Plot of two I_D–V_G curves for $V_G = 0.8$ V and $V_D = 0.05$ and 0.8 V (linear and saturated cases). (c) DIBL versus the number of random ITs.

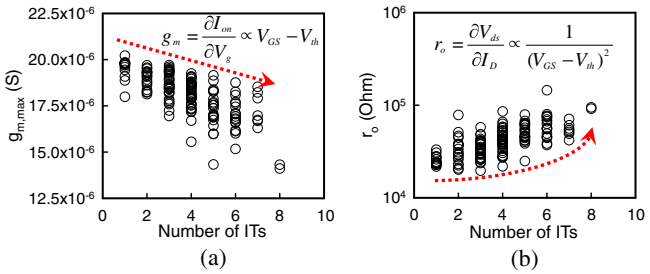

Fig. 5. (Color online) (a) $g_{m,max}$ (b) and r_o with respect to the number of random ITs for the 196 random ITs-fluctuated N-MOSFETs.

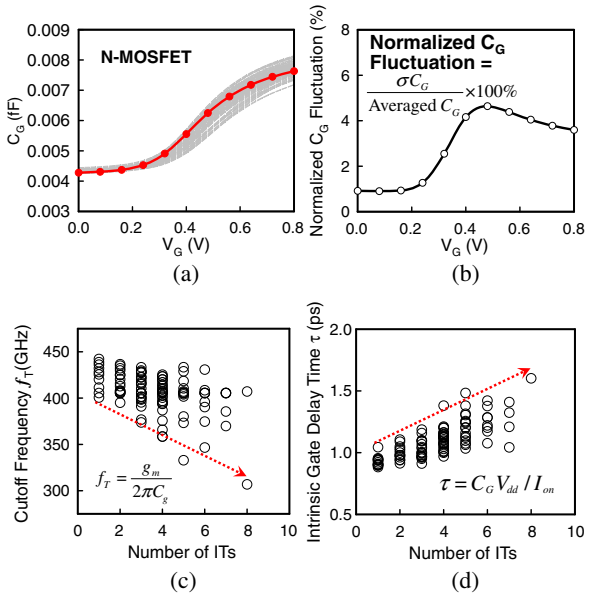

Fig. 6. (Color online) (a) The random ITs-fluctuated C_G–V_G curves for the studied 16-nm-gate N-MOSFETs, where the nominal case is red and the fluctuated data are in gray. (b) The normalized C_G fluctuation. (c) The cutoff frequency versus the number of random ITs. (d) The intrinsic gate delay versus the number of random ITs.

parts are marked as dark-pink dots. Three cases are selected among 196 simulations to demonstrate random number-and-position associated local repulsive coulomb field as well as disturbed surface current conducting path. Figures 3(b) and 3(d) are the two cases which have same number of ITs (4 ITs). These two devices have similar I_{on} owing to similar current conduction areas, as shown in Figs. 3(b″) and 3(d″). However, their I_{off} are different because random ITs near the source end locally results in relatively higher local spike of potential barriers and thus raises V_{th}, compared with ITs appearing in the drain end [Fig. 3(b′)]. Random number effect of ITs at HfO_2/Si interface are major obstacles to electrons and disturbed surface current conducting path, which is explained in Figs. 3(c) and 3(d). The two cases have similar I_{off} but different I_{on} owing to random number effect. As shown in Figs. 3(c″) and 3(d″), although 8 ITs in Fig. 3(c) positioning away from the source end have weakened interaction with mobile electrons due to the relatively larger drift velocity and electron transport energy, many local spikes of potential barriers still effectively impede surface current conduction which is even stronger than that of ITs appearing in the source end, as shown in Fig. 3(d″). Thus, the device with random ITs of Fig. 3(c) has minimal I_{on}, compared with the case of Fig. 3(d). The random ITs-fluctuated DIBL effect is pronounced for the 16-nm-gate N-MOSFETs, as shown in Fig. 4(c). In the weak inversion region there is a potential barrier at the channel region owing to a balance between drift and diffusion current. The barrier height decreases as V_D increases, as shown in Fig. 4(a); it results in an increased I_D, as shown in Fig. 4(b), which is controlled not only by V_G, but also by V_D. The DIBL effect could be observed through the I_D–V_G curves of a device under the linear ($V_D = 0.05$ V) and saturated ($V_D = 0.8$ V) cases, as shown in Fig. 4(b), deriving by the lateral shift of V_{th} divided the difference of V_D in inset of Fig. 4(c). Figure 4(c) shows the ITs-fluctuated DIBL characteristic of the 16-nm-gate N-MOSFETs, the DIBL decreases as the number of ITs increases due to ITs decrease the probability of electric-field lines penetrating from drain to source. The tendency of increasing fluctuation of DIBL follows σV_{th} as the number of ITs increases. The maximum g_m ($g_{m,max}$) and the output resistance (r_o) of transistor as functions of the number of ITs are shown in Figs. 5(a) and 5(b). Since g_m varies with ($V_{GS} - V_{th}$), $g_{m,max}$ decreases owing to V_{th} is increased with increasing the number of ITs; similarly, r_o is increased as the number of ITs increases. The random position of ITs results in rather different fluctuations of characteristics despite the same number of ITs. Furthermore, the magnitude of the spread characteristics increases as the number of ITs increases.

Gate capacitance of MOSFET devices is one of important AC parameters, comparison between the 1D ITF simulation and our approach is listed in Table I for $V_G = 0.4$ and 0.8 V. σV_G calculated by 1D method is underestimated. Figure 6(a) shows the random ITs-fluctuated gate capacitance–gate voltage (C_G–V_G); where the lateral shift of C_G is a result of the variation of V_{th}; and the substantially altered slopes of C_G–V_G curves can be attributed to the random-ITs-position

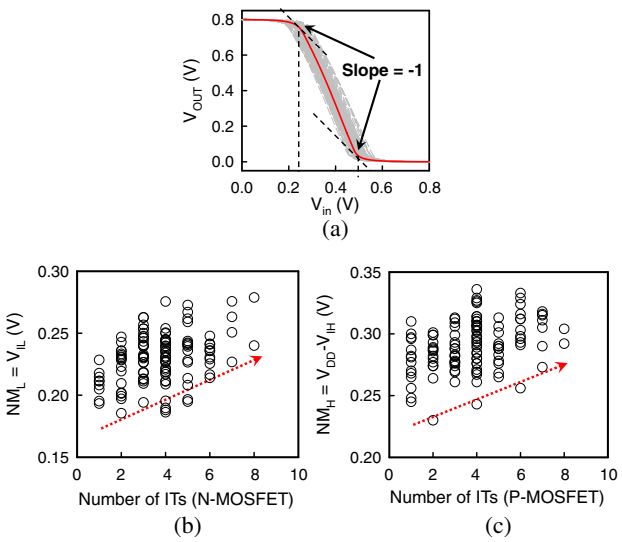

Fig. 7. (Color online) (a) The random ITs-fluctuated voltage transfer curves ($V_{out} - V_{in}$) of the 16-nm-gate CMOS inverter circuits. The parts of slope $= -1$ indicate the low and high noise margins of the inverter. (b) and (c) show noise margins, NM_L and NM_H, as a function of the dopant number in the 16-nm-gate N- and P-MOSFETs.

effect, which was also observed for devices under influence of RDF.[5)] The normalized C_G fluctuation versus V_G, as shown in Fig. 6(b), is normalized by the nominal C_G. The result implies the importance of random-ITs-position effect. Notably devices with high V_G, the screening effect of the inversion layer of the devices can not effectively screen the variation of potential, and thus, the normalized σC_G still suffers from sizeable fluctuation which is different from RDF's results.[5)] The results of g_m and C_G enables us to estimate the cutoff frequency and intrinsic gate delay time of the studied 16-nm-gate N-MOSFETs, as shown in Figs. 6(c) and 6(d), respectively, where the insets give the definition of these quantities. The cutoff frequency is decreased and τ is increased as the number of ITs increases. With the decreasing g_m and increasing C_G, the cutoff frequency of the device decreases with increasing ITs' number. τ is increased as the dopant number increases due to the decreasing on-state current and increasing C_G. Their fluctuation magnitude is increased as the number of ITs increases. The random ITs' effect not only causes fluctuations in V_{th} and I_D but also affects C_G of the transistor. For the 16-nm-gate P-MOSFETs, not shown here, we do perform similar simulations, in order to study the NM of the 16-nm-gate CMOS inverter circuit.

Figure 7(a) shows the transfer characteristic (plot of $V_{out} - V_{in}$) of the random ITs-fluctuated 16-nm-gate CMOS inverters. Two points on the voltage transfer curve determine the circuit's NMs. The two points on the voltage transfer curve are defined as those values of V_{in} where the incremental gain is unity; the slope is -1 V/V. Figures 7(b) and 7(c) show the NMs for the logic "1" and "0", NM_H and NM_L, respectively, as a function of the ITs' number. In addition, even the cases with the same number of ITs, their NMs are still different due to ITs' random position effect. The NM_L increases as the number of ITs increases because of the increased V_{th} of the 16-nm-gate N-MOSFETs. For the NM_H, as numbers of ITs in the 16-nm-gate P-MOSFETs increase, the increased V_{th} of the device may decrease the V_{IH} of the $V_{out} - V_{in}$ curve and, thus, increase the NM_H. As listed in Table II, both the fluctuations of NM_L ($\sigma NM_L = 20.3$ mV) and NM_H ($\sigma NM_H = 20.1$ mV) are smaller than the RDs-induced $\sigma NM_{L,RDs}$ of 35 mV and $\sigma NM_{H,RDs}$ of 30 mV, respectively. RDs-induced NM_L and NM_H fluctuations are 42 and 33% larger than ITs-induced data. If we assume the random ITs and random dopants are independent and identically distributed (*iid*) random variables, statistical sums of variances of the random ITs and the random dopants calculated by using formulas $(\sigma^2 NM_{L,ITs} + \sigma^2 NM_{L,RDs})^{1/2}$ and $(\sigma^2 NM_{H,ITs} + \sigma^2 NM_{H,RDs})^{1/2}$ are 40.4 and 36.1 mV, respectively. As summarized in Table II, the $\sigma NM_{L,RDs+ITs}$ and $\sigma NM_{H,RDs+ITs}$ resulting from the combined random ITs and random dopants are 37.6 and 33.1 mV. Therefore, the *iid* assumption with respect to RDs and ITs may not always hold because it does not consider the interaction between ITF and RDF (the results according to *iid* assumption are 7.5 and 9.1% overestimation) which should be subject to further studies.

Table II. Comparison of σNM_L and σNM_H induced by the random ITs (in mV), the random dopants, and the combined random ITs and dopants for 16-nm CMOS inverter circuit. Statistical sums of variances of the random ITs and the random dopants are calculated by using formulas $(\sigma^2 NM_{L,ITs} + \sigma^2 NM_{L,RDs})^{1/2}$ and $(\sigma^2 NM_{H,ITs} + \sigma^2 NM_{H,RDs})^{1/2}$, respectively, where we assume that the random ITs and random dopants are independent and identically distributed random variables.

	σNM_L	σNM_H
Random ITs	20.3	20.1
Random dopants	35.0	30.0
Statistical sum	40.4	36.1
Combined random ITs and random dopants	37.6	33.1

4. Conclusions

In this study, we have focused on electrical and transfer-characteristic fluctuations in 16-nm-gate TiN/HfO_2 MOSFET devices and inverter circuit induced by random ITs at HfO_2/Si interface. The preliminary findings of this study indicate the random ITs' effect not only causes fluctuations in V_{th} and current but also affects the gate capacitance of the transistor. In contrast to random-dopant fluctuation, the screening effect of inversion layer cannot effectively screen potential's variation; thus, devices still have noticeable fluctuation of gate capacitance under high gate bias. The DIBL and the cutoff frequency decrease, and the intrinsic gate delay time increases as the number of ITs increases together with their increased fluctuation. The NMs of inverter circuit increase as the number of random ITs increases; however, the NMs' fluctuations are also increased due to the more sources of fluctuation at HfO_2/Si interface of HKMG devices. Random ITs near the source end result in significant locally enhanced spikes of surface potential which not only fluctuates V_{th} but also perturbs carrier's transport. Additionally, the interaction between RDs and ITs should be subject to further investigation for clearer understandings. Reduction of the fluctuation resulting from random ITs at HfO_2/Si interface could be explored by reducing the entire density of random ITs; for example, if the entire IT's density vary from 0.8×10^9 to $6 \times$

$10^{10}\,eV^{-1}\,cm^{-2}$ at HfO_2/Si interface of each 16-nm-gate N-MOSFET device (a tenth of the original setting in this work), σV_{th} will be reduced from 26.3 to 10.2 mV (about 61.2% reduction). Notably, preliminary result of the interaction between random dopants and interface traps in 16-nm-gate HKMG MOSFET devices was reported in ref. 37. We are currently calibrating fabricated and measured 16-nm HKMG CMOS samples.

Acknowledgments

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