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Robust Data Retention and Superior Endurance of Silicon–Oxide–Nitride–Oxide–Silicon-Type Nonvolatile Memory with NH_3-Plasma-Treated and Pd-Nanocrystal-Embedded Charge Storage Layer

Sheng-Hsien Liu, Wen-Luh Yang[1]*, Yu-Ping Hsiao[1], and Tien-Sheng Chao[2]

Ph. D. Program in Electrical and Communications Engineering, Feng Chia University, Taichung 407, Taiwan
[1]*Department of Electronic Engineering, Feng Chia University, Taichung 407, Taiwan*
[2]*Department of Electrophysics, National Chiao Tung University, Hsinchu 330, Taiwan*

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In this study, we investigated an ammonia (NH_3) plasma-pretreatment (PT) for suppressing the formation of interface states between metal nanocrystals (NCs) and the surrounding dielectric during the NC forming process with the aim of obtaining a highly reliable Pd NC memory. The discharge-based multipulse (DMP) technique was performed to analyze the distribution of trap energy levels in the Pd NCs/Si_3N_4-stacked storage layer. Through DMP analysis, it is confirmed that the NH_3 PT not only significantly increases the quality of the surrounding dielectric of metal NCs but also effectively passivates shallow trap sites in the Si_3N_4 trapping layer. As compared with the sample without NH_3 PT, the NH_3-plasma-treated device exhibits better reliability characteristics such as excellent charge retention (only 5% charge loss for 10^4 s retention time) and very high endurance (no memory window narrowing after 10^5 program/erase cycles). In addition, the robust multilevel cell retention properties of the NH_3-plasma-treated memory are also demonstrated. © 2012 The Japan Society of Applied Physics

1. Introduction

Recently, charge-trapping-type nonvolatile memories (CT-NVMs) with embedded metal nanocrystals (NCs) have been extensively studied as a promising next-generation NVM owing to the benefits of combining quantum wells and discrete trap sites.[1–5] When metal NCs are embedded in the dielectric, the interface between the NCs and the dielectric has a high defect density and these defects always lie in unstable states. This is ascribed to material mismatching and thermal damage caused by the NC forming process.[6,7] This phenomenon results in a serious Fermi level pinning effect that shifts the effective work function at the interface between the metal NCs and the dielectric.[8–11] Thus, it is difficult for electron charges to be stored in quantum wells accurately and it is easy for them to be pinned on interface states between the NCs and the dielectric. Also, these storage charges in interface states are easily discharged from the storage layer through a trap-assisted tunneling mechanism,[12] resulting in a critical charge retention issue, especially in a high-temperature environment. As a result, the quality of the dielectric surrounding of the metal NCs is a key factor in the reliability of NVM.

In this study, an NH_3 plasma-pretreatment (PT) has been utilized to passivate the dielectric surface before metal deposition to suppress the formation of interface states. It is expected that the NH_3 plasma passivation can yield a high-quality dielectric surface to prevent damage induced by the metal NC formation process. Palladium (Pd) metal was selected as the NC material in this study owing to its high work function of 5.1 eV[13] as well as its good performance in Pd NC NVMs.[7,14] The electrical characteristics, including the program and erase (P/E) speeds, charge retention, and endurance, for the CT-NVM with embedded Pd NCs with and without NH_3 PT are demonstrated. Additionally, the multilevel cell (MLC) retention characteristics of the NH_3-plasma-treated device were also investigated in this study.

*E-mail address: wlyang@fcu.edu.tw

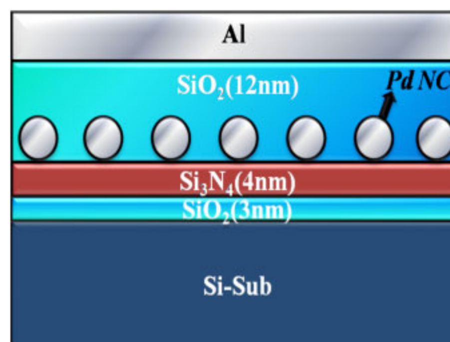

Fig. 1. (Color online) Schematic structure of the MONOS capacitor NVM with embedded Pd NCs.

2. Device Fabrication

The devices were prepared on ⟨100⟩ p-type silicon wafers. After standard Radio Corporation of America (RCA) cleaning, a 3-nm-thick silicon oxide (SiO_2) film was thermally grown as a tunnel layer in N_2O ambient, then a silicon nitride (Si_3N_4) film with 4 nm thickness was deposited at 780 °C by low-pressure chemical vapor deposition. Subsequently, NH_3 PT was performed on the $Si_3N_4/SiO_2/Si$-stacked layer at 375 °C for 60 s by a high-density plasma chemical vapor deposition system. A 2-nm-thick Pd thin film was then deposited by electron-gun evaporation. Afterward, Pd NCs were formed by 600 °C thermal annealing for 30 s, and then a Pd NCs/Si_3N_4-stacked storage layer was obtained. To avoid the possibility of Pd oxidizing, the formation process was performed in N_2 atmosphere. A 12-nm-thick blocking oxide layer was sequentially deposited by plasma enhanced chemical vapor deposition. Finally, aluminum films were deposited and patterned on both the top and back sides of the samples to form a metal/oxide/nitride/oxide/silicon (MONOS) capacitor NVM with embedded Pd NCs, as shown in Fig. 1. In addition, a control sample (without NH_3 PT) was also prepared. The diameter of the devices was 200 µm. The structural analysis of the Pd NCs was performed by

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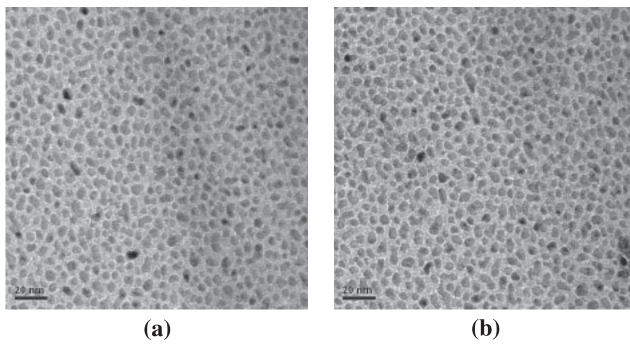


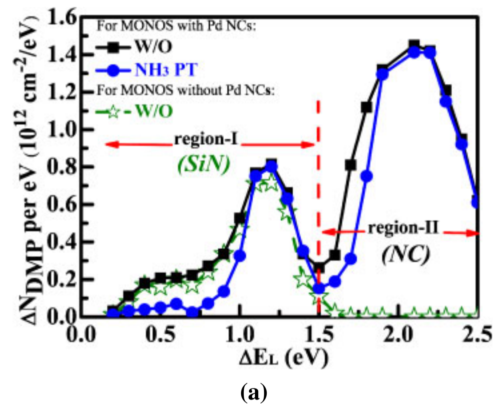
Fig. 2. Top-view TEM images of Pd NCs deposited on the Si_3N_4 surface (a) without and (b) with NH_3 plasma treatment.

transmission electron microscopy (TEM), and the electrical properties were determined by Keithley 4200 and 82 C-V systems.

3. Results and Discussion

Figure 2(a) displays a top-view TEM image of the Pd NCs without NH_3 PT deposited on the Si_3N_4 surface. It is confirmed that the Pd NCs were self-assembled on the Si_3N_4 surface from the ultrathin Pd film with 2 nm thickness after 600 °C thermal annealing for 30 s. The range of diameters and the number density of the Pd NCs are estimated to be 3–6 nm and *ca.* $1.58 \times 10^{12}\ cm^{-2}$, respectively. A top-view TEM image of the Pd NCs with NH_3 PT is shown in Fig. 2(b). In Figs. 2(a) and 2(b), it is seen that both the range of diameters and the number density of the Pd NCs are approximately similar. It is verified that the formation of Pd NCs is unaffected by NH_3 PT. That is because the NH_3 PT process time is short, making it difficult for it to affect the roughness of the Si_3N_4 surface.

To investigate the influence of NH_3 PT on the Pd NCs/Si_3N_4-stacked storage layer, the discharge-based multipulse (DMP) technique[15] was used to further analyze the distribution of trap energy level, as shown in Fig. 3(a). Figure 3(a) shows the distribution of trap energy levels for the Si_3N_4-only trapping layer and the Pd NCs/Si_3N_4-stacked storage layer with/without NH_3 PT. In the figure, ΔE_L on the *x*-axis and ΔN_{DMP} on the *y*-axis represent the trap energy level and equivalent trap sheet density, respectively. Figure 3(b) displays the related energy band diagram of the MONOS structure with embedded Pd NCs. Note that, ΔE_L on the *x*-axis in Fig. 3(a) and ΔE_L in Fig. 3(b) correspond to each other. By comparison of the trap energy-level distribution for MANOS with and without the Pd NCs, it is found that the trap energy-level distribution in MANOS without the Pd NCs is within the range of 0.2–1.5 eV and excludes the trap energy level in the range of 1.5–2.5 eV. Moreover, in a previous report,[16] it was explicitly pointed out that the distribution of trap energy levels in a stoichiometric Si_3N_4 trapping layer is mainly located in the region of 1.26–1.46 eV in a $SiO_2/Si_3N_4/SiO_2$ stack. This implies that the trap energy-level profile in the Si_3N_4 trapping layer locates in the range of 0.2–1.5 eV and the trap energy-level profile within the range of 1.5–2.5 eV can be attributed to the contribution of NCs. Therefore, the distribution of trap energy levels in Fig. 3(a) can be divided into two parts: (1) region I: 0.2–1.5 eV; (2) region II: 1.5–



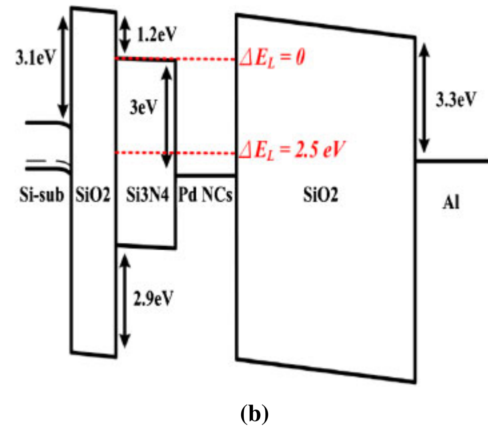


Fig. 3. (Color online) (a) Distribution of trap energy levels in the Si_3N_4 storage layer and the Pd NCs/Si_3N_4-stacked storage layer with/without NH_3 plasma treatment and (b) related energy band diagram of MONOS NVM structure with embedded Pd NCs.

2.5 eV. The trap profiles in region I and region II belong to the Si_3N_4 trapping layer and the contribution of Pd NCs, respectively. Based on the DMP measurement mechanism, the electrons trapped in NCs indeed have difficulty discharging to the Si substrate via direct tunneling due to 7 nm (SiO_2 thickness + Si_3N_4 thickness) away from the Si substrate. Consequently, the trap profile in region II cannot represent the real trap energy-level profile in the NCs, but it can be regarded as the trap energy-level profile contributed from the NCs. In addition, through the comparison of region II of the MONOS devices with and without NH_3 PT, we can determine the influence of NH_3 PT on the trap energy-level distribution in the MONOS with NC memories. It is found that in region I, the Si_3N_4 trapping layer with NH_3 PT has a 63% decrease in sheet density of trap sites within the energy-level region of 0.2–1.0 eV as compared with that without NH_3 PT. This is due to part of the shallow trap sites in the Si_3N_4 trapping layer being passivated by nitrogen plasma during the NH_3 PT process. Also, it is found that the sheet density of trap sites within the energy-level region of 1.0–1.5 eV is unchanged after NH_3 PT. This result implies that the NH_3 plasma passivation is sensitive to shallow trap sites and insensitive to deep trap sites. On the other hand, in region II, there is a 44% decrease in the sheet density of trap sites within the energy-level region of 1.5–1.8 eV for the NH_3-plasma-treated sample. This is ascribed to NH_3-plasma-treated Si_3N_4 having a high-quality surface, which prevents the formation of interface states during the

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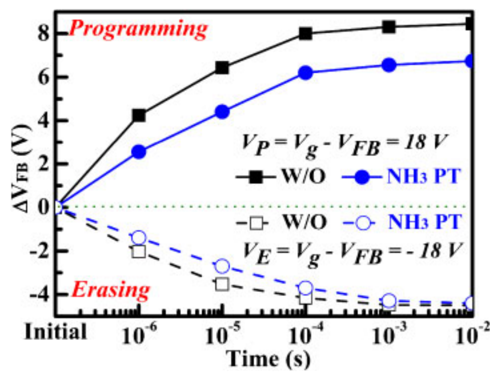

Fig. 4. (Color online) Program and erase transients of the Pd NC NVMs with and without NH_3 plasma treatment.

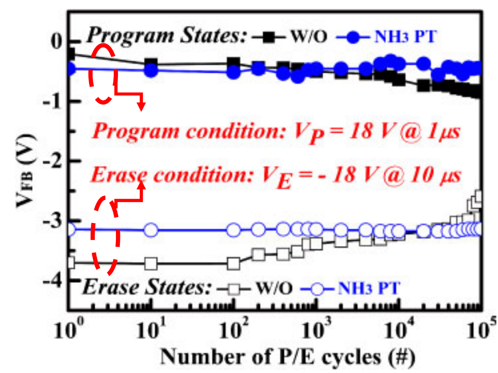

Fig. 5. (Color online) Endurance characteristics of the Pd NC NVMs with and without NH_3 plasma treatment.

NC forming process. In addition, the NH_3 PT causes a 29% decrease in the trap density of the Pd NCs/Si_3N_4-stacked storage layer. However, these 29% lost trap sites are at shallow energy levels and easily cause charge loss problems. Therefore, the trap sites that are passivated by NH_3 PT are unnecessary for highly reliable NVM.

The P/E transients of the Pd NC memories with and without NH_3 PT are shown in Fig. 4. The figure shows that the control sample has a high program speed as well as a larger memory window than the NH_3-plasma-treated sample. As compared with that of the control sample, the charge trapping efficiency of the NH_3 plasma-treated device is decreased *ca.* 25% by NH_3 PT; even so, this phenomenon is immaterial to the CT-NVMs. This is because most of the 25% lost charges are momentarily stored at shallow trap sites in the Si_3N_4 trapping layer and interface states between the Pd NCs and the Si_3N_4, making it easy for them to escape from the storage layer, especially at high temperatures. For highly reliable NVM, therefore, it is clearly necessary to eliminate shallow trap sites. For the erase measurement, the devices were initially operated in the program state, that is, V_{FB}-shift = 4.5 V. It is found that the NH_3-plasma-treated memory has a lower erase speed than the control sample. This is ascribed to the equivalent trap energy level of the NH_3 PT storage layer being deeper than that of the storage layer without NH_3 PT, and a related result is shown in Fig. 3(a). As the electron charges are stored in deep trap sites, it is difficult for them to be removed under the erase operation.

Figure 5 presents the endurance characteristics of the devices with and without NH_3 PT. The pulse conditions of program and erase are $V_P = 18$ V at 1 μs and $V_E = -18$ V at 10 μs, respectively. For the control sample, it is found that the memory window is degraded to *ca.* 50% after 10^5 P/E cycles. However, we consider that the shifts of V_{FB} in the program and erase states are dominated by various mechanisms. The upward shift of V_{FB} in the erase state is due to the defects around the NCs and because the metal NCs enhance the strong electric field between the NCs and the Si substrate.[17,18] The strong electric field induced by NCs exists not only on the tunnel SiO_2 layer but also at the interface between Si_3N_4 and the NCs.[19] Through the assistance of the shallow deficiencies around the NCs and the strong electric field at the interface between Si_3N_4 and the NCs, there is a high probability that programming

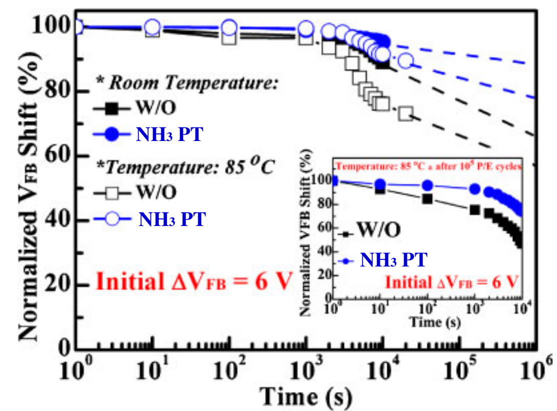

Fig. 6. (Color online) Charge retention characteristics of Pd NC NVMs with and without NH_3 plasma treatment at room temperature and 85 °C. The inset shows the postcycling retention properties of the devices at 85 °C after 10^5 P/E cycles.

charges are injected into the top dielectric. Also, the charges stored in the top dielectric are difficult to be removed. On the other hand, the downward shift of V_{FB} in the program state is due to the formation of leakage path in the surrounding dielectric caused by the frequent P/E cycles.[20,21] In contrast, the NH_3-plasma-treated device exhibits superior endurance with no memory window narrowing. The stable program state is attributed to the high-quality dielectric suppressing the formation of damage caused by the endurance test. This implies that charges can be steadily and accurately stored in the NCs to form a strong coulomb blocking effect at the NC storage layer. The strong coulomb blocking effect can suppress charge injection into the top dielectric to yield a stable erase state.

Figure 6 shows the charge retention characteristics of the devices with and without NH_3 PT at room temperature (RT) and 85 °C. The normalized V_{FB} shift is defined as the ratio between the V_{FB} shift at the time of interest and at the beginning. The devices were initially measured in the program state, that is, V_{FB} shift = 6 V. For the NH_3-plasma-treated device, only 5 and 9% charge losses are observed at RT and 85 °C for a retention time 10^4 s, respectively. According to the results of extrapolation, it also exhibits excellent retention properties with only 10 and 22% charge losses at RT and 85 °C after 10^6 s, respectively. By contrast,

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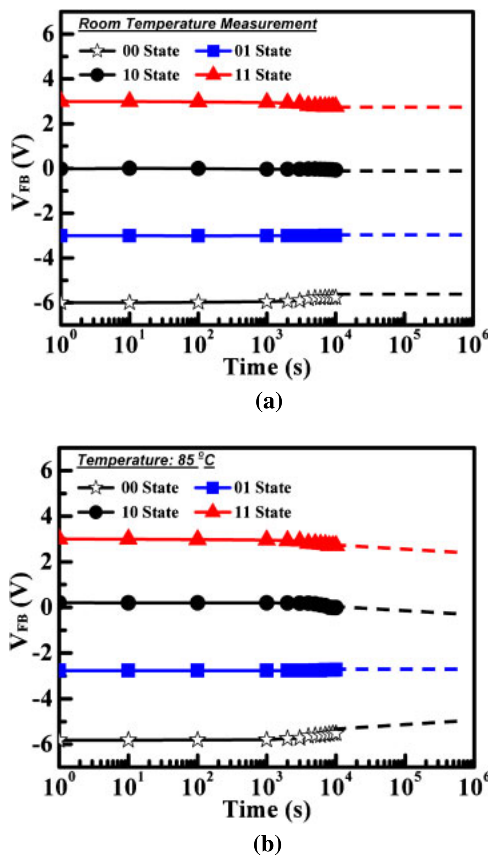

Fig. 7. (Color online) MLC retention characteristics of the NH_3-plasma-treated Pd NC NVM at (a) room temperature and (b) 85 °C.

the sample without NH_3 PT has worse retention properties with extrapolated charge losses of 35 and 44% after 10^6 s at RT and 85 °C, respectively. It is obvious that the retention characteristic of the NH_3-plasma-treated NC memory is better than that of the sample without NH_3 PT. This improvement is attributed to the improved quality of the surrounding dielectric of the Pd NCs and the elimination of shallow trap sites in the Si_3N_4 trapping layer. Additionally, the postcycling retention characteristics were further studied at 85 °C after 10^5 P/E cycles, as shown in the inset of Fig. 6. In the figure, the Pd NC memories with and without NH_3 PT were measured to have 30 and 56% charge losses after 10^4 s, respectively. The result indicates that the NH_3-plasma-treated NC memory has strong resistance to the formation of leakage paths in the surrounding dielectric caused by frequent Fowler–Nordheim electron injection. This is attributed to the high-quality dielectric around the Pd NCs. Figures 7(a) and 7(b) show the MLC retention characteristics of the NH_3-plasma-treated device at RT and 85 °C, respectively. It is seen that the NH_3-plasma-treated Pd NC memory shows robust charge retention with no significant sensing-window narrowing. This is attributed to high-quality dielectric around the Pd NCs.

4. Conclusions

In this work, the quality of the surrounding dielectric of the Pd NCs has been improved significantly by using NH_3 PT for a high-reliability NC memory. Through DMP analysis, the influence of NH_3 PT on the distribution of trap energy levels in a Pd NCs/Si_3N_4-stacked storage layer has been demonstrated and described clearly. The NH_3 PT not only suppresses the formation of interface states during the NC forming process but also eliminates the unnecessary shallow trap sites in the Si_3N_4 trapping layer. Moreover, the NH_3 PT results in Pd NC memory exhibiting robust retention as well as superior endurance characteristics. Under NAND-type MLC operation, the NH_3-plasma-treated device also shows exceptional retention.

Acknowledgements

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1) C. Lee, T. H. Hou, and E. C. C. Kan: IEEE Trans. Electron Devices **52** (2005) 2697.
2) W. R. Chen, T. C. Chang, J. L. Yeh, S. M. Sze, and C. Y. Chang: J. Appl. Phys. **104** (2008) 094303.
3) J. Lu, T. C. Chang, Y. T. Chen, J. J. Huang, P. C. Yang, S. C. Chen, H. C. Huang, D. S. Gan, N. J. Ho, Y. Shi, and A. K. Chu: Appl. Phys. Lett. **96** (2010) 262107.
4) Y. T. Chen, T. C. Chang, J. Lu, J. J. Huang, P. C. Yang, S. C. Chen, A. K. Chu, H. C. Huang, D. S. Gan, N. J. Ho, and Y. Shi: Thin Solid Films **518** (2010) 7324.
5) Y. H. Wu, L. L. Chen, Y. S. Lin, C. H. Chang, J. H. Huang, and G. P. Yu: IEEE Electron Device Lett. **30** (2009) 617.
6) C. C. Lin, T. C. Chang, C. H. Tu, W. R. Chen, C. W. Hu, S. M. Sze, T. Y. Tseng, S. C. Chen, and J. Y. Lin: Appl. Phys. Lett. **94** (2009) 062106.
7) T. K. Kang, T. C. Liao, C. L. Lin, and W. F. Wu: Jpn. J. Appl. Phys. **49** (2010) 086202.
8) T. H. Hou, U. Ganguly, and E. C. Kan: IEEE Electron Device Lett. **28** (2007) 103.
9) J. Robertson: J. Vac. Sci. Technol. B **18** (2000) 1785.
10) C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, and P. Tobin: VLSI Symp. Tech. Dig., 2003, p. 9.
11) S. Samavedam, L. La, P. Tobin, B. White, C. Hobbs, L. Fonseca, A. Demkov, J. Schaeffer, E. Luckowski, A. Martinez, M. Raymond, D. Triyoso, D. Roan, V. Dhandapani, R. Garcia, S. Anderson, K. Moore, H. Tseng, C. Capasso, O. Adetutu, D. Gilmer, W. Taylor, R. Hegde, and J. Grant: IEDM Tech. Dig., 2004, p. 307.
12) M. Houssa, M. Tuominen, M. Naili, V. Afanas'ev, A. Stesmans, S. Haukka, and M. M. Heyns: J. Appl. Phys. **87** (2000) 8615.
13) M. S. Shivaraman, I. Lundstrom, C. Svensson, and H. Hammarsten: Electron. Lett. **12** (2007) 483.
14) K. S. Seol, S. J. Choi, J. Y. Choi, E. J. Jang, B. K. Kim, S. J. Park, D. G. Cha, I. Y. Song, J. B. Park, Y. Park, and S. H. Choi: Appl. Phys. Lett. **89** (2006) 083109.
15) X. F. Zheng, W. D. Zhang, B. Govoreanu, J. F. Zhang, and J. V. Houdt: IEDM Tech. Dig., 2009, p. 139.
16) T. H. Kim, I. H. Park, J. D. Lee, H. C. Shin, and B. G. Park: Appl. Phys. Lett. **89** (2006) 063508.
17) G. Puzzilli and F. Irrera: IEEE Trans. Electron Devices **53** (2006) 775.
18) H. Liu, W. Winkenwerder, Y. Liu, D. Ferrer, D. Shahrjerdi, S. K. Stanley, J. G. Ekerdt, and S. K. Banerjee: IEEE Trans. Electron Devices **55** (2008) 3610.
19) W. R. Chen, T. C. Chang, J. L. Yeh, S. M. Sze, and C. Y. Chang: Appl. Phys. Lett. **92** (2008) 152114.
20) C. C. Lin, T. C. Chang, C. H. Tu, W. R. Chen, C. W. Hu, S. M. Sze, T. Y. Tseng, S. C. Chen, and J. Y. Lin: Appl. Phys. Lett. **94** (2009) 062106.
21) S. C. Chen, T. C. Chang, W. R. Chen, Y. C. Lo, K. T. Wu, S. M. Sze, J. Chen, I. H. Liao, and F. S. Yeh (Huang): Thin Solid Films **518** (2010) 7339.

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