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Characteristics of 4H-SiC RF MOSFETs on a Semi-insulating Substrate

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This study has provided considerable insight into the impact of device down scaling on the characteristics of RF devices. This type of RF devices, featuring a thin p-layer based on a semi-insulating substrate, is free from the unwanted parasitic effects resulting from traditional conducting substrates. We fabricated 4H-SiC RF MOSFETs with f_T/f_{MAX} of 0.7/1.5 GHz and, in so doing, identified the key issues associated with short channel effects, influencing device mobility and the RF characteristics of RF MOSFETs on a semi-insulating substrate.

Introduction

Silicon carbide (SiC) has gained considerable attention in recent years for high-power microwave applications owing to its superior properties, such as high electron velocity, high electric field breakdown strength, and high thermal conductivity. It must be noted that SiC with a breakdown field 10x greater than that of silicon substrate has been widely studied during the past decades. High-Frequency SiC MESFETs with power densities up to 2.8W/mm at 1.8 GHz have been demonstrated [1]. However, MESFETs with negative input voltage and normally-on characteristics are unsuitable for system level designs. Recently, n-channel enhancement MOSFETs have been attracting a great deal of attention, due to their high drain voltage, freedom from gate lag, and normally-off characteristics.

Although 4H-SiC RF MOSFETs have been demonstrated with cutoff frequencies as high as 7GHz [2] and power density up to 1.9W/mm at 3GHz [3], the parasitic elements introduced by the conduction layer seriously influence the operation frequency, gain, and power density. A high-resistance SiC semi-insulating scheme was proposed to reduce parasitic effects, realizing a 4H-SiC RF BJT device with f_T/f_{MAX} of 7/5.2 GHz on a semi-insulating substrate [4]. Because device scaling is necessary to enhance the current density for high power density RF amplifier applications, scaling considerations are often of critical importance in the development of next-generation RF devices. In addition, the short-channel effects (SCEs) of dimension scaling have not been characterized as comprehensively.

It is well known that the SCEs may become a serious issue as RF MOSFETs are scaled down, due to their short channel length. The other factors limiting performance include the thickness of the oxide, source/drain sheet resistance, contact resistance, and channel mobility. Overcoming these factors is crucial. With this in mind, we fabricated SiC MOSFETs of various dimensions on semi-insulating substrates to investigate the impact of down scaling RF MOSFETs to the submicron level.

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In this study, we investigated variations in the performance of transistors in RF devices at the sub-micron-scale. The phenomena of sub-micron devices have been discussed in detail, suggesting that the mobility and DC/RF characteristics would be jeopardized by a vanadium-doped semi-insulating substrate and poorly controlled nitrogen implantation for source/drain activation. Overall, the experimental results agree qualitatively with speculations made in the previous research [1]-[10].

Device Design And Fabrication

Figure 1 shows a cross-section of the device structure, fabricated using a five-mask process. Dual-finger devices were fabricated. The starting material was a top 0.5 μm-thick n-type layer on a 1 μm-thick p-type layer, overlaying a Si-face of a 2-inch 8° off-axis vanadium-doped semi-insulating 4H-SiC substrate. The nominal doping/thickness values of the n- and p-layers were 1.4×10^{17} cm^{-3}/0.5 μm and 6×10^{16} cm^{-3}/1 μm, respectively. RIE was performed to etch the top n-type epi-layer in SF_6/O_2 ambient.

E-beam lithography (EBL) was used to define channel length from 0.5 to 1.5 μm. Source and drain regions are box profiles formed by four nitrogen ion implantations. The implantation energies are in the range of 20 to 200 keV and the total dose is 5.4×10^{15} cm^{-2} giving a concentration of 4×10^{20} cm^{-3}. Implant species are activated by annealing for 30 min at 1400^oC in argon. The implantation energies and doses are decided according to Monte-Carlo simulations in the SRIM program. A 3-hour thermal dry oxidation was followed by densification to achieve the gate oxide a total thickness of 350Å. To explore oxide scaling issue, a thin oxide thickness is required. A layer of 1000Å/200Å of Ni/Ti is thermally evaporated and lifted off as n-type contact metal. And the ohmic contacts can be formed under vacuum at 1130^oC for 3 minutes in an infrared gold image furnace.

Sequentially, the second step E-beam lithography (EBL) was employed to define the gate metal. To reduce the gate-to-drain capacitance (C_{gd}) and gate-to-source capacitance (C_{gs}), EBL was also performed to reduce the overlaps, fabricating 0.3μm gate-to-source and gate-to-drain overlaps. A layer of 2000Å/200Å of Au/Ti is thermally evaporated and lifted off as gate metal. Finally, another 2000Å/200Å of Au/Ti layer was thermally evaporated and patterned to serve as gate, drain, and source pads.

Figure 2 shows the small signal model for MOSFETs. For good RF performance, it is needed to reduce the C_{gs} and C_{gd} in order to achieve higher cut-off frequency (f_T) and maximum available power gain frequency (f_{MAX}). Higher Rds and lower parasitic capacitance (Cds) can be obtained by employing a high resistivity substrate.

$$f_T = \frac{g_m}{2\pi C_{gs}\sqrt{1+\omega^2 C_{ds}^2 R_L^2}} \qquad [1]$$

$$f_{MAX} \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})}\frac{1}{\left[4g_{ds}(R_i+R_s+R_G)\right]^{1/2}} = \frac{f_T}{2}\sqrt{\frac{1}{g_{ds}(R_i+R_s+R_g)}} = \frac{f_T}{2}\sqrt{\frac{R_{ds}}{(R_i+R_s+R_g)}} \qquad [2]$$

Results and Discussion

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Figure 3 shows the drain current and (Id)-drain voltage (Vd) characteristics of 4H-SiC MOSFETs with two different channel lengths: (a) L_{ch}=1.5μm, (b) L_{ch}=0.7μm, respectively.

Drain current rose quickly in conjunction with an increase in drain voltage; however, an apparent discrepancy in performance was observed between the two devices. Correspondingly, the unexpected *Id-Vd* characteristic observed in the short-channel nMOSFET device could be attributed to large source/drain resistance and/or short channel effects (SCEs).

As the channel length decreased to submicron dimensions, the fringing field from the drain to the channel further extended to the source region weakening the gate control capability, resulting in apparent SCEs. Initially, to verify these issues, source/drain engineering had to be clarified to verify the *Id-Vd* data required. Contact and sheet resistance was measured as 9.976×10^{-4}(Ωcm^2) and 2350 (Ω/sq), respectively. Device resistance (Ron) from *Id-Vd* characteristics was estimated as $9.7\text{x}10^3$(Ωmm) at Vg =20V, indicating incomplete source/drain activation by nitrogen implantation. Thus, the linear *Id-Vd* curve in the channel without charge saturation was probably the resistance of the large device (Ron) and SCEs. Reduction in resistance by phosphorus implantation [5] has been demonstrated to be one order of magnitude lower than nitrogen implantation. However, it is worth noting that the in-situ annealing process at 650 ^{o}C for the reduction of trap-density in the source/drain region is necessary for SiC devices with phosphorus implantation. Moreover, specific contact resistivity can be reduced to a large degree through a metal contact scheme using evaporated Au/Ti for the phosphorus implantation device without post annealing [6].

Figure 4 shows that DIBL (Drain induced barrier lowering) was the obvious effect of reducing the devices to submicron levels, resulting in increasing subthreshold current. For 0.5 μm devices, an apparent shift in the curve for higher drain bias conditions indicated that the barrier between the source and drain was lower, leading to surface punch-through.

To further clarify the scaling issues, the dependence of transconductance peak on channel length was investigated. Figure 5 shows the transconductance characteristic for SiC nMOSFET with the channel lengths of (a) L=1.5μm, (b) L=0.5μm, respectively.

The gradual deformation of g_m-Vg curve and the drop in the transconductance peak may account for the large source/drain resistance and poor gate leakage. As mentioned previously, the sub-micron MOSFETs, miniaturized by constant field scaling, suffered from large gate leakage and serious SCEs, due to a scaling of the oxide thickness. As shown in Fig. 5, the g_m-Vg characteristic of long-channel nMOSFETs could not be achieved to the peak value due to the thinness of the oxide layer. On the other hand, a large gate leakage current could increase while the gate voltage was applied over 20V. However, the unwanted drain current appeared at Vg=0V in the short-channel nMOSFET because of the punch through effect as drain voltage (Vd) was increased to over 20V. Fortunately, gate leakage could be further reduced through the introduction of a high-quality oxide. These results have demonstrated the importance of well-characterized source-drain region and gate-stack engineering to enhance the transconductance performance in scaled SiC RF MOSFEFs. High-k dielectrics such as HfO_2-based

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insulating stacks for gate-stack engineering have been demonstrated to improve gate insulation [7].

The mobility characteristic of nMOSFET with a channel length of 1.5μm in Fig. 6 shows a peak value of 0.1(cm^2/Vs), which is lower than in the previous study [3]. Because the substantial degradation in mobility is more apparent in the short-channel device, it was not possible to extract the mobility value, because of an unexpected Id-Vg data. In addition, the excess source-drain series resistance caused by nitrogen implantation may have played a dominant role in the degradation of mobility. This suggests that the large drop in voltage originated from source/drain series resistance in the channel decreasing transconductance, resulting in a drop in channel-mobility. On the other hand, the trapping effect from the vanadium-doped semi-insulating layer is another important factor consistent with the previous study [8]. Deep level impurities caused channel carrier trapping and backscattering, which led to a serious degradation in mobility. Therefore, inserting a buffer layer between the substrate and the semi-insulating layer [9] was the alternate way to reduce the trapping effect from the vanadium-doped substrate. Direct observation of these characteristics of transistors makes it clear that the limits of scaling are apparent in oxide breakdown and source/drain resistance.

Small-signal RF characterization of lateral MOSFETs on a semi-insulating substrate with channel lengths ranging from 0.5μm to 1μm was performed on the wafer using a network analyzer. The contribution of contact pads was de-embedded by subtracting the y–parameters of a dummy structure comprising only pads from the y–parameters of the MOSFET. Figure 7 shows the extrinsic current gain h21 and the maximum available power gain (MAG) for the devices of different channel lengths. The extrinsic cutoff frequency for L_{ch}=0.7μm and L_{ch} =0.5μm was 0.7GHz and 0.45GHz, respectively. The MAG frequency for L_{ch}=0.7μm and L_{ch}=0.5μm was 1.5GHz and 0.55GHz, respectively. The main reasons for poor high frequency characteristics were low drive current and low mobility. The related literature has reported that the growth of gate oxides on ion-implanted aluminum material results in high mobility [10] but details of the mechanism remain unclear. The gate-drain overlap capacitance (C_{gd}) and gate-source overlap capacitance (C_{gs}) also strongly influenced the RF characteristics in the scaling of the device. Higher quality oxides would be required to reduce the parasitic capacitance effect to improve high frequency characteristics. In addition, it is worth noting that the optimistic bias point for RF measurement could not be pinpointed due to the influence of SCEs and Ron on the DC characteristics.

Conclusion

In this work, we demonstrated SiC RF MOSFETs on a semi-insulating substrate to produce f_T (0.7GHz) and f_{MAX} (1.5GHz), respectively. The critical aspects of the process were identified and evaluated based on a strategy of device scaling. We concluded that the DC and RF characteristics of nMOSFET are dominated by the device resistance (on-resistance), SCEs, oxide quality, and interface charge trapping effect. Due to the crucial influence of on-resistance on sub-micron devices, low contact resistance and sheet resistance is essential. Secondly, due to the trapping effect, increased effort is required to study vanadium-doped semi-insulating substrates for RF power applications. Thirdly, excellent oxide quality is necessary to increase mobility and breakdown field. The concrete approaches to overcoming these scaling issues have been reported, but these

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approaches would still require verification in future applications. Therefore, device integration for SiC RF MOSFET requires further investigation to fully satisfy the requirements of device scaling.

Acknowledgments

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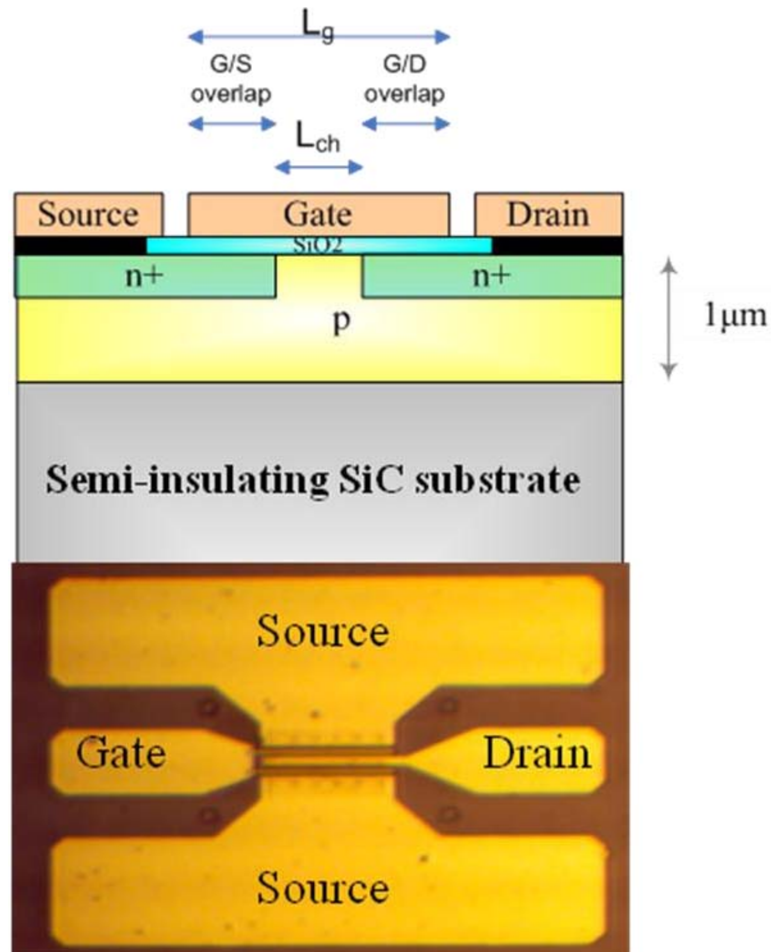

Figure 1. Cross-sectional schematic of the 4H-SiC RF MOSFETs

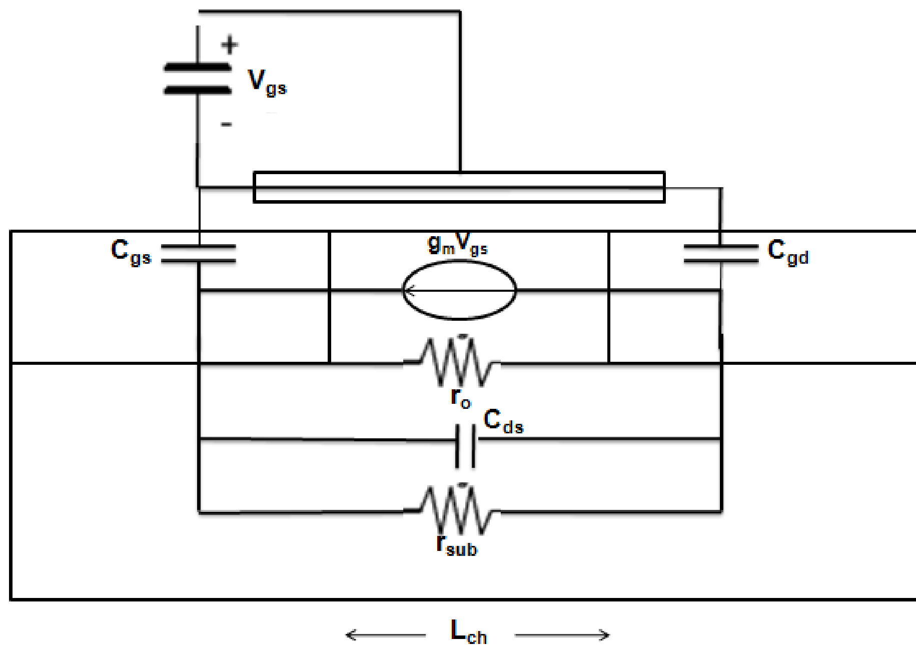

Figure 2. The small signal model of MOSFET.

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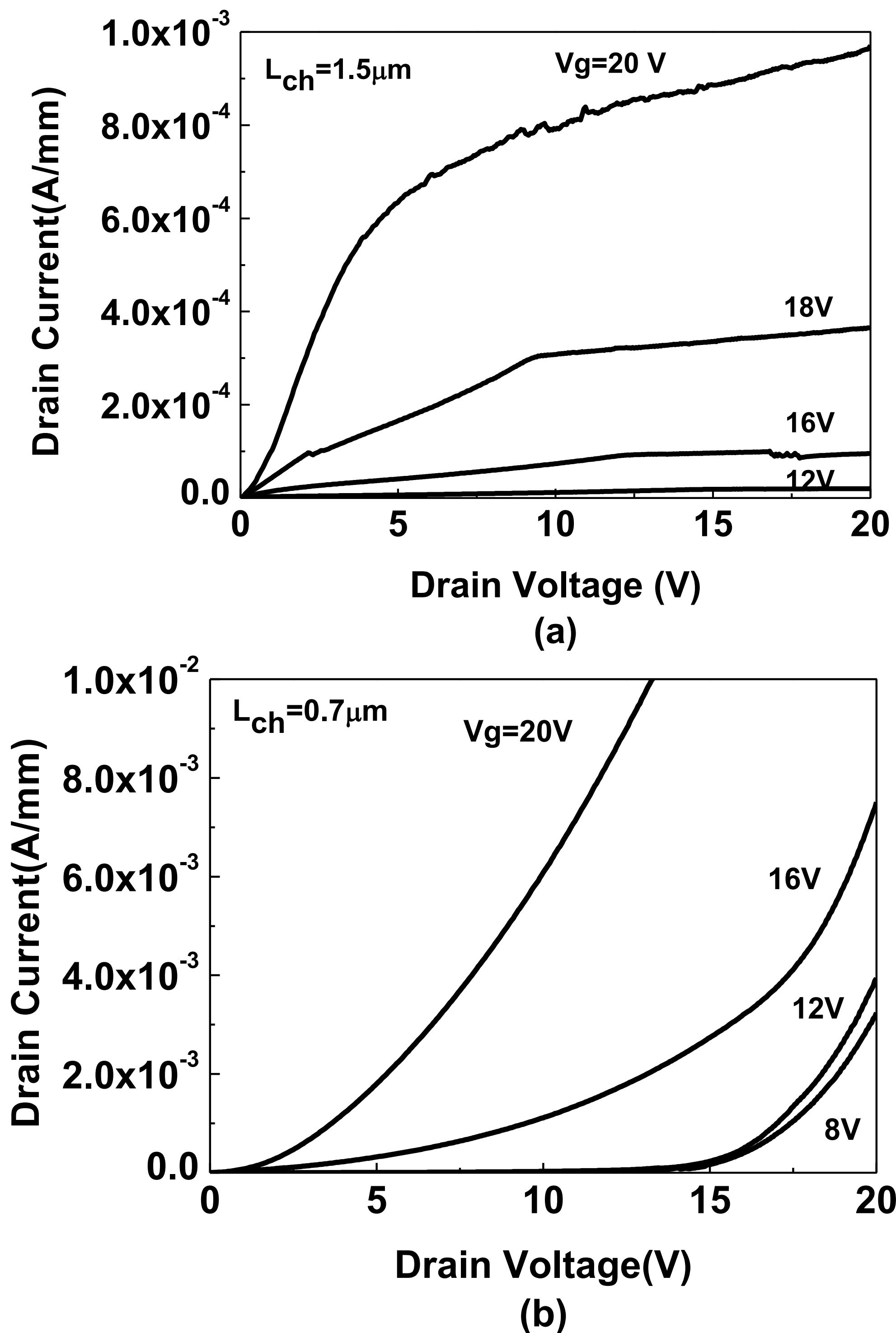

Figure 3. Drain–current as a function of drain voltage for SiC devices with the gate lengths of (a) 1.5μm and (b) 0.7μm.

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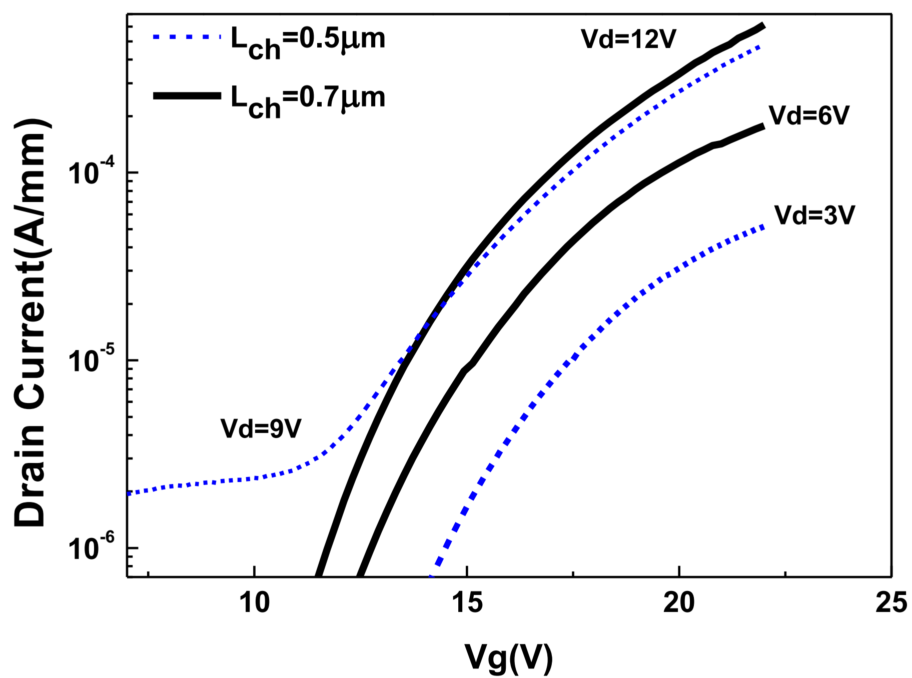

Figure 4. Drain-current as a function of gate voltage with the gate lengths of 0.5μm and 0.7μm.

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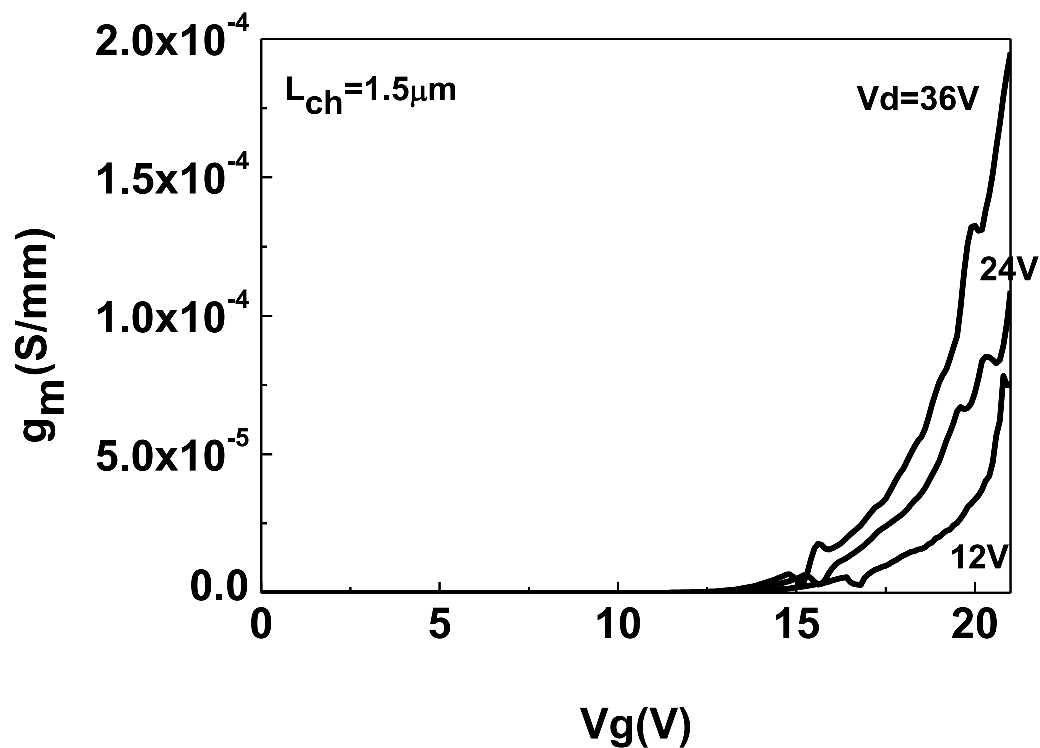
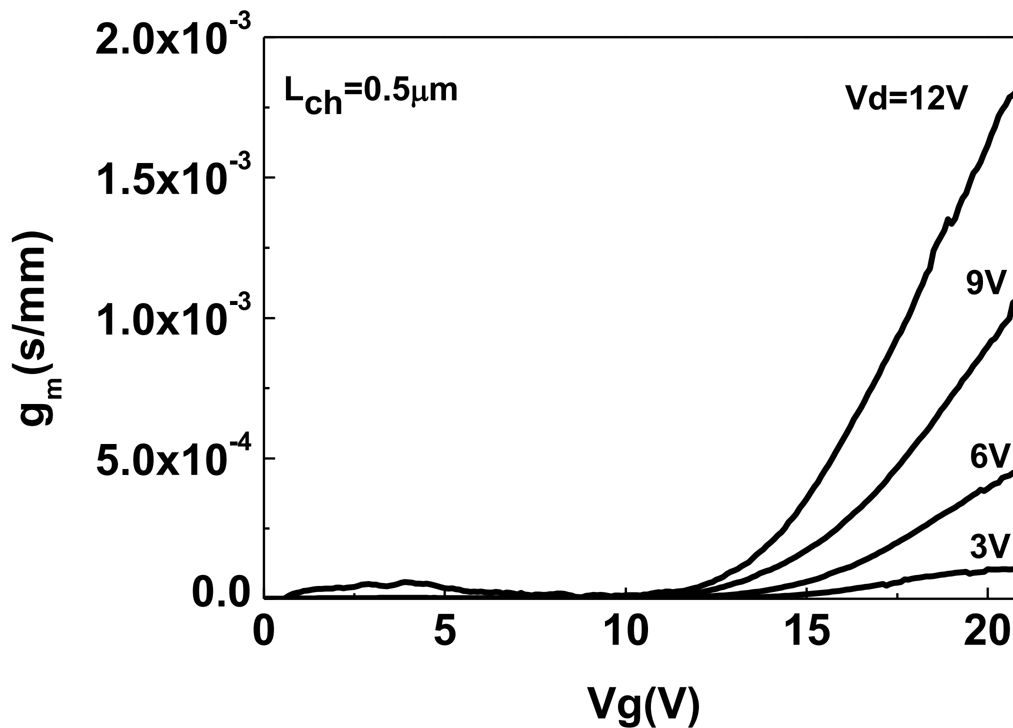


(a)



(b)

Figure 5. Transconductance as a function of gate voltage for SiC devices with the gate lengths of (a) 1.5 and (b) 0.5μm.

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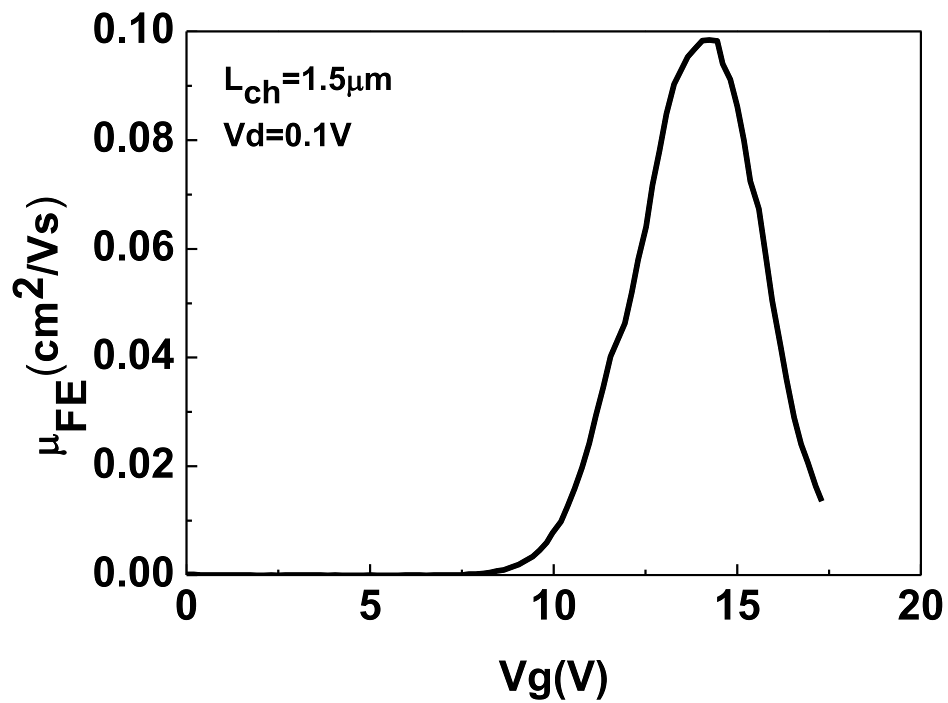

Figure 6. Field-effect mobility as a function of gate voltage.

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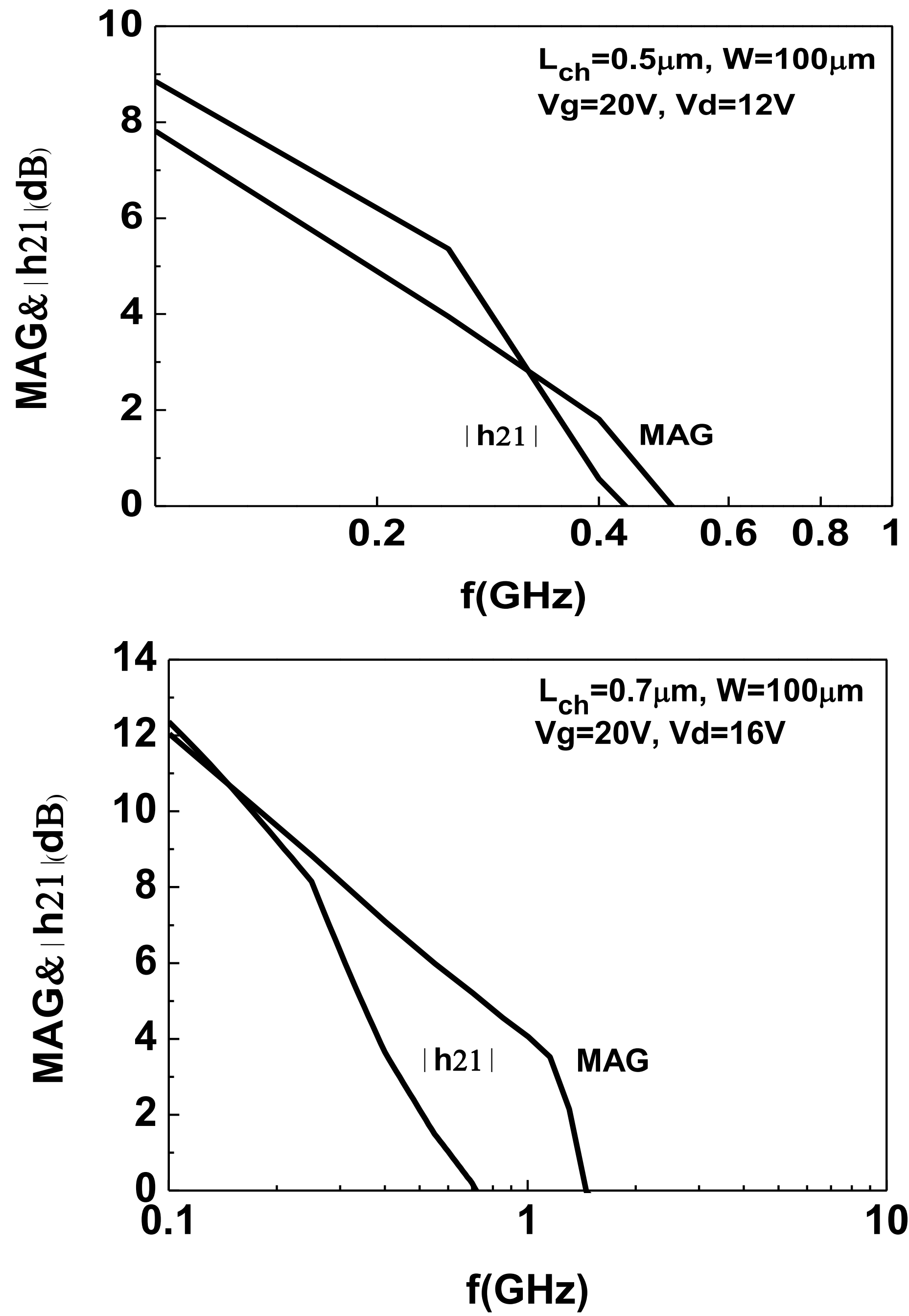

Figure 7. Extrinsic current gain and maximum available power gain for different channel length devices.

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