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Two-stage trigger silicon-controller rectifier (SCR) for radio-frequency (RF) input and output protections in nanometer technologies

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ABSTRACT

In this paper, a two-stage trigger (TST) scheme is proposed to implement a low-capacitance and zero-ohm input resistance electrostatic-discharge (ESD) protection device for nanometer technology applications. Besides the main trigger device diode string, the output transistor can also be used as the trigger device. The dimension of the main trigger device can be reduced for minimizing its capacitance with the additional trigger device. Moreover, the output transistor can be as the driving device without any series resistor. This is because the diode string can help to prevent integrated circuits (ICs) from ESD damage before the primary ESD protection device turns on.

1. Introduction

CMOS technology scaling has resulted in a continuous improvement in radio-frequency (RF) performances of MOSFETs. The cut-off frequency (f_T) over 100 GHz has been demonstrated in the 90 nm CMOS technology [1]. In order not to interfere with the RF signal, a transistor has the maximum loading capacitance limitation [2] and cannot be in series with the resistor. This is because the series resistor will induce the noise, reflection, and increase the power gain loss. Ideal ESD devices for RF input and output protections not only should be low-capacitance devices but also should be zero-ohm resistance devices. With the move into nanometer technologies, however, devices become more vulnerable to the ESD stress than ever due to the ultra-thin oxide (<20 Å), ultra-shallow junction, and short-channel effect [3]. How to develop low-capacitance ESD protection devices to protect the vulnerable output transistors without any series resistors becomes a big challenge in nanometer CMOS technologies.

Although several schemes [4–6] have been demonstrated that allow the RF signal pad to connect the drain or gate of the transistor directly, they all have their own limitations. The diode trigger silicon-control-rectifier (DTSCR) [4] has been demonstrated that can protect the ultra-thin oxide in nanometer technologies. However, its ESD protection capability for the core device (1.0 V) is still unknown. The mutual-protection (MP) scheme [5] is a scheme to enhance the device ESD robustness. Using this scheme, the ESD threshold voltage of output transistor strongly depends on its size. Without enough dimensions, the output transistor cannot own the required ESD level even the MP scheme is used. The semi-self-protection (SSP) scheme [6] is only verified in 0.18 um technologies. However, the maximum current density of the fully silicided transistor decreases from 5.3 mA/μm to 1.3 mA/μm as the technology switches from the 0.18 μm process to the 45 nm process (Fig. 1). Because of lacking the enough self-protection capability, the output transistor's ESD capability by using the SSP scheme is still questionable in nanometer technologies.

In [5], the MP scheme can be used to improve the ESD performance of the output transistor to compensate its self-protection capability decrease. In [6], if the self-protection capability of the output transistor is recovered, the SSP scheme still can work well in nanometer technologies. From the above, a new ESD structure, which combines MP and SSP schemes, is proposed for RF output protection in nanometer technologies [7]. Since the new ESD structure includes two different kinds of trigger devices and one primary ESD device (SCR), it is called two-stage trigger (TST) ESD protection device.

In this work, the DTSCR, SSP-ESD device and TST-ESD device are investigated by using the 45 nm technology to study the influence of the trigger device on the protection capabilities of these ESD devices for core devices.

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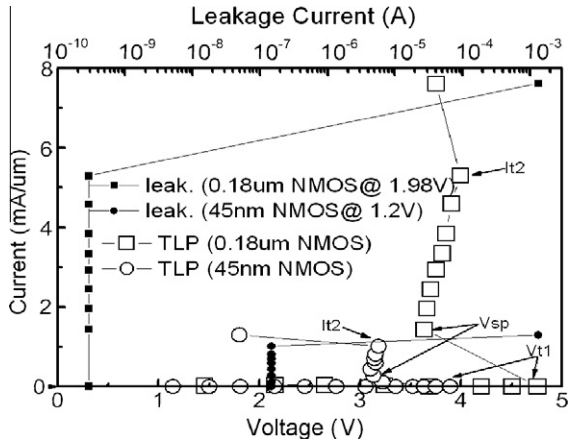

Fig. 1. High current IV characteristics of fully silicided NMOSFET for 0.18 μm and 45 nm technologies.

2. Device structures

The process used to fabricate the devices is the 45 nm CMOS technology in 1.0 V/1.8 V and all devices are applied only for 1.0 V operations with 16 Å gate oxide thicknesses. In this study, the main difference of the three test structures is the trigger device. For positive ESD stresses, all test structures use the SCR as the primary ESD protection device; for negative ESD stresses, the diode (D_A) from the *n*-type well (NW) to P-substrate is applied. All the three test structures are shown in Figs. 2, 5, and 8, respectively. In addition, there is a P+ guard-ring, an NW guard-ring and one power clamping protection device between the power terminal (V_{CC}) and the ground terminal (V_{SS}). Combined with the two guard-rings and power clamping device, all test structures can provide ESD protections for ESD four different zapping modes [6].

2.1. Diode-trigger SCR (DTSCR)

Fig. 2 shows the layout and schematic diagrams of the DTSCR [4] and one output NMOSFET transistor in 64 μm total channel width. The DTSCR has one kind of trigger device, which is three-stage diode strings (TSDSs) in parallel and located at outside the primary ESD protection device (SCR). If the applied voltage is higher than the turn-on threshold voltage of the TSDS, the diodes act as the pnp bipolar transistors (D1–D3 in Fig. 2b) to inject the emitter currents into the P-substrate to raise the substrate potential. As the potential voltage (V_{sub}) of the under-SCR cathode-substrate is raised higher than 0.7 V, the p–n junction between the cathode and P-substrate is forwarded to cause the npn bipolar (npn_s) turn on. Thus, electrons injected from the npn_s are collected by the SCR anode to pull down the NW potential (V_{NW}) to induce the pnp bipolar (pnp_s) turn on. When both npn_s and pnp_s turn on, the SCR enters the latch-up state [8] (SCR turns on).

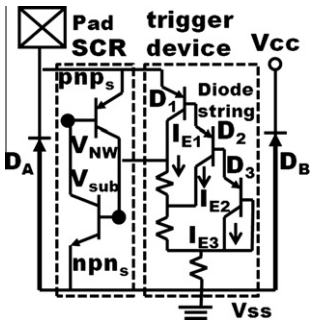

Fig. 2b. The schematic diagram for DTSCR.

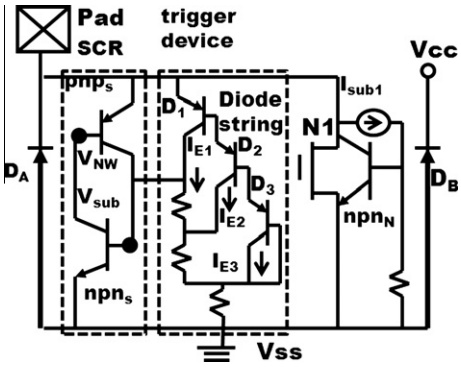

Fig. 2c. The schematic diagram for DTSCR with output transistor (N1).

Fig. 3 shows the high current IV characteristics of the DTSCR (Fig. 2b) under the 100*n* s transmission line pulse (TLP) stress events. The trigger-on voltage (V_{t1}), the snapback voltage (V_{sp}) and the maximum current before damage (secondary breakdown current, I_{t2}) of the DTSCR are 4.4 V, 1.6 V and 1.42 A, respectively. If the device leakage current (Leak.) reaches 1 μA, the device status is decided as FAIL. Before the failure, the device current is I_{t2}. Fig. 4 shows the high current *I–V* characteristics of only N1 and DTSCR combined with the clamping device N1 (Fig. 2c). Both devices are under 100*n* s TLP stresses. V_{t1}, V_{sp}, I_{t2} of DTSCR with N1 are similar to those of N1, but much different from those of DTSCR (Fig. 3). This implies that DTSCR cannot be turned on for protecting N1 since its V_{t1} is larger than N1's V_{t1} (3.95 V). From ESD test results, DTSCR can pass HBM 2.5 KV and MM 100 V. However, DTSCR with N1 cannot pass HBM 500 V or MM 50 V.

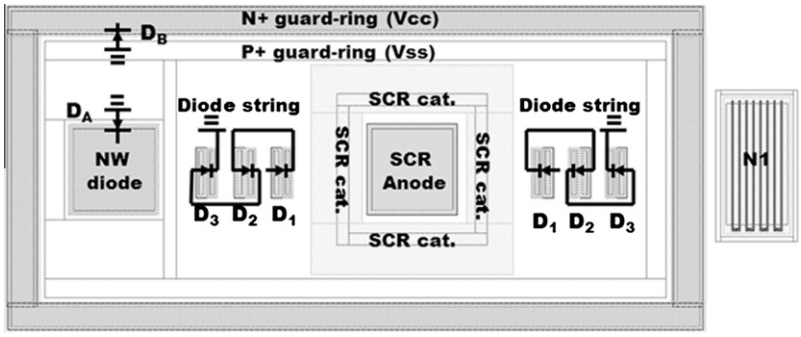

Fig. 2a. The layout of DTSCR with the output transistor (N1).

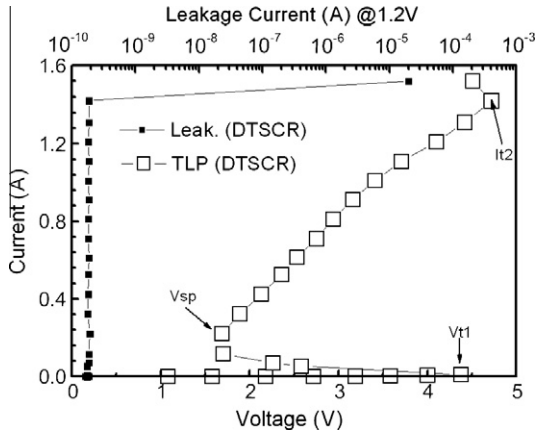

Fig. 3. High current *I–V* characteristics of the DTSCR.

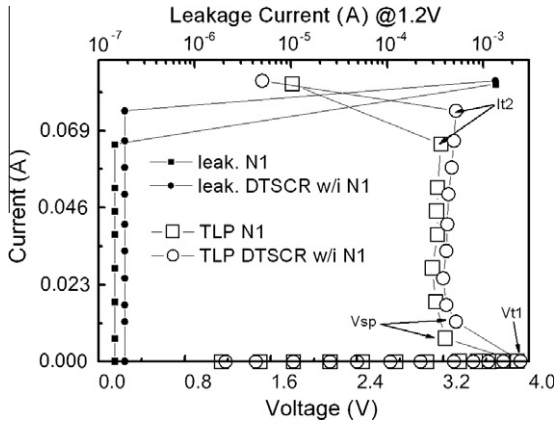

Fig. 4. High current *I–V* characteristics of the N1 and the DTSCR with the N1 under the 100*n* s TLP stresses.

2.2. Semi-self-protection (SSP) ESD device

Fig. 5 shows the layout and schematic diagram of the SSP-ESD device. Unlike the test structure in Fig. 2, N1 is moved inside the guard-rings to act as the trigger device for SCR [6]. As the applied voltage is higher than the device breakdown voltage, the avalanche breakdown occurs at the drain junction to generate the substrate current (I_{sub}) into P-substrate. I_{sub} flows through the substrate resistor (R_{sub}) to raise the substrate potential (V_{sub}). Thus, the forward source junction results in the source terminal injecting the

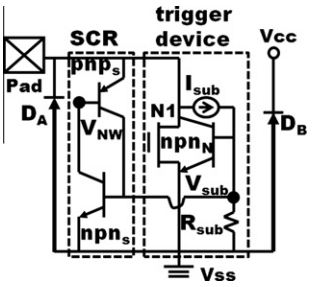

Fig. 5b. The schematic diagram of the SSP-ESD device.

electrons. Then, the injected electrons flow through the channel and the high field drain region for adding the impact-ionization probabilities. It generates the I_{sub} to keep forwarding the source junction to inject the electrons. These actions form a positive-feedback loop, corresponding to the npn bipolar turned on. Subsequently, the SCR cathode could be forwarded to cause its junction injecting the electrons. Finally, the SCR anode triggers the SCR on if the I_{sub} is large enough.

Fig. 6 shows that SSP enters the higher voltage (~3 V) and the lower current (~150 mA) region first and then switches into the lower voltage (~2 V) and higher current (~200 mA) region. Fig. 7 shows the high current *I–V* characteristics of the SSP-ESD device versus the total width of the N1. For SSP-ESD device with a 64 μm total channel width N1, its behavior is similar to a NMOSFET. Its V_{t1} and V_{sp} are the same as those of N1 in Fig. 4, but its I_{t2} (275 mA) is slightly higher than N1's I_{t2} (68 mA). This implies that the SSP scheme cannot work well in the 45 nm technology for the small total width output transistor since the generated I_{sub} is not large enough to turn on SCR completely. From ESD test results, it only can pass HBM 0.5 KV. However, for SSP-ESD device with a 128 μm total width N1, its behavior is similar to a SCR, which V_{sp} is 2.3 V and I_{t2} is increased to 1 A. This implies that the SSP scheme can work well in the 45 nm technology if large total channel width output transistors are adopted. From ESD test results, SSP with 128 μm width N1 can pass HBM 2 KV and MM 100 V.

2.3. Two-stage trigger (TST) ESD device

Although the TSDS cannot make the V_{t1} of DTSCR smaller than that of the core transistor, it can make the core transistor more robust [4]. Adding the TSDS into the SSP-ESD device, a new ESD device is proposed as shown in Fig. 8, which includes two different kinds of trigger devices (TSDS and NMOSFETs (N1)). The TSDS

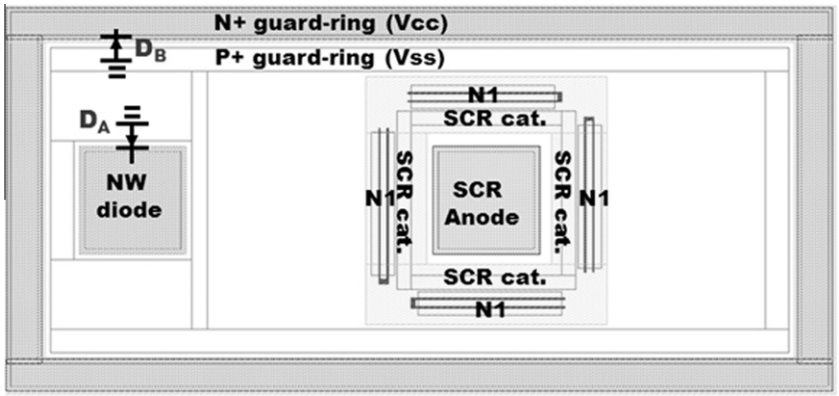

Fig. 5a. The layout of the SSP-ESD device.

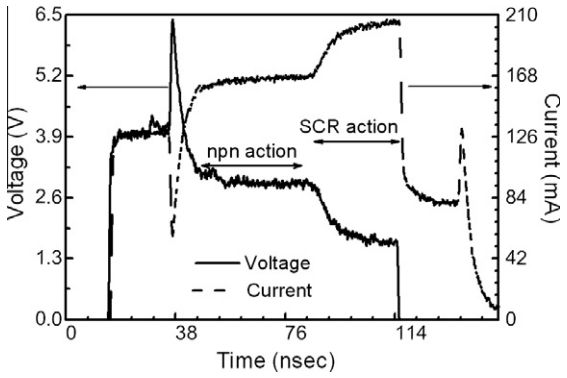

Fig. 6. Voltage and current waveforms of the SSP-ESD device with N1 in 128 μm total width under 1st snapback TLP in Fig. 5.

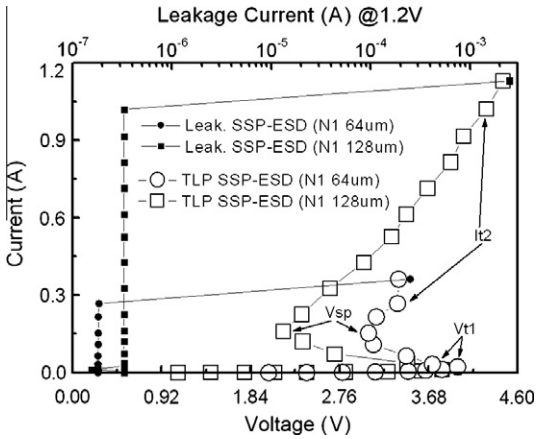

Fig. 7. High current *I–V* characteristics of SSP-ESD device vs. the total width of N1 in Fig. 5.

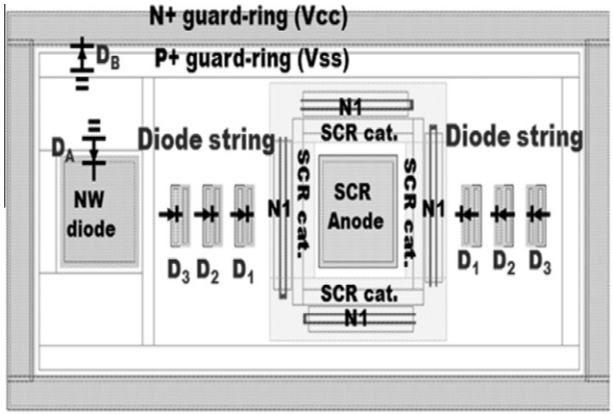

Fig. 8a. The layout of TST-ESD device.

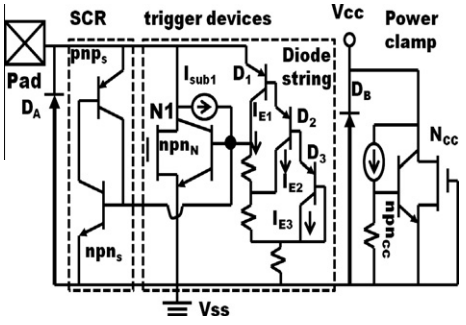

Fig. 8b. The schematic diagram of TST-ESD device.

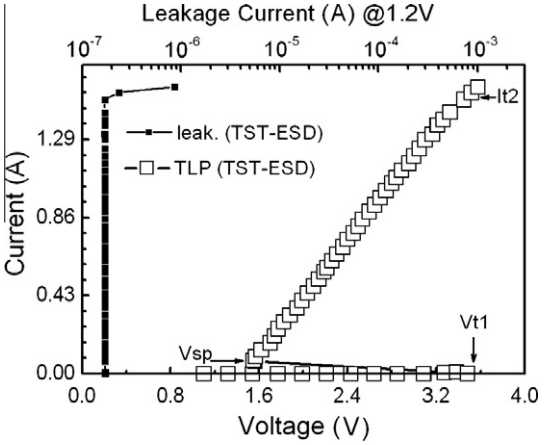

Fig. 9. High current *I–V* Characteristics of the TST-ESD device under the 100*n* s +TLP/V_{SS} stresses.

can provide the emitter currents (I_{E1}, I_{E2}, and I_{E3}) to the p-substrate. This makes the parasitic npn bipolar (npn_N) of the N1 turn on for preventing IC from ESD damage before SCR turns on.

Then, the npn_N also can provide the additional substrate current (I_{sub1}) to the p-substrate. With two different kinds of substrate currents, the SCR of the new ESD device can be turned on more easily than that of the DTSCR or SSP-ESD device. Fig. 9 shows that both V_{t1} and V_{sp} of the new ESD device under positive TLP stresses with grounding V_{SS} (+TLP/V_{SS}) are smaller than those of N1 in Fig. 4. Thus, the SCR of the new ESD protection device can effectively protect the core transistor against ESD damage without any series resistor between the bonding pad and output driving circuits.

Fig. 10 shows that after a 3.5 KV HBM zapping event, the damages of the new ESD device occur at SCR, but do not occur at N1. It is proved that the new ESD device can work well for RF output ESD protections in nanometer technologies. Since there are two trigger devices and ESD devices turn on one by one, this new ESD device is called as two-stage trigger (TST) ESD device.

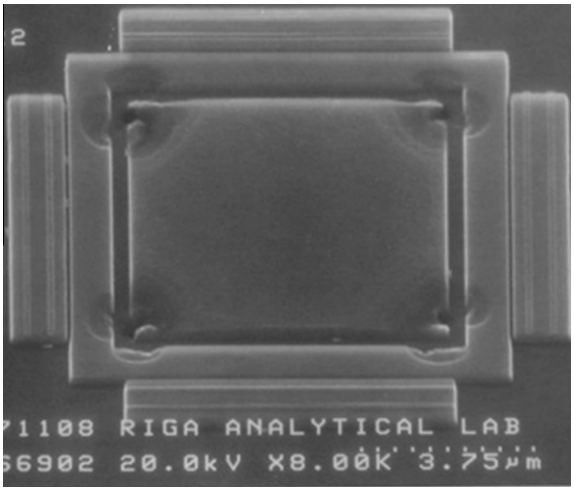

Fig. 10. After a 3.5 KV HBM zapping event, damage sites of TST ESD device at SCR, not at N1.

3. TST-ESD device characteristics and applications

For TST-ESD devices, there are many silicon data in this study. There are the high current *I–V* characteristics, DC *I–V* characteristics, high-frequency characteristics and applications which are described in the below sub-sections. In Sections 3.1–3.3, N1 total channel width size is 64 μm.

3.1. High current I–V characteristics of the TST-ESD device

Although the TST-ESD device is designed for ±ESD/V_{SS} (IC PAD under ±ESD stresses and V_{SS} is grounded) protections, it can also be for ±ESD/V_{CC} (V_{CC} is grounded) zapping as it cooperates with the power clamp device (N_{cc} in Fig. 8b). Figs. 9 and 11 show the high current *I–V* characteristics of the TST-ESD device under +TLP/V_{SS} stresses and three other stress modes, −TLP/V_{SS}, +TLP/V_{CC}, and −TLP/V_{CC}, respectively. Except −TLP/V_{SS} stress mode, three other curves have the snapback phenomena caused by SCR or the npn bipolar turning on.

By comparing Figs. 9 and 3, the I_{t2} (1.52 A) of the TST-ESD device under +TLP/V_{SS} stresses is slightly higher than DTSCR's I_{t2} (1.42 A). Moreover, for +ESD/V_{SS} mode, the ESD threshold voltages of DTSCR are HBM 2.5 KV and MM 100 V, but the ESD threshold voltages of the TST-ESD device can be improved to HBM 3 KV and MM 150 V.

From Fig. 8, the main discharge component for −TLP/V_{SS} stress is the diode D_A since it will be forwarded to sink the −TLP/V_{SS} current as the Pad applied voltage is below −0.7 V. Fig. 11 shows that the current rises with the applied voltage until the current equals to I_{t2} (1.5 A). For this zapping mode, the TST-ESD device can pass HBM 3 KV and MM 150 V.

As the V_{CC} is grounded, from Fig. 8, the diode D_B with the TSDS, N1 and SCR will be turned on for sinking the +TLP/V_{CC} current. The diode D_A with the npn bipolar (npn_{cc}) of the power clamp device will be turned on for sinking the −TLP/V_{CC} current. Thus, the curve for +TLP/V_{CC} in Fig. 11 represents the combination characteristics of the diode and SCR. The curve for −TLP/V_{CC} in Fig. 11 represents the combination characteristics of the diode and npn bipolar. Both the I_{t2} values for the two stress modes are equal to 1.5 A since they are determined by the weakest components in their discharge paths. Compared to the diode D_B and the power clamp device, the SCR with N1 and the diode D_A are more vulnerable since their dimensions are smaller. Thus, the ESD threshold voltages of the TST-ESD device for +ESD/V_{CC} and −ESD/V_{CC} zapping modes are the same as those for +ESD/V_{SS} and −ESD/V_{SS} zapping modes, which are all equal to HBM 3.0 KV and MM 150 V.

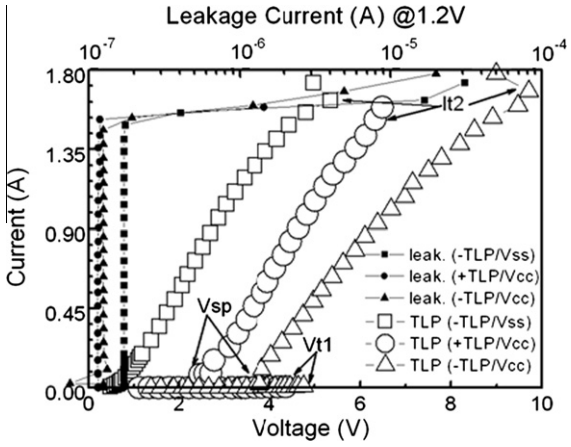

Fig. 11. High current *I–V* Characteristics of the TST-ESD device under the 100*n* s −TLP/V_{SS}, +TLP/V_{CC}, and −TLP/V_{CC} stresses.

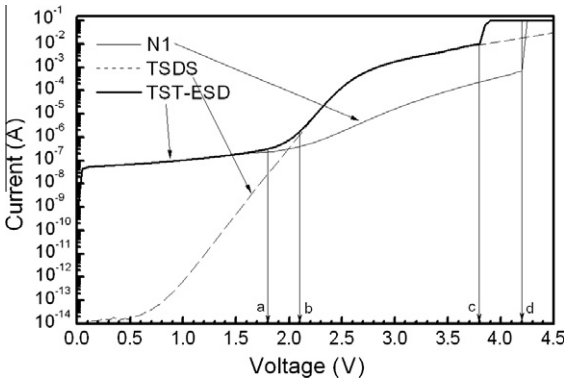

Fig. 12. DC *I–V* characteristics of the NMOSFET (N1), three-stage diode string (TSDS) and TST-ESD protection device in Fig. 8.

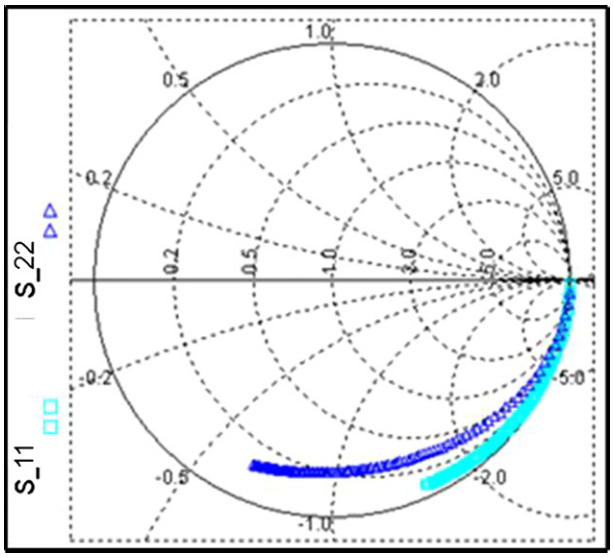

Fig. 13a. Smith-chart representation of S_{11} and S_{22}.

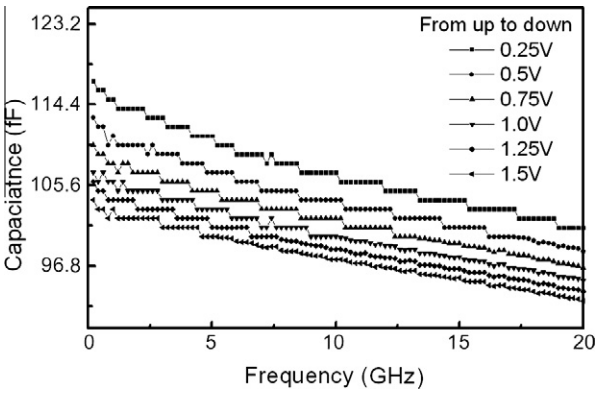

Fig. 13b. The extracted capacitance based on S_{11} for TST-ESD device.

3.2. DC I–V characteristics of the TST-ESD device

Fig. 12 shows the DC *I–V* characteristics of a NMOSFET N1, a TSDS and a TST-ESD device. From the three curves, most currents of the TST-ESD device come from N1 since the TSDS current is too small and can be neglected as the applied voltage is below 1.7 V. This implies that the TSDS does not increase

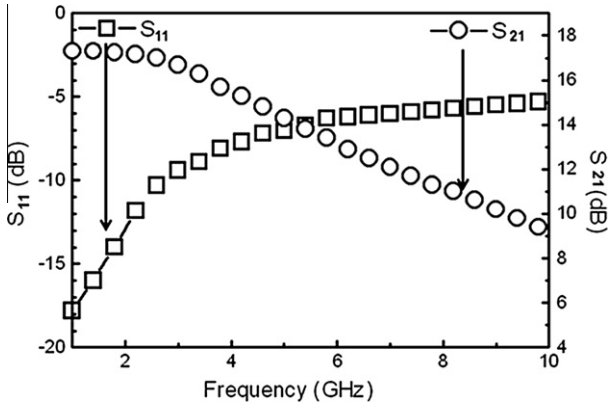

Fig. 14. Measured S-parameters (S_{11} and S_{21}) of the TST-ESD device in Fig. 8.

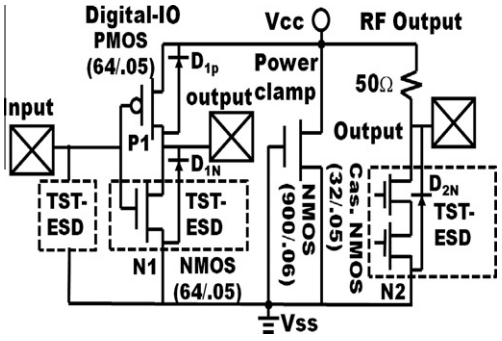

Fig. 15. Schematic diagrams for digital IO and RF output ESD protection.

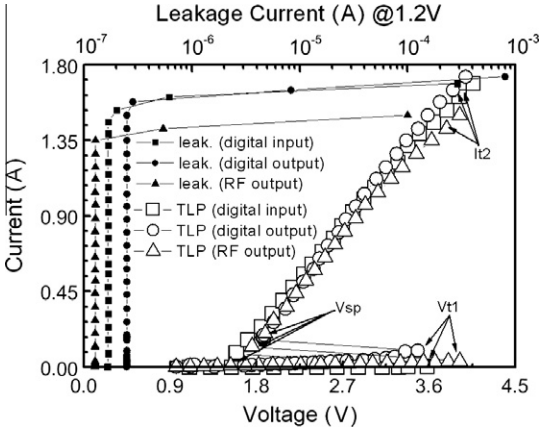

Fig. 16. High current *I–V* characteristics for the digital input pad, output pad and RF output pad under +TLP/V_{SS}.

the leakage current of the output transistor under IC normal operation (voltage $\leqslant$ 1.2 V). As the applied voltage is beyond the turn-on threshold voltage of the TSDS (2.1 V), the current of the TSDS is in the several orders of magnitude larger than that of N1. Thus, most currents of the TST-ESD device will come from the TSDS, not from N1. It can also be found that the currents of the TST-ESD device and the N1 jump to the clamp current 100 mA at 3.8 V and 4.2 V, respectively. The voltages are almost equal to their V_{t1} values measured from the TLP. This demonstrates that the TSDS can provide the large current to make the npn bipolar and SCR of the TST-ESD device turn on more

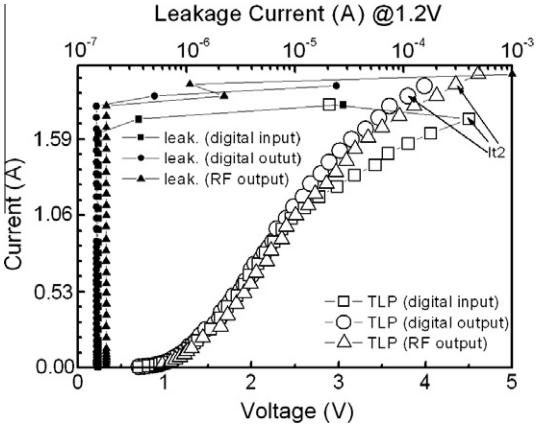

Fig. 17. High current *I–V* characteristics for the digital input pad, output pad and RF output pad under −TLP/V_{SS} stresses.

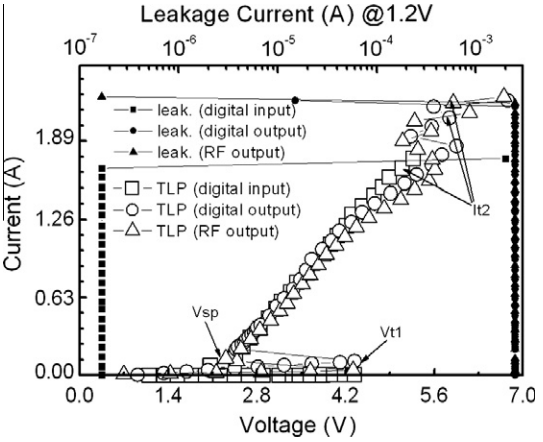

Fig. 18. High current *I–V* characteristics for the digital input pad, output pad and RF output pad under +TLP/V_{CC} stresses.

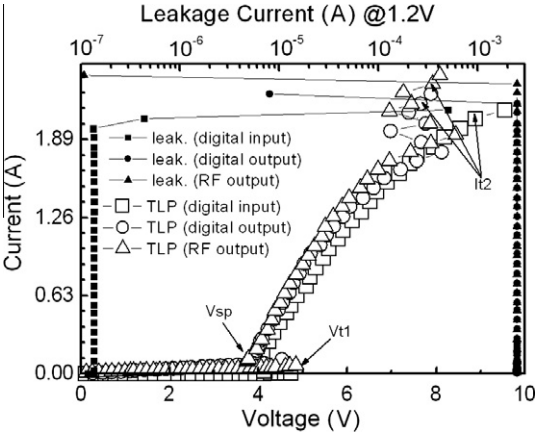

Fig. 19. High current *I–V* characteristics for the digital input pad, output pad and RF output pad under −TLP/V_{CC} stresses.

easily, resulting in the smaller V_{t1}. For a NMOSFET, however, it is without the large current to turn on the parasitic npn bipolar unless the applied voltage is beyond the device avalanche breakdown voltage. It can be found that the current of N1 is still below 1 mA at 4.1 V.

Table 1
ESD test results for test pattern in Fig. 1.

HBM/MM	+ESD/V_{SS}	−ESD/V_{SS}	+ESD/V_{CC}	−ESD/V_{CC}
TST-ESD	3 KV/150 V	3.5 kV/200 V	3 KV/150 V	3.5 KV/200 V
Dig. input pad	3 KV/150 V	3.5 KV/200 V	3 KV/150 V	3.5 KV/200 V
Dig. output pad	3 KV/150 V	3.5 KV/200 V	4 KV/200 V	3.5 KV/200 V
RF output pad	2.5 KV/150 V	3.5 KV/200 V	2.5 KV/150 V	3.5 KV/200 V

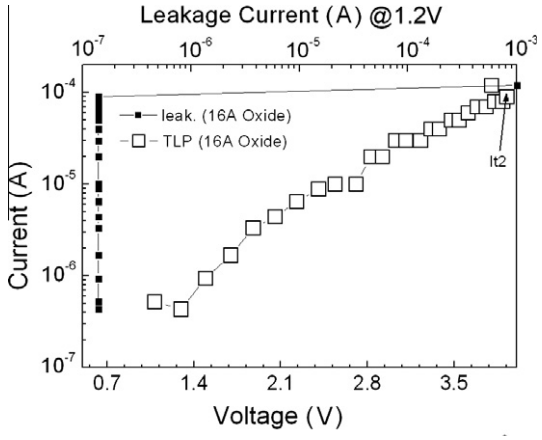

Fig. 20. High current *I–V* characteristics for a 16 Å oxide under the 100*n* s TLP stresses.

3.3. High-frequency characteristics of the TST-ESD device

In order to measure the high frequency characteristics and capacitances of the SSP-ESD device, ground-signal-ground (GSG) pads are taken into experiments. The apparatus used to measure the S-parameters is HP-8510C network analyzer. The measured frequency is from 0.2 GHz to 20 GHz and the DC reversed-biased voltages are from 0 V to 1.5 V.

Fig. 13 shows the Smith-chart representations of S11 and S22 and the extracted capacitance of the TST-ESD device. The extracted capacitance of the TST-ESD biased on 0.25 V and 0.2 GHz is 118fF, which only differs from the spice simulated value 116.4 fF in 1.6 fF. From the spice simulation, the capacitances for the NMOSFET N1, SCR with diode D_A and TSDS are 71.6 fF, 42.4 fF, and 2.4 fF, respectively.

The measured S-parameters (S11 and S21) of the TST-ESD device in Fig. 8 versus the frequency are shown in Fig. 14. It can be found that the TST-ESD device exhibits the good input matching, which S11 is within −20 dB when the frequency is below 10 GHz. The power gain (S21) for TST-ESD device are 17.4 dB at 2 GHz and 13.5 dB at 5.8 GHz, respectively. Excluding the N1, the power gain loss caused by the ESD devices is only 0.8 dB.

3.4. Applications for TST-ESD device

Fig. 15 shows the schematic diagram of a digital input/output circuit (IO), and a RF output (differential amplifier) [9] to evaluate the protection capability of the TST-ESD device. The NMOSFET (N1) of the digital output and cascode NMOSFET (N2) of the RF output are embedded in the TST-ESD architecture, but there is only one power clamp in Fig. 15. From the Section 3.1, a single TST-ESD device can provide the current path to sink the ESD charges for any zapping mode as it cooperates with the power-clamp device. For digital input pad, there are no other ESD discharge components except the TST-ESD device from Fig. 15. Hence, its discharge behavior (Figs. 16–19) and ESD failure threshold voltages (Table 1) for all zapping modes are the same as those of the TST-ESD device. No matter what kinds of the input components (in Fig. 15) are, they all cannot sink the high ESD currents except the TST-ESD device. Then, the digital IO and RF output under the four kinds of ESD zapping modes can be depicted as follows.

For +ESD/V_{SS} mode, most ESD currents flow from the pad through the SCR of the TST-ESD device to V_{SS}. It can be seen that the *I–V* curves of the Fig. 16 are similar to those of the TST-ESD device as shown in Fig. 9. The V_{t1} values, I_{t2} values and ESD threshold voltages of the digital output and input are almost the same as those of the TST-ESD device. This implies that the TST-ESD device also can effectively protect the ultra-thin gate oxide since its V_{t1} and V_{t2} are smaller than the breakdown voltage (3.95 V) of a 16 Å oxide as shown in Fig. 20. For RF output, its V_{t1} is larger than the TST-ESD device's V_{t1} and its I_{t2} and ESD performance are slightly smaller than those of the TST-ESD device. It is because that a cascode NMOS has the higher V_{t1}, smaller I_{t2} and lower ESD threshold voltage compared to a NMOSFET [10,11].

A. For –ESD/V_{SS} mode, most ESD currents flow from V_{SS} through the diode D_A of the TST-ESD device to the zapped pad. For the digital output pad, some ESD currents flow through the parasitic diode D_{1N} of NMOS (N1) to the zapped pad; for the RF output pad, some ESD currents flow through the parasitic diode D_{2N} of cascode NMOS (N_2) to the zapped pad. Fig. 17 shows that all currents follow the exponential trajectory to rise as the voltages are beyond 0.7 V. Since both the digital output and RF output have the additional current paths to sink ESD currents, their I_{t2} and ESD threshold voltage are higher than those of the TST-ESD device.
B. For +ESD/V_{CC} mode, most ESD currents flow from the pad through SCR of the TST-ESD device and the parasitic diode of power-clamp device to V_{CC}. For the digital output pad, some ESD currents flow through the diode D_{1P} of PMOS (P1) to V_{CC}; for the RF output pad, some ESD currents flow through the 50 Ω resistor to V_{CC}. However, the dissipated ESD currents are small compared to the SCR currents. Fig. 18 shows that the discharge behaviors of the output pads for this mode are like a SCR with a diode. The V_{t1} and V_{sp} are higher than those of the TST-ESD device under +TLP/V_{SS} stresses in 0.7 V. With the additional current paths, the digital output can get higher I_{t2} and obtain a higher ESD threshold voltage compared to those of the TST-ESD device. Since the resistor current is too small if compared to the SCR current, the ESD failure threshold voltages of the RF output for this mode are the same as those for +ESD/V_{SS} zapping mode.
C. For –ESD/V_{CC} mode, most currents flow from V_{CC} through the parasitic npn bipolar of the power clamp device and the diodes D_A of the TST-ESD device to the pad. Fig. 19 shows that the behaviors of the output pads during –TLP/V_{CC} stresses are like an npn bipolar with a diode, which V_{t1} and V_{sp} are about 5 V and 3.8 V, respectively. Similar to the +ESD/V_{CC} mode, the current flowing through the 50 Ω resistor of the RF output is too small and can be neglected compared to the npn bipolar current. Hence, the ESD failure threshold

voltages for this zapping mode are all the same no matter the structures are the TST-ESD device, digital input, digital output or RF output.

4. Conclusion

The two-stage trigger (TST) scheme is better than the single-stage trigger scheme for the core device protections in the nanometer technologies. It does not induce the leakage issues under the IC normal operations and can reduce the ESD device V_{t1}. TST device V_{t1} is smaller than the protected device V_{t1} and the breakdown voltage of the ultra thin oxide ($\leqslant$20 Å). Moreover, it allows the RF transceiver and receiver to connect to the pad directly.

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