Temperature Dependence of Electron Mobility on Strained nMOSFETs Fabricated by Strain-Gate Engineering

Tien-Shun Chang, Tsung Yi Lu, and Tien-Sheng Chao

***Abstract*—An effective electron mobility improvement that uses strain-proximity-free technique (SPFT) has been demonstrated using strain-gate engineering. The electron mobility of nMOSFETs with SPFT exhibits a 15% increase over that of counterpart techniques. The preamorphous layer (PAL) gate structure on the SPFT showed a further performance boost. The electron mobility exhibits a 52% improvement in nMOSFET using a combination of SPFT and PAL gate structure. Furthermore, the gain in electron mobility in the SPFT in combination with PAL gate structure decreases at high temperatures. Gate dielectric interface states and ionized gate impurities inducing carrier scattering will play important roles when operating devices under high-temperature conditions.**

***Index Terms*—Mobility, nMOSFETs, strain, temperature.**

I. Introduction

FOR the development of sub-32-nm CMOS technology [1], mobility improvement by strain engineering will be limited by the narrowing gate space and scaling down of poly-Si gate thickness [2]. Stressor volume limitation and process integration issues are the key challenges for boosting performance in circuit applications. Stress memorization technique (SMT) has been reported to improve electron mobility in nMOSFETs and has been widely studied using different methods [1]–[4]. However, most previous studies have demonstrated the performance boost without considering the scalability of the gate space in high-density circuits. Longitudinal tensile stress becomes limited as the stressor volume reaches its saturation point, causing performance degradation [5].

Strain-proximity-free technique (SPFT) has been shown to offer performance improvement without the limitation of stressor volume in high-density CMOS circuits [6]. In this letter, we demonstrate electron mobility and drain current improvement in nMOSFETs by using SPFT in combination with a preamorphous layer (PAL) gate structure. Furthermore, we found that the additional thermal annealing process (two-step annealing processes) leads to greater stress into the channel. The temperature dependence of electron mobility in the strain-gate structure is also discussed. In order to extend the applications of devices operating across wide temperature ranges, analysis of the electrical properties at various temperatures is required. Phonon scattering dominating electron mobility at high temperatures by lattice vibration is a well-known mechanism in Si. We have found that the gain in electron mobility in SPFT in combination with PAL gate structure decreases at high temperatures. Gate dielectric and Si interface properties are investigated to explain this phenomenon.

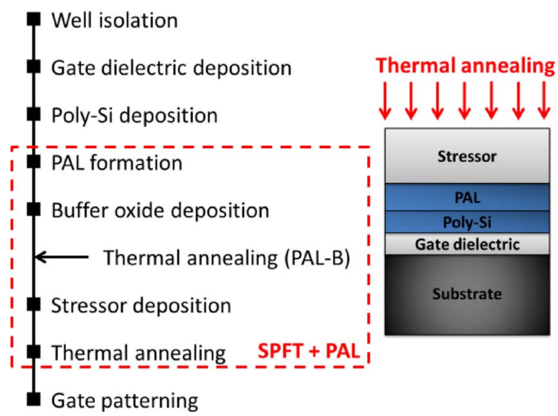

Fig. 1. Process flow for SPFT.

II. Experiment

nMOSFETs were fabricated on 6-in wafers with a resistivity of 15–25 $\Omega \cdot$ cm. Grown in a vertical furnace are 2.0 ± 0.1-nm gate oxide and 200-nm poly-Si. The process flow of SPFT, proposed in order to introduce stress into the channel, is shown in Fig. 1. Before patterning of the poly-Si gate, the SPFT was processed by high-tensile stressor deposition, rapid thermal annealing using spike annealing at 1050 °C, and stressor removal processes. The stressor used in the SPFT was a high-tensile thermal CVD SiN film of 100-nm thickness. The stress level of this film is close to 1.3 GPa. The PAL gate structure is proposed by PAL (PAL-A) in gate using an implantation process. It was inserted into the SPFT process after poly-Si deposition [7]. The dosage split of the As is [40 keV, 5×10^{15} cm^{-2}]. The PAL combines a two-step annealing process (PAL-B) with SPFT, which, inserted after the stressor buffer oxide deposition, can bring greater stress into the channel. Dry

Manuscript received October 15, 2011; revised April 4, 2012; accepted April 6, 2012. Date of publication May 2, 2012; date of current version June 22, 2012. This work was supported by the National Science Council, Taiwan, under Contract 100-2221-E-009-012-MY3. The review of this letter was arranged by Editor C. Bulucea.

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Digital Object Identifier 10.1109/LED.2012.2194982

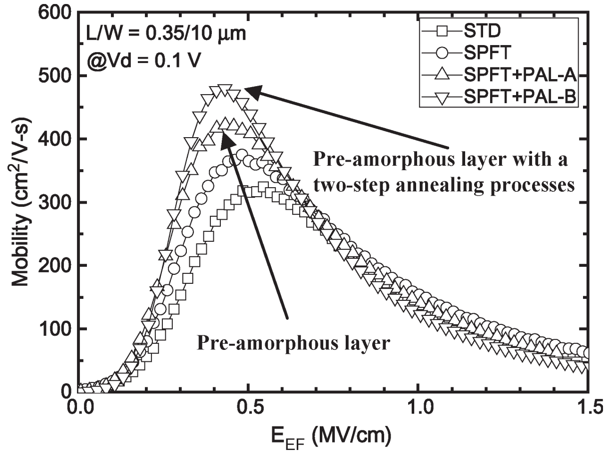

Fig. 2. nMOSFET electron mobility for STD, SPFT, SPFT with PAL-A, and SPFT with PAL-B.

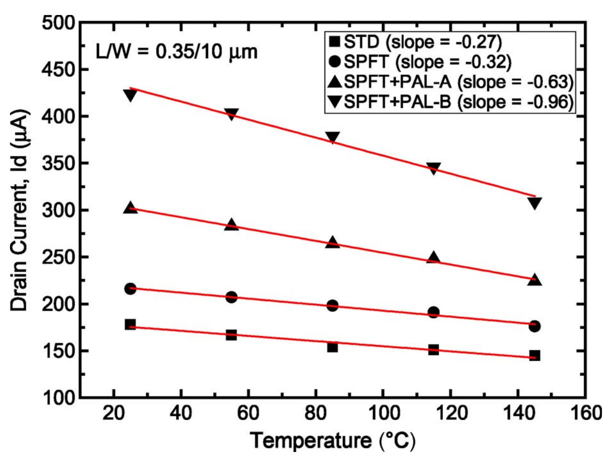

Fig. 3. nMOSFET drain current for STD, SPFT, SPFT with PAL-A, and SPFT with PAL-B under various temperatures. The slope of the fitting curve shows the degradation rate of the drain current.

and wet etching was used in the stressor removal process. After gate patterning, source/drain extension implantation, sidewall spacer, and S/D formation were carried out. A 100-nm thermal CVD tensile SiN CESL was deposited on all transistors. After interlayer-dielectric film deposition and contact patterning, a four-level metallization (Ti–TiN-Al-TiN) was carried out in the PVD system.

III. Results and Discussion

The electrical gate oxide inversion thickness is around 29.6 ± 0.2 Å for all split conditions. The performance improvement of nMOSFET in SPFT is shown in Fig. 2. Electron mobility is improved by 15% using SPFT, compared to standard devices. Moreover, a significant improvement in mobility in SPFT with PAL-A and SPFT with PAL-B is found, as shown in Fig. 3. It appears that SPFT with PAL-A and SPFT with PAL-B can further improve mobility, by 33% and 52%, respectively.

A simple model is proposed to explain the mechanism of SPFT. It has been reported that the longitudinal tensile stress and vertical compressive stress are the major components of stress in SMT processes [8], [9]. In the SPFT approach, the thermal annealing process transfers high tensile stress from the disposable stressor to the gate poly-Si, inducing a plastic strain in the poly-Si. To compensate for this external stress from the disposable stressor, a very high vertical compressive strain is induced in the poly-Si gate. The deformation of the poly-Si is thus expanded in the longitudinal direction and compressed in the vertical direction. This further creates longitudinal tensile stress and vertical compressive stress in the Si channel. After stressor removal, the high longitudinal tensile stress and vertical compressive stress will be memorized in the channel region. This mechanism explains the increased stress resulting from the use of SPFT to improve electron mobility [10]. Moreover, preamorphous poly-Si during the PAL-A and PAL-B processes offers greater compressive strain. Optimization of As implantation energy, dosage, and thermal annealing process at the gate region provides more longitudinal tensile stress and vertical compressive stress to the channel region. This result is similar to the results of previous studies in SPFT with a stacked random-poly-Si-grain gate structure [6].

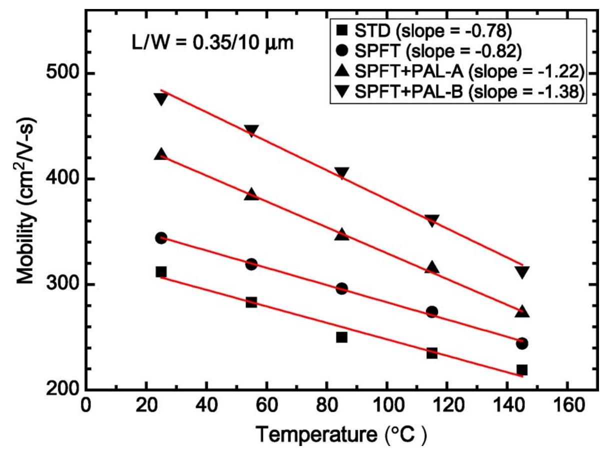

Fig. 4. nMOSFET electron mobility for STD, SPFT, SPFT with PAL-A, and SPFT with PAL-B at various temperatures. The slope of the fitting curve shows the degradation rate of electron mobility.

Fig. 3 shows the measured drain current at various temperatures. A significant improvement of drain current in SPFT and SPFTs with PAL-A and PAL-B accompanies the improvement of electron mobility. It is shown that the drain current is decreased when temperature is increased. This may be attributed to phonon scattering and reveals mobility degradation. However, the gains of drain current by SPFTs in combination with PAL-A and PAL-B are also decreased when temperature is increased. The slopes of the fitting curves on STD, SPFT, SPFT with PAL-A, and SPFT with PAL-B are -0.27, -0.32, -0.63, and -0.96, respectively. The drain current degradation rate of SPFT with PAL gate structures is more serious than that of STD devices at high temperatures. This means that the strain dependence of mobility improvement becomes weak at high temperatures, particularly on the SPFT in combination with PAL gate structures.

As shown in Fig. 4, electron mobility shows a similar trend with the drain current under various temperatures. The slopes of the STD, SPFT, SPFT with PAL-A, and SPFT with PAL-B are -0.78, -0.82, -1.22, and -1.38, respectively. Higher temperature leads to lower electron mobility gain in the SPFT with the PAL gate structure. The gate dielectric interface state

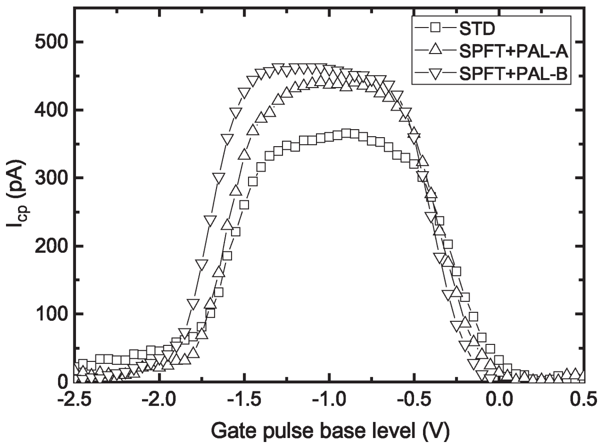

Fig. 5. Charge pumping current for STD, SPFT with PAL-A, and SPFT with PAL-B processes.

density of SPFT with PAL gate structure is checked by measuring the charge pumping current (as shown in Fig. 5). SPFT with PAL-A and SPFT with PAL-B obtained higher interface state density than the STD device. The gate dielectric interface charge and gate impurity play important roles in carrier scattering [11], [12]. Electron mobility is dominated by Coulomb scattering at room temperature and low-electric-field region [13]. Moreover, interface charge inducing Coulomb scattering is in proportion to temperature as $1/\mu_{int}(T) \propto T$[14]. Simultaneously, more ionized impurities in the gate resulting from increasing temperature will enhance remote Coulomb scattering. Therefore, we found that the gain of electron mobility in the SPFT with PAL-A and SPFT with PAL-B is decreased at high temperatures.

IV. Conclusion

We have proposed a scheme of two-step annealing processes for electron mobility improvement that uses the SPFT in combination with a PAL gate structure. The gain of mobility decreases as temperature increases, due to the gate dielectric interface charges and ionized impurities. Therefore, controlling gate impurities and improving interface quality are the keys to continued improvement in future CMOS technology.

Acknowledgment

The authors would like to thank the National Nano Device Laboratory, Hsinchu, Taiwan, for the support in device fabrications.

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