Independently-Controlled-Gate FinFET Schmitt Trigger Sub-Threshold SRAMs

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***Abstract*—In this work, we propose three novel independently-controlled-gate Schmitt Trigger (IG_ST) FinFET SRAM cells for sub-threshold operation. The proposed IG_ST 8 T SRAM cells utilize split-gate FinFET devices with the front-gate devices serving as the stacking devices, and the back-gate devices serving as the intermediate node conditioning devices to provide built-in feedback mechanism for Schmitt Trigger action, thus reducing the cell transistor count/area and achieving improved static noise margin (SNM) and better tolerance to process variation and random variations. 3-D mixed-mode simulations are used to evaluate the Read static noise margin (RSNM), Write static noise margin (WSNM), hold static noise margin (HSNM), and Standby leakage of proposed cells, and results are compared with the standard 6 T cells and previously reported 10 T Schmitt Trigger sub-threshold SRAM cells. Compared with the conventional tied-gate 6 T cell, the proposed IG_ST SRAM cells demonstrate 1.81X and 2.11X higher nominal RSNM at V_{CS} = 0.4 and 0.15 V, respectively. The cell layouts and areas are assessed based on scaled ground rules from 32 nm node, and the density advantage over previously reported 10 T Schmitt Trigger sub-threshold SRAM cells are illustrated. The cell AC performance (Read access time, Write time, and Read access time versus the number of cells per bit-line considering worst-case data pattern for bit-line leakage) and temperature dependence are evaluated, and shown to be adequate for the intended sub-threshold applications. Compared with previously reported 10 T Schmitt Trigger sub-threshold SRAM cells, the proposed cells exhibit comparable or better RSNM, higher density, and lower Standby leakage current. 3-D mixed-mode Monte Carlo simulations are performed to investigate the impacts of process variations ($L_{\rm eff}$, $\rm EOT$, $W_{\rm fin}$, *and* $H_{\rm fin}$) and random variations (Gate LER and Fin LER) on RSNM, WSNM, and HSNM. Our results indicate that even at the worst corner, two of the proposed cells can provide sufficient margin of μ/σ ratio.**

***Index Terms*—FinFET, low power SRAM, Schmitt Trigger, static noise margin, sub-threshold SRAM.**

I. Introduction

FOR ultra-low-power applications, such as portable devices, implanted medical instruments, and wireless body sensing networks, operating circuit below threshold voltage is an effective solution [1], [2] to reduce static and dynamic power consumption. However, with the scaling of technology, the stability of conventional 6 T SRAM cell [see Fig. 1(a)] deteriorates significantly, especially in sub-threshold operation [3]–[5]. Due to its superior short channel control, steeper sub-threshold swing, reduced leakage current, and immunity to random dopant fluctuation (RDF) [6], [7], FinFET-based SRAM emerges as a promising candidate for future low-voltage operation [8], [9].

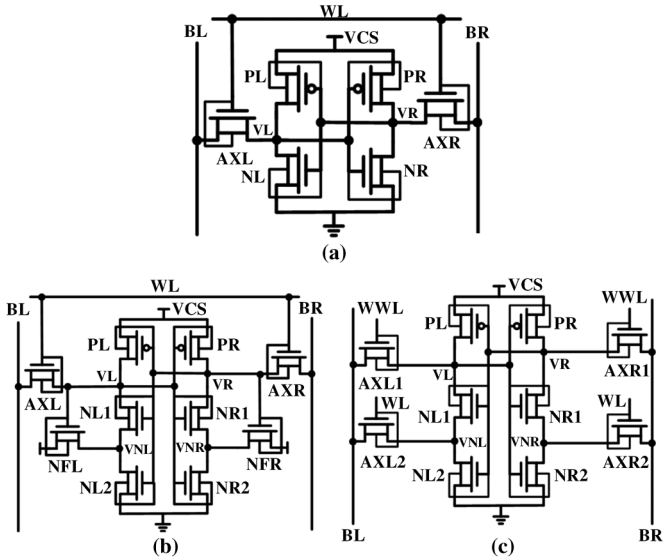

Fig. 1. Schematic of various FinFET cells: (a) conventional 6 T (6 T), (b) Schmitt Trigger 10 T (ST1) [3], and (c) Schmitt Trigger 10 T (ST2) [8].

Various sub-threshold SRAM cells in bulk CMOS have been proposed to improve cell stability [3]–[5], [10]. In particular, Schmitt Trigger-based feedback mechanism [3], [10] has been used to improve the RSNM, Write-ability, and to improve the tolerance to process variation. As shown in Fig. 1(b) [3] and (c) [10], these 10 T Schmitt Trigger sub-threshold SRAM cells (designated as ST1 and ST2, respectively) add stacking transistors (NL1 and NR1) and feedback transistors [NFL/NFR in Fig. 1(b), and AXL2/AXR2 in Fig. 1(c)] to provide the feedback mechanism for conditioning the intermediate node to raise the cell-inverter trip voltage for rising input, thus improving RSNM. These cells have been shown to operate at $V_{CS} \sim 0.15$ V. The Schmitt Trigger feedback mechanism has also been shown to improve the tolerance to process variations [3], [10]. With the capability of independent gate control in double-gate FinFET devices, we propose three novel FinFET independently-controlled-gate Schmitt Trigger (IG_ST) SRAM cells (shown as IG_ST1, IG_ST2, and IG_ST3 in Fig. 2(a)–(c),

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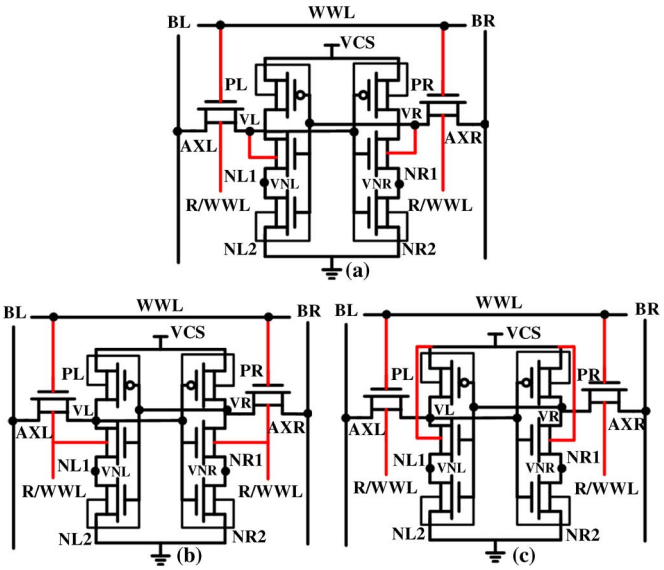

Fig. 2. Schematic of proposed Schmitt Trigger-based independently-controlled gate FinFET cells: (a) IG_ST1, (b) IG_ST2, and (c) IG_ST3.

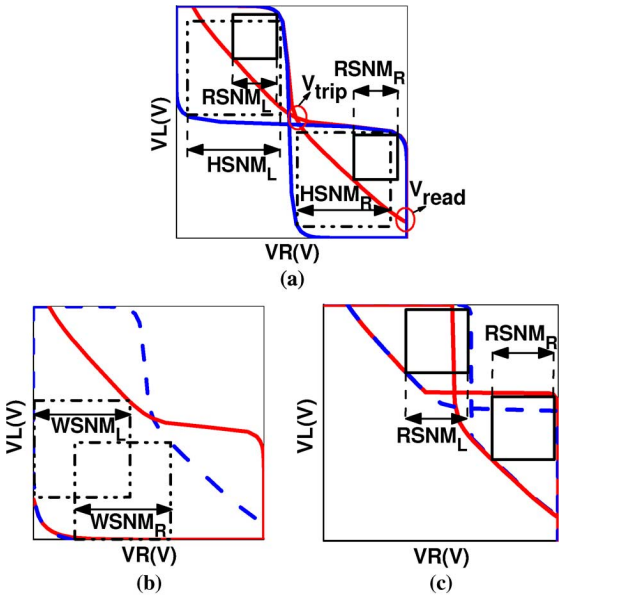

Fig. 3. Voltage transfer characteristic curves used to calculate SNM: (a) Read and Hold mode, (b) Write mode, and (c) ST1 in Read mode.

respectively). These cells utilize split-gate FinFET devices with the front-gate devices serving as the stacking devices, and the back-gate devices serving as the intermediate node conditioning devices to provide built-in feedback mechanism for Schmitt Trigger action, thus reducing the cell transistor count/area and achieving improved SNM and better tolerance to process variations and random variations. In this work, we evaluate and compare the cell stability, leakage, area, performance, and tolerance to process variations and random variations of the proposed cells with conventional 6 T SRAM cell and previously reported 10 T Schmitt Trigger SRAM cells for sub-threshold operation using TCAD 3-D mixed-mode simulations [11]. In Section II, the basic operations of the proposed Schmitt Trigger sub-threshold SRAM cells are described. Section III investigates the cell RSNM, WSNM, HSNM, and cell leakage in sub-threshold region. The cell layouts, areas, and cell AC performance (such as cell Read access time, cell Write time (Time-to-Write), Read access time versus the number of cells per bit-line considering worst-case data pattern for bit-line leakage, and temperature dependence) are assessed based on scaled ground rules from 32 nm node in Section IV. In Section V, 3-D mixed-mode Monte Carlo simulations are performed to evaluate the impacts of local random variations, notably the Gate line edge roughness (LER) and Fin LER, on FinFET SRAM stability. The combined effects with process variations ($L_{\rm eff}$, EOT, $W_{\rm fin}$, *and* $H_{\rm fin}$) are then examined for overall robustness of cell stability. Our results indicate that even at the worst corner, two of the proposed cells can provide sufficient margin of μ/σ ratio. The conclusion of this paper is given in Section VI.

II. Schmitt Trigger-Based FinFET SRAMs

In previous works [3], [10], ST1 and ST2 use Schmitt Trigger characteristics to enhance RSNM in low voltage operation. For ST1 [see Fig. 1(b)], the feedback mechanism from NFR (NFL) that conditions the intermediate stacking node VNR (VNL) is adaptively enabled according to the direction of input transition (1 to 0, or 0 to 1). During Read operation (assume $\rm VL = 0$ $\rm VR = V_{CS}$), the voltage of VL would rise to $V_{\rm read}$ [see Fig. 3(a)] due to the voltage divider effect between AXL and pull-down transistors (NL1-NL2). If $V_{\rm read}$ is higher than the switching threshold $V_{\rm trip}$ [see Fig. 3(a)] of the opposite cell inverter (PR-NR1-NR2), the data in cell storage nodes would be flipped, thus causing Read failure. With the Schmitt Trigger feedback mechanism, the $V_{\rm trip}$ of the inverter (PR-NR1-NR2) is increased due to: 1) higher VNR node voltage, which is conditioned to one diode drop below $\rm VR(= V_{CS})$ by the feedback transistor NFR and 2) higher V_T of NR1 owing to its reverse body-to-source bias (for bulk device). As such, the RSNM improves and the stored data in VL and VR is preserved. The detailed voltage transfer characteristics (VTC) is shown in Fig. 3(c), where the improved RSNM due to higher $V_{\rm trip}$ can be seen. During Write operation (again assume $\rm VL = 0$ $\rm VR = V_{CS}$), the feedback transistor NFL turns off. Due to series combination of pull-down transistors NL1 and NL2, the $V_{\rm trip}$ of the inverter (PL-NL1-NL2) is raised to higher voltage with identical mechanism of writing "1" to "0", resulting in better Write margin and Write-ability. The ST2 cell uses AXR2 (AXL2) to adaptively control cell inverter switching threshold. The gates of the feedback transistors AXR2 (AXL2) are connected to word-line to provide a firmer/stronger intermediate node conditioning action than that in ST1 where the gates of NFL (NFR) are connected to cell storage nodes. Moreover, during Write operation, AXR2 (AXL2) provides extra path to discharge the cell internal nodes to improve the Write margin and performance. Therefore, both RSNM and Write-ability are further enhanced compared with ST1.

Due to the flexibility of independently-controlled-gate (IG) operation in FinFET structure, the role of the Schmitt Trigger feedback transistor could be realized from the existing transistor NR1 (NL1). By splitting the front- and back-gate of NR1

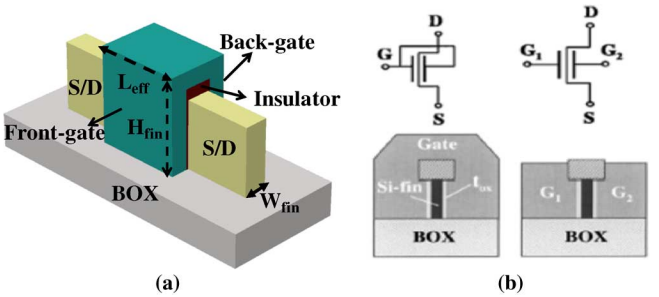

Fig. 4. (a) FinFET device structure and (b) tied-gate and IG configurations [12].

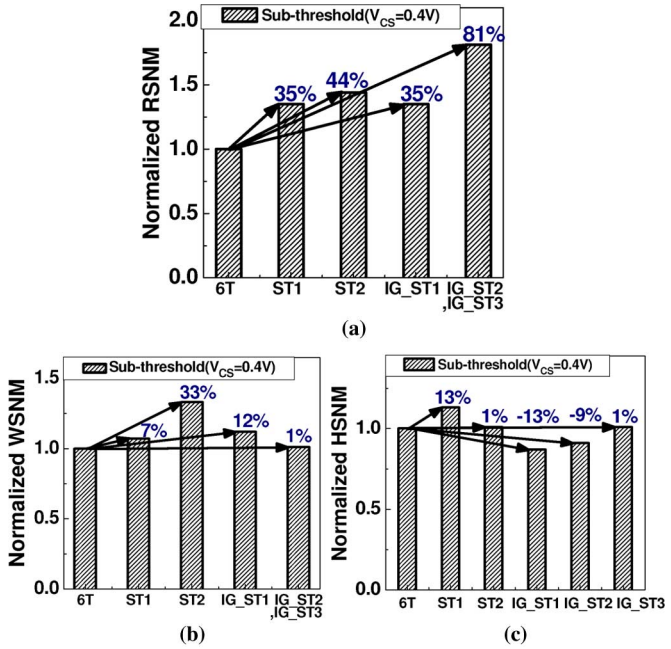

Fig. 5. Comparison of normalized nominal (a) RSNM, (b) WSNM, and (c) HSNM for different cells.

(NL1), one can use the front-gate as the stacking device, and the back-gate as the intermediate node conditioning device to provide built-in feedback mechanism for Schmitt Trigger action, thus reducing the cell transistor count/area. Three novel SRAM cell structures are proposed in this work. IG_ST1 [see Fig. 2(a)] forms Schmitt Trigger feedback path by connecting the back-gate of NR1 (NL1) to cell storage node VR (VL). During Read operation (assume $\mathrm{VL} = 0\ \mathrm{VR} = V_{CS}$), the feedback mechanism is enabled with the node voltage VNR conditioned to one diode drop below VR by the back-gate of NR1, thus increasing V_{trip} of the cell inverter (PR-NR1-NR2) and improving the RSNM. Notice that as VL rises and VR falls, the feedback (intermediate node conditioning) mechanism becomes weaker and the switching slope (steepness) of IG_ST1 cell would degrade. Notice also that split-gate configuration is used for the access pass-transistor AXL (AXR), so only one gate is enabled during Read to reduce Read disturb, while both gates are enabled during Write to improve Write-ability and performance. During Write operation (assume $\mathrm{VL} = 0\ \mathrm{VR} = V_{CS}$), due to reduced NL1 strength with its back-gate connected to $\mathrm{VL}(= 0)$, and the series NL1-NL2 pull-down configuration, the trip voltage of the left cell inverter (PL-NL1-NL2) is raised, thus further improving the Write-ability.

In IG_ST2 [see Fig. 2(b)], the back-gates of NR1 (NL1) and AXR (AXL) are connected to the R/WWL. The connection of the back-gates of NR1 (NL1) to R/WWL provides a firmer/stronger intermediate node conditioning action, and a steeper switching transition (since the back-gate of NR1 is always "High" during Read) than IG_ST1. Furthermore, during Write operation $(\mathrm{VL} = 0\ \mathrm{VR} = V_{CS})$, due to stronger NL1 with its back-gate always at "High", its Write-ability is slightly degraded with respect to IG_ST1 cell.

In IG_ST3 cell [see Fig. 2(c)], the back-gates of NR1 (NL1) are connected to V_{CS}. Therefore, the cell would preserve the Schmitt Trigger feedback mechanism even when the R/WWL and WWL are turned off (i.e., Hold mode). In Read and Write mode, IG_ST3 cell has the same Schmitt Trigger feedback mechanism as IG_ST2 cell. Hence, IG_ST3 would have better HSNM, and the same RSNM and WSNM with IG_ST2 cell.

Fig. 4(a) shows the FinFET device structure studied in this paper and Fig. 4(b) shows the tied-gate and independently-controlled-gate configurations [12]. Our analyses are based on FinFET device with $\mathrm{Na} = 1 \times 10^{17}\ \mathrm{cm}^{-3}$, $L_{\mathrm{eff}} = 25$ nm, $W_{\mathrm{fin}} = 7$ nm, $H_{\mathrm{fin}} = 20$ nm, and $\mathrm{EOT} = 0.65$ nm, consistent with the ITRS Roadmap projection. The threshold voltage of the devices are $V_{TN} \sim 0.45$ V and $V_{TP} \sim 0.45$ V.

III. SNM and Standby Leakage of Sub-Threshold FinFET SRAM Cells

The RSNM is defined as the length of maximum square that can fit inside the butterfly curves in Read mode [13], and the minimum of $\mathrm{RSNM_L}$ and $\mathrm{RSNM_R}$ is chosen as the cell RSNM [see Fig. 3(a)]. The HSNM is defined similar to RSNM with the cell in Standby (Hold) mode. The WSNM is defined as the minimum square spanning between the curves in Write mode [see Fig. 3(b)], and the smaller of $\mathrm{WSNM_L}$ and $\mathrm{WSNM_R}$ is chosen as the cell WSNM. Due to the asymmetrical voltage transfer curves (VTC) for ST1 cell, the corresponding RSNM is as shown in Fig. 3(c).

In Fig. 5(a), the normalized nominal RSNM of different cells are compared in sub-threshold region $(V_{CS} = 0.4\ \mathrm{V})$. With the help of feedback mechanism, Schmitt Trigger-based cells show significantly better nominal RSNM (35%–81%) than the conventional 6 T cell. In particular, IG_ST2 and IG_ST3 have the most significant improvement in nominal RSNM ($\sim$81%) due to their steeper switching characteristics and reduced V_{read}. In Write mode [see Fig. 5(b)], Schmitt Trigger-based cells also show better nominal WSNM (1% to 33%). The improvement is most significant for ST2 cell due to its two parallel discharging paths for cell internal nodes and tied-gate pass-transistor configuration. In Hold mode [see Fig. 5(c)], IG_ST1 and IG_ST2 have slightly lower nominal HSNM due to the split-gate configuration of NL1 (NR1) which slightly degrades the switching slope (steepness). Notice that IG_ST1 maintains the feedback mechanism even in Hold mode, as the intermediate node VNL (or VNR) is still conditioned by the back-gate of NL1 (or NR1) to one diode drop below the "High" cell storage node. Also

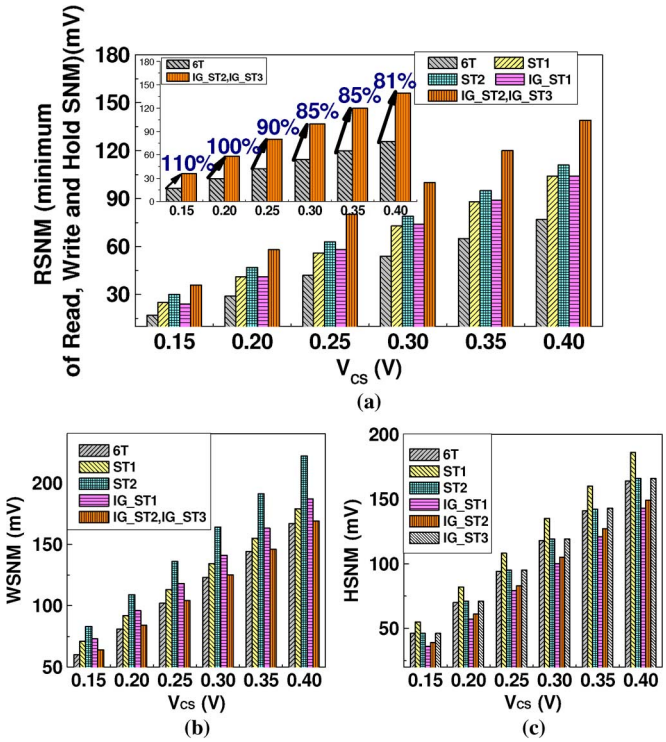

Fig. 6. Comparison of nominal (a) RSNM, (b) WSNM, and (c) HSNM in ultra-low voltage operation.

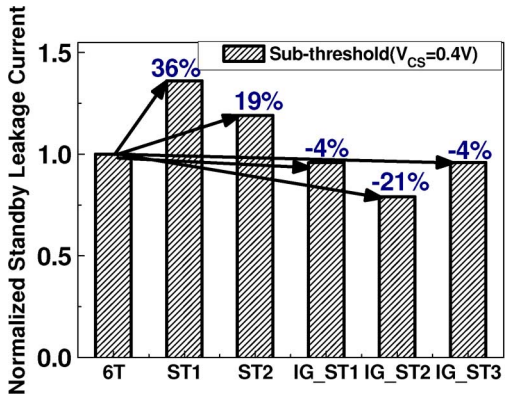

Fig. 7. Comparison of cell Standby leakage current (at $V_{CS} = 0.4$ V) of various cells.

TABLE I
LAYOUT DESIGN RULES

L_{eff}=25nm node	scale
x=contacted gate pitch	100nm
y=fin pitch	100nm
z=contact to contact pitch	80nm
M1 pitch	80nm
M2 pitch	80nm

the V_T of the front-gate of NL1 (or NR1) will be lower due to gate-to-gate coupling. The switching transition also tends to be soft as the feedback mechanism weakens and eventual diminishes with the switching transition.

For IG_ST2 in Hold mode, the back-gates of NL1 (and NR1) are at "Low", hence there is no feedback mechanism. The V_T of the front-gates of NL1 and NR1 will be a little bit higher due to gate-to-gate coupling, thus $V_{\rm trip}$ tends to be a little higher. The HSNM, however, does not constitute a limitation on SRAM stability, while RSNM does [13]. IG_ST3 exhibits HSNM comparable to (1% better) 6 T cell since it preserves the Schmitt Trigger feedback mechanism in Hold mode. The stability of the cells operating at ultra-low voltages is assessed in Fig. 6. It can be seen that RSNM is most critical for the supply voltage range from 0.4 V down to 0.15 V. Furthermore, the improvements of RSNM of the proposed cells over 6 T cell become more significant as the supply voltage decreases [shown in Fig. 6(a) inset]. For IG_ST2 and IG_ST3 cell, the improvement increases from 81% to 110% as V_{CS} scales from 0.4 to 0.15 V.

Notice that during Write operation, both R/WWL and WWL are turned on, so both the front- and back-gate of the access pass-transistor AXL (AXR) are enabled. As such, the half-select disturb along the selected WL is more serious than the half-select disturb during Read operation. Notice also that other sub-threshold SRAM cells, like those in [4] and [5], and previously reported 10 T Schmitt Trigger sub-threshold SRAM cells [3], [10] have similar Write half-select disturb constraint. Therefore, non-bit-interleaving architecture or Byte Writing architecture should be used to best exploit the improved RSNM of these sub-threshold SRAM cells.

Fig. 7 compares the Standby leakage current of different cells. The conditions of cell storage nodes are VR = "Low" and VL = "High". Compared with 6 T cell, ST1 and ST2 have extra leakage path through NFR and AXR2, and therefore exhibit 36% and 19% higher Standby leakage current, respectively. Without extra cell leakage path, IG_ST1 and IG_ST3 show slightly lower leakage (4%) compared with 6 T cell. Moreover, IG_ST2 cell, with the back-gate of the stacking transistor (NL1/NR1) off in Standby, reduces up to 21% cell leakage current compared with 6 T cell.

IV. Cell Area and Read/Write Performance of Sub-Threshold FinFET SRAMs

A. Cell Area

Based on published design rules of 32-nm technologies [14]–[16] and scaling factor from ITRS Roadmap, the cell area of various FinFET SRAM cells are estimated and compared. Table I summarizes the pertinent layout design rules used in this work. In Fig. 8(a), we illustrate the layouts of different cells and estimate the corresponding area overhead. We establish a standard 6 T thin-cell layout [17] which requires 4.5 fin pitch in horizontal dimension and 2 contacted gate pitch in vertical dimension, and the area is 0.09 μm^2. For ST1 and ST2 cells, extra feedback [NFL (NFR) and AXL2 (AXR2)] and stacking [NL1 (NR1)] transistors result in increase of 69% and 50% in horizontal and vertical dimension, respectively. Furthermore, extra Metal-2 track is required to connect the internal nodes. In contrast, our proposed cells could reduce the areas occupied by the two feedback transistors (horizontal dimension) and the contacts at NL2 (NR2) drain side (vertical dimension). As shown in Fig. 8(b), the proposed cells (IG_ST1, IG_ST2, and

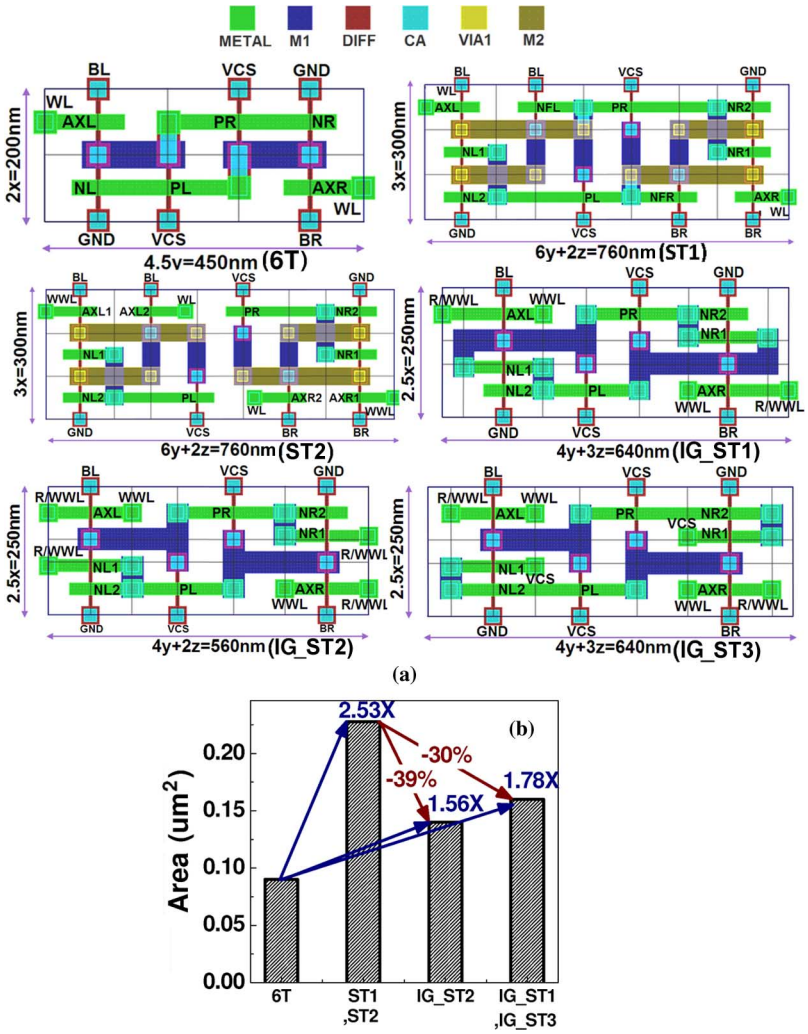

Fig. 8. (a) Various FinFET cell layouts and (b) comparison of cell areas of various FinFET cells.

IG_ST3) can save 30%–39% area compared with ST1 and ST2 cells.

In the following sections, the cell Read access time and Write time (Time-to-Write) are assessed by 3-D TCAD mixed-mode transient simulations. The length of bit-line is 128 cells. A capacitive load is added onto each bit-line to account for the capacitance of wires and connected devices. The bit-line wire length and capacitance for various cells are calculated from the heights of cell layouts described in Section A.

B. Cell Read Access Time

Fig. 9(a) shows the definition of "cell" Read access time, which is measured as the time required for developing 50 mV bit-line differential voltage after the word-line turns on. The "cell" Read access time strongly depends on the Read current through the access and pull-down transistors. In Fig. 9(b), we compare "cell" Read access time of various FinFET SRAM cells for operating voltages (V_{CS}) ranging from 0.40 V down to 0.20 V. For IG_ST1, IG_ST2, and IG_ST3 cells, the reduced strength of access transistor (with only one-gate on during Read) benefits the RSNM, but severely degrades the cell Read access time as compared with 6 T cell in tied-gate configuration (93X

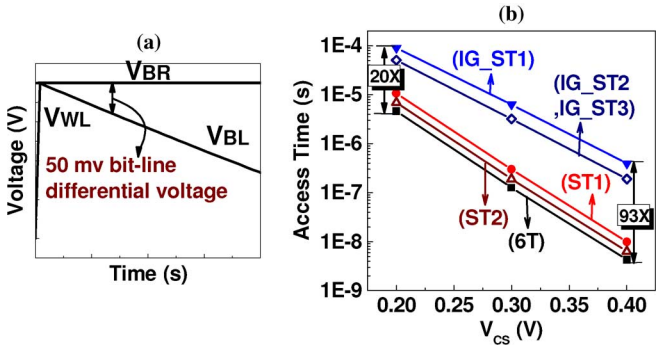

Fig. 9. (a) Definition of "cell" Read access time and (b) comparison of "cell" Read access time for different FinFET cells operating at various V_{CS} (128 cells per bit-line).

slower). However, with the scaling of V_{CS} to 0.2 V, the difference decreases to 20X. This is because the current driving capability of the access transistor depends exponentially on the gate voltage (V_{CS}) in sub-threshold region and the effect of device sizing (device width of single-gate mode versus tied-gate mode) becomes less significant at lower voltage. Notice that

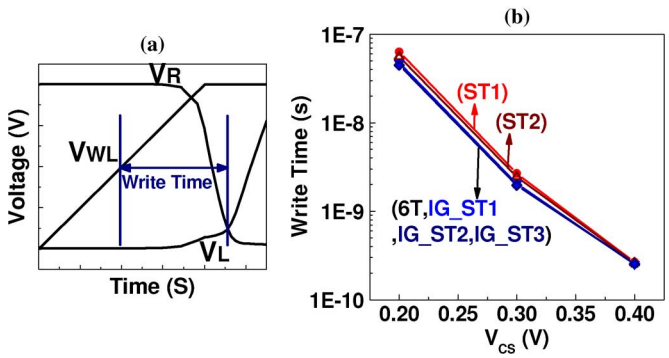

Fig. 10. (a) Definition of "cell" Write time (Time-to-Write) and (b) comparison of "cell" Write time of different FinFET cells operating at various V_{CS} (128 cells per bit-line).

sub-threshold SRAMs typically aim for applications such as implantable devices, medical instruments, and wireless sensor networks with operating frequency ranging from several hundred Hz to several hundred kHz, and power dissipation from μW to tens of μWs. Thus, the Read access times for the proposed cells appear adequate for the intended application.

C. Cell Write Time (Time-to-Write)

For Write operation, the "cell" Write time is defined as the time it takes for the voltages of two cell storage nodes to cross over after the word-line turns on [see Fig. 10(a)]. Fig. 10(b) compares the Write time of different cells operating at various V_{CS}. As can be seen, the Write time of these cells are comparable due to the similar configuration of access and pull-up transistors during Write. The Write times of cell ST1 and ST2 are slightly larger than other cells at $V_{CS} = 0.2$ V due to their increased node capacitances. Also notice that compared with cell Read access time, the cell Write time is significantly shorter.

D. Read Access Time With Worst-Case Bit-Line Leakage Current

In this section, the impact of bit-line leakage, due to the Standby leakage currents from unselected cells on the selected bit-line pair, on "cell" Read access time is investigated. Fig. 11(a) illustrates the worst-case data pattern for bit-line leakage. All unselected cells have the same data which is opposite to the selected cell. The solid arrow line symbolizes the Read current in the selected cell, while the dashed arrow lines represent the leakage currents from the unselected cells which rival the Read current. The leakage currents would charge up the low-going bit-line while discharge the bit-line which is supposed to be held at "High". Thus, the bit-line differential voltage is reduced, resulting in degradation of sensing margin and speed. Fig. 11(b) shows the dependence of "cell" Read access time on the number of cells per bit-line. Due to the better gate control and lower leakage current of FinFET devices, increasing the number of cells per bit-line from 32 to 256 degrades the cell Read access time by about 5–6X. Thus, the proposed cells can support adequate number of cells per bit-line to meet the density requirement with adequate performance (several hundred Hz to several hundred kHz) for the intended applications.

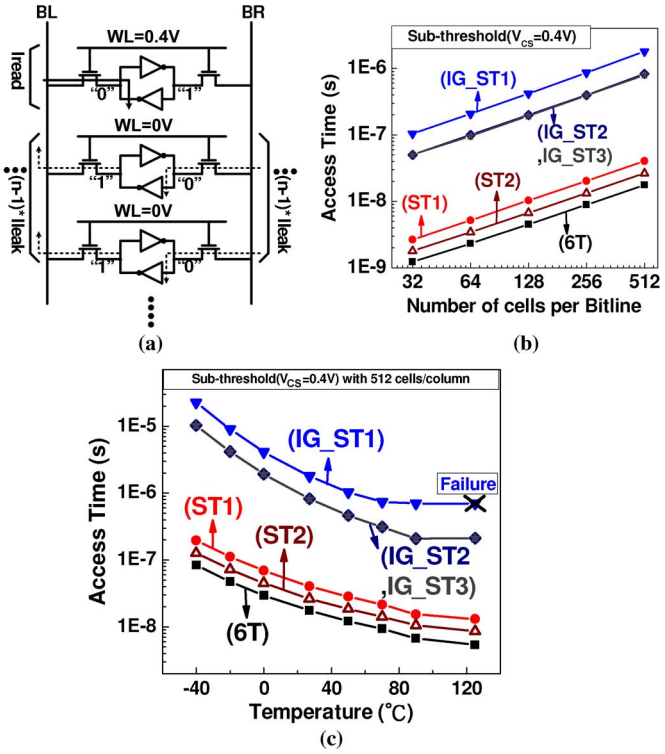

Fig. 11. (a) Schematics showing the worst-case bit-line data pattern for leakage current affecting Read operation. (b) Read access time considering worst-case bit-line leakage current versus number of cells per bit-line. (c) Read access time of 512 cells per bit-line (worst-case bit-line data pattern) versus temperature.

It is important to point out that the temperature significantly affects transistor leakage current (two orders difference from 27 °C to 125 °C) [18]. Fig. 11(c) shows the Read access time of 512 cells per bit-line for the worst-case bit-line data pattern versus temperature. It can be seen that except for IG_ST1 cell at 125 °C, other cells can successfully perform Read operation across the temperature range. The failure of IG_ST1 cell is mainly due to its slower sense signal development (longer Read access time), rendering it more susceptible to bit-line leakage.

V. Analysis of Process/Random Variation for FinFET Sub-Threshold SRAM Cells

As described in [3] and [10], the feedback mechanism also provides built-in process tolerance. This is because the feedback NFET would track the process variation and adjust the feedback for conditioning the intermediate node accordingly. Using ST1 as an example, at Fast-N (FN) corner, the V_T of the feedback NFET (NFL/NFR) would be lower, resulting in higher intermediate node (VNL or VNR) voltage, thus partially compensating for the lower V_T of the cell pull-down NFET transistor stacks. In this section, we describe results from 3-D mixed-mode Monte Carlo simulations considering the impacts of process variations and local random variations on cell stability.

Among various local random variation sources, line edge roughness (LER) has been shown to be the most important one for FinFET device [19], [20]. It consists of variations from the deviations of gate length (Gate LER) and fin width (Fin LER). For LER analysis, a RMS amplitude $\Delta = 1.5$ nm and correlation length $\Lambda = 20$ nm [19], [20] are assumed. Fig. 12

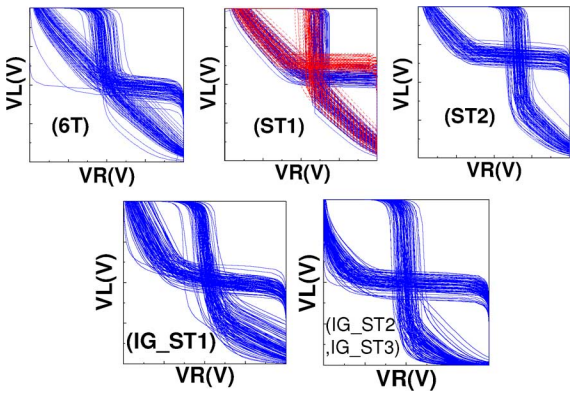

Fig. 12. Voltage transfer characteristics of various cells considering Fin LER from 3-D mixed-mode Monte Carlo simulations.

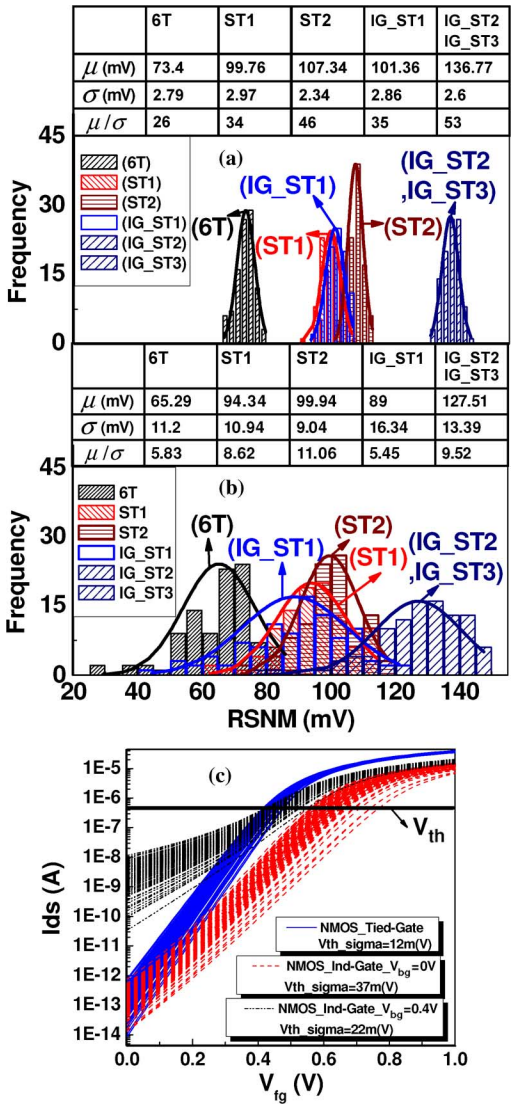

Fig. 13. Probability distribution of RSNM (at $V_{CS} = 0.4$ V) considering (a) Gate LER and (b) Fin LER for different SRAM cell structures from 3-D mixed-mode Monte Carlo simulations. (c) $I_d - V_g$ curves of independent-gate and tied-gate mode considering Fin LER from 3-D Monte Carlo simulations (150 samples).

illustrates the butterfly curves (at $V_{CS} = 0.4$ V) induced by Fin LER of different cells. 3-D TCAD mixed-mode Monte Carlo

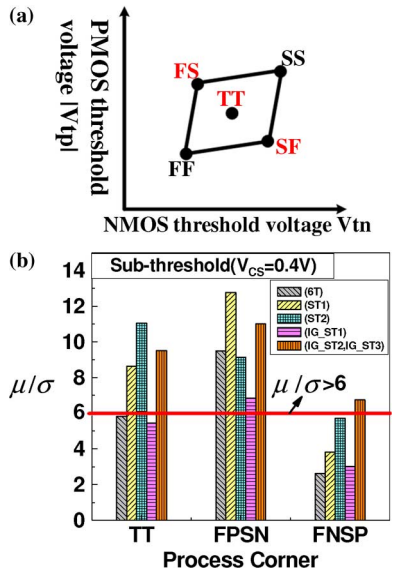

Fig. 14. (a) Definition of various process corners. (b) Comparison of μ/σ for RSNM of various cells at different process corners combined with local random variation (Fin LER).

simulations with 100 samples for each case are analyzed [19], [21]. Fig. 13 compares the probability distribution of the RSNM (at $V_{CS} = 0.4$ V) of different cell structures induced by Gate LER [see Fig. 13(a)] and Fin LER [see Fig. 13(b)], respectively. As can be seen, Fin LER represents the dominating source of RSNM variation. For Gate LER, the μ/σ ratios of all Schmitt Trigger-based cells are well over 30. For Fin LER, the μ/σ ratio can be seen to be much smaller than that for Gate LER. Notice that a μ/σ ratio of at least around 5–6 is desirable. We can see that except for IG_ST1 cell (μ/σ ratio $= 5.45$), other Schmitt Trigger-based cells can provide significantly better margin than that of 6 T (μ/σ ratio $= 5.83$). This is because IG_ST1 cell operating in independent-gate mode has worse electrostatic integrity than the tied-gate mode [22], and its nominal RSNM improvement (over 6 T cell) is less significant than IG_ST2 and IG_ST3 cells due to its softer (less steep) switching characteristics as discussed in Section II. Fig. 13(c) shows the $I_d - V_g$ dispersion curves considering Fin LER from 3-D TCAD Monte Carlo simulations with 150 samples. It clearly shows that independent-gate mode has larger σVth than tied-gate mode. The results are consistent with the larger σRSNM observed in the proposed cells using independent-gate technique.

In order to evaluate the robustness of these FinFET SRAM cells under process variations, several process corners are defined in Fig. 14(a). In this work, $\pm 20\%$ device parameter deviations are assumed and two most critical device parameters (L_{eff} and W_{fin}) are used to characterize fast and slow devices. Three corners (TT, FNSP, and FPSN) combined with local random Fin LER are considered in these cells and compared in Fig. 14(b). It can be seen that FNSP corner exhibits relatively smaller μ/σ ratio than other corners, and most cells fail to satisfy the requirement of $\mu/\sigma > 6$ at this corner. Notice that IG_ST2 and IG_ST3 can still provide sufficient margin (μ/σ ratio $= 7$) and show the best robustness for RSNM under the combined influence of process and local random variations.

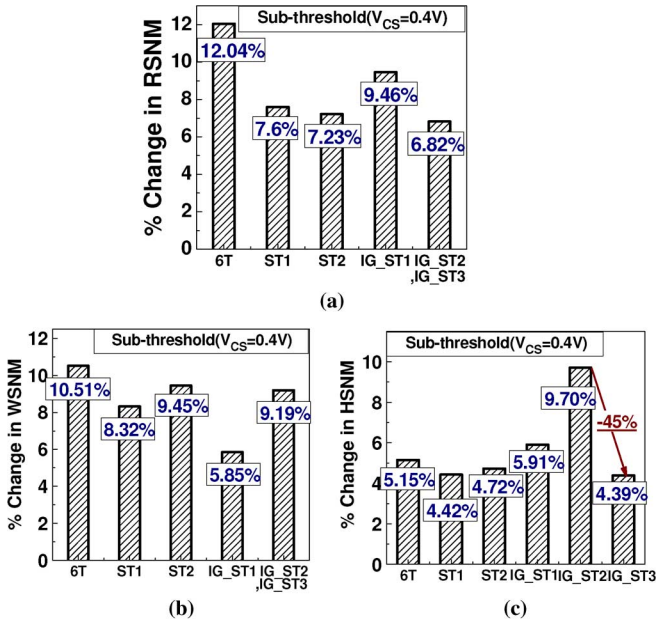

Fig. 15. (a) RSNM, (b) WSNM, and (c) HSNM sensitivity to process parameter variations such as $L_{\rm eff}$, $W_{\rm fin}$, EOT and $H_{\rm fin}$ variation (-20% to 20%).

TABLE II
COMPARISONS OF OUR PROPOSED CELLS WITH CONVENTIONAL 6 T AND 10 T SCHMITT TRIGGER-BASED SRAM CELLS

	6T	ST1	ST2	IG_ST1	IG_ST2	IG_ST3
Stability (mV)						
Read	77	104	111	104	139	139
Write	167	179	222	187	169	169
Hold	164	186	166	143	149	166
Normalized STBY Leakage Current	1	1.36	1.19	0.96	0.79	0.96
Read Time (ns)	4.26	9.92	6.3	396	190	190
Write Time (ps)	255	266	262	253	254	254
Variation (μ/σ @ FNSP)	2.62	3.82	5.72	3.02	6.75	6.75
Normalized Area	1	2.53	2.53	1.56	1.78	1.78

In addition to RSNM variations described above, the sensitivity of cell stability (ΔSNM) to device parameters are also assessed. ΔSNM is calculated from the SNM difference by taking $\pm 20\%$ device parameter deviations, including $L_{\rm eff}$, $W_{\rm fin}$, EOT, and $H_{\rm fin}$, i.e., $\Delta\mathrm{SNM} = |\mathrm{SNM}(P+20\%) - \mathrm{SNM}(P-20\%)|$. The % change in SNM is defined as $\Delta\mathrm{SNM}/\mathrm{SNM}_{\rm nominal}$. Fig. 15 compares the % change in SNM of various cells during Read, Write, and Hold operations. In Fig. 15(a), IG_ST2 and IG_ST3 cells are found to exhibit least sensitivity (smallest % change in RSNM) to device parameter variations. In Fig. 15(b), Schmitt Trigger-based cells show slightly better (lower) WSNM sensitivity. In Fig. 15(c), IG_ST2 shows the worst % change in HSNM since there is no feedback mechanism during Hold operation. Among our proposed cells, IG_ST3 cell, with the strongest feedback mechanism, demonstrates better HSNM than that in IG_ST1 and IG_ST2 cells. Table II summarizes and compares several important metrics among conventional 6 T and Schmitt Trigger based SRAM cells. It can be seen that our proposed Schmitt Trigger-based independently-controlled-gate FinFET SRAM cells exhibit superior cell stability even under the influence of device variations at different process corners. Moreover, the Standby leakage current of the proposed cells is lower than other reference cells to meet the requirement of ultra-low power applications.

VI. CONCLUSION

We proposed three novel Schmitt Trigger-based independently-controlled-gate FinFET SRAM cells for sub-threshold operation, and comprehensively analyzed and compared the proposed cells with conventional 6 T and previously reported 10 T Schmitt Trigger sub-threshold SRAM cells. Our results showed significant nominal RSNM improvements in IG_ST2 and IG_ST3 cells (81% over 6 T cell at $V_{CS} = 0.40$ V) without degrading nominal WSNM and HSNM. At ultra-low-voltage ($V_{CS} = 0.15$ V), the nominal RSNM improvement could reach 110%. The areas of the proposed cells were shown to be 30%–39% smaller (and cell Standby leakage from 20% to over 50% lower) than previously reported 10 T Schmitt Trigger sub-threshold SRAM cells. The cell AC performance (Read access time, Write time) was assessed using TCAD 3-D mixed-mode simulations. The proposed cells were shown to support sufficient number of cells per bit-line and offer adequate performance for the intended sub-threshold applications under worst-case bit-line data pattern for leakage current. 3-D mixed-mode Monte Carlo simulations were carried out to investigate the impacts of process variations and random (LER) variations on the cell stability. IG_ST2 and IG_ST3 cells were shown to exhibit sufficient margin (μ/σ ratio $= 7$) even at the worst corner (FNSP). With enhanced cell stability, reduced cell area and Standby leakage, adequate performance, and robust tolerance to process variations and random variations, the proposed IG_ST2 and IG_ST3 cells are promising candidates for future ultra-low-voltage sub-threshold applications.

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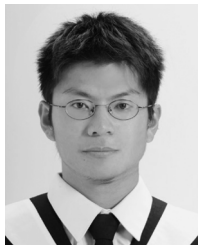

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also been very active and visible in leakage/variation/degradation tolerant circuit and SRAM design techniques. He took early retirement from IBM to join National Chiao-Tung University, Hsinchu, Taiwan, as a Chair Professor in the Department of Electronics Engineering in February 2008. He has authored many invited papers in international journals such as the *International Journal of High Speed Electronics*, the PROCEEDINGS OF IEEE, the *IEEE Circuits and Devices Magazine*, and the *Microelectronics Journal*. He holds 38 U.S. patents with another 14 pending. He has authored or coauthored over 300 papers.

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