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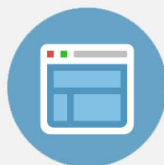
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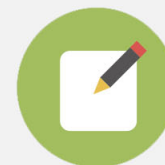


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A study of phase transition behaviors of chalcogenide layers using *in situ* alternative-current impedance spectroscopy

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Electrical properties of chalcogenide thin films, both pristine $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST) and cerium-doped GST, were investigated by *in situ* alternative-current (AC) impedance spectroscopy. With the aid of brick-layer model and nano-grain composite model, the roles of grain and grain-boundary on the phase transition of chalcogenides were distinguished and the dominance of grain boundary was observed. Tangent loss behaviors deduced by impedance analysis revealed alien-element doping alters the interfacial polarization and delays the phase-transition rate of GST. Analytical results also illustrated that the *in situ* AC impedance spectroscopy can be an alternative tool for characterizing the phase-change kinetics of chalcogenides thin films with nano-scale grain sizes. © 2012 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4729528>]

I. INTRODUCTION

Recently, phase-change random access memory (PRAM) has attracted considerable research interests both in the views of scientific and technological developments.¹ PRAM utilizes chalcogenides as the programming layers and their unique amorphous-to-crystalline phase transition behaviors have been widely studied in the field of optical memory devices.^{2–5} The advantages of chalcogenides applied to PRAM include low power consumption, high operational speed, high data storage density, excellent scalability to nano-scale cell sizes, and good process compatibility to complementary metal-oxide-semiconductor (CMOS) technology.⁶ However, insufficiency in material properties of chalcogenides constrains the electrical performance of PRAM as the device size continuously shrinks. To overcome this difficulty, the chalcogenides with new chemical constitutions and alien-element doping methods have been developed for physical property modifications.^{7–9} At present, the doping elements such as nitrogen (N),^{10–12} silicon oxide (SiO_x),^{13,14} oxygen (O),^{15,16} silicon (Si),^{17,18} bismuth (Bi),^{19–21} tin (Sn),²¹ silver (Ag),²² molybdenum (Mo),²³ and cerium (Ce)²⁴ have been reported and their effects on the phase-change kinetics of chalcogenides have been studied. Conventionally, the analyses were carried out by measuring the change of resistance (R) of samples against the temperature either in exothermal or isothermal manner. The key phase-transition parameters, e.g., the recrystallization temperatures (T_x) and activation energy (E_a), were then calibrated so as to explore the doping effects on phase-transition behaviors of chalcogenides.

Impedance spectroscopy is a versatile tool for characterizing the electrical properties of materials, in particular, the influences of interfaces on the electrical properties of samples.²⁵ For instance, it has been applied to determine the effects of grain boundaries on the polarization phenomena of

ceramic materials.^{26,27} In doped samples, the dopants may present as the solute atoms in the grains, segregate toward the grain boundaries, or form the intermetallic compounds when beyond the solubility limit. This alters the carrier transports both in grains and grain boundaries of sample and, with the aid of equivalent circuit models, their effects on conduction behaviors can be analyzed via the impedance measurement at various frequencies.^{28–30}

Impedance spectroscopy has been applied to study the chalcogenides, for instance, M-Sánchez *et al.* determined the T_x of GST annealed at different temperatures³¹ while Qamhieh *et al.* found the resistance property and relaxation frequency of GST possess the same temperature dependence.³² In oxygen-doped GST samples, impedance analysis revealed the dopant indeed affects the phase-transition behaviors of GST³³ and alters the contribution of grain and grain-boundary to the electrical properties of doped GST.³⁴

This work establishes an *in situ* alternative-current (AC) impedance measurement for analyzing the phase-transition behaviors of pristine $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST) and cerium-doped GST (Ce-GST) in conjunction with the equivalent circuit models, e.g., the brick-layer model (BLM)^{35–37} and the nano-grain composite model (n-GCM).³⁸ In addition to distinguishing the roles of grain and grain-boundary to electrical properties, the feasibility of impedance spectroscopy to characterize the phase-change kinetics of chalcogenides is also discussed.

II. EXPERIMENT

The 150-nm thick pristine GST and Ce-GST layers were separately deposited on the thermally oxidized Si wafer substrates in a sputtering system with background pressure better than 2×10^{-6} Torr. The thin-film deposition was accomplished at the radio-frequency (RF) sputtering power = 55 W and the working pressure = 3 mTorr with argon (Ar) as the inlet flow gas. The Ce doping was achieved by the target-attachment sputtering method reported elsewhere.²⁴ The amount of Ce added in GST was adjusted by adjusting the number of Ce pellets attached on the GST

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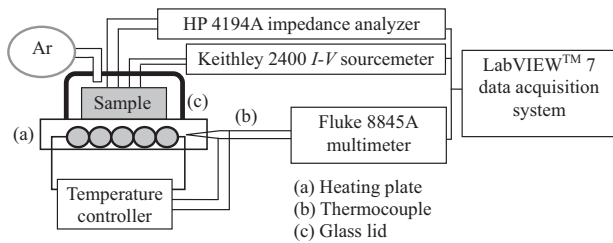


FIG. 1. Schematic illustration of the setup of *in situ* electrical measurement system.

target and, in this work, the Ce-GST sample contained about 2.35 at. % Ce.

The electrical properties of chalcogenide samples as a function of temperature were acquired in an *in situ* manner by an electrical measurement system equipped with the LABVIEW™ 7 data acquisition software schematically illustrated in Fig. 1. The samples were placed in a heating chamber with Ar as the protecting gas and heated to desired temperature at a rate of 1 °C/min. The R values of samples were measured by two-point probe method and acquired by the data acquisition system in every 15 s. The impedance data were measured at temperatures of 100, 150, 175, 200, 225, 250, 275, 300, 325, and 350 °C in the frequency range of 40 Hz to 10 MHz at a constant voltage of 0.5 V. At each test temperature, the impedance data scan in such a frequency range took about 30 s. The contributions of the grain and the grain boundary to electrical properties of chalcogenide samples were then differentiated by fitting the impedance data in terms of above-mentioned equivalent circuit models utilizing the ZVIEW software.³⁹ The electrical property data included the values of R and capacitance (C), e.g., R_g and C_g for the grain and R_{gb} and C_{gb} for the grain boundary. X-ray diffraction (XRD) measurements were performed in a Bruker Instruments D8 DISCOVER system within the Cu- K_α radiation at wavelength of 0.15406 nm, scan rate of 0.04°/s, and a fixed x-ray grazing incidence angle of 2°.

III. RESULTS AND DISCUSSION

A. Microstructures

Figures 2(a) and 2(b) separately present the XRD profiles of pristine GST and Ce-GST samples subjected to 1 h annealing at various temperatures of 200, 250, 300, and 350 °C. It can be seen that the GST possesses the face-centered cubic

(FCC) structure at temperatures below 300 °C and transforms to hexagonal structure when the sample is heated to 350 °C. As shown in Fig. 2(b), amorphous-to-FCC phase transition similarly occurs in Ce-GST. However, Ce-GST remains in FCC structure at all test temperatures, implying that the Ce doping may stabilize the GST in the FCC status.

A calibration of full-width-half-maximum (FWHM) of the characteristic XRD peaks shown in Fig. 2 found that the FWHM decreases with the increase of annealing temperature for both GST and Ce-GST. Moreover, the FWHM of Ce-GST is larger than that of pristine GST at the same temperature, e.g., $\text{FWHM}_{(200)} = 2.04^\circ$ for Ce-GST while $\text{FWHM}_{(200)} = 1.15^\circ$ for GST at 300 °C. The peak broadening implies a grain refinement in the doped sample as predicted by the Scherrer's formula,⁴⁰ a result similarly observed by the transmission electron microscopy on GST and Ce-GST reported previously.²⁴ Notably, no XRD peak corresponding to the Ce-related intermetallic compounds was observed in Fig. 2(b). The Ce-GST hence remained in solid-solution form or, the Ce elements present in GST matrix as the solute atoms.

Figure 3(a) presents the correlation of annealing temperature with the grain size of chalcogenide samples deduced by the FWHM analysis of XRD profiles shown in Fig. 2 and TEM characterizations shown in Figs. 3(b)–3(e). The grain size of Ce-GST is apparently smaller than that of GST at the same annealing temperature, evidencing the grain refinement due to Ce doping. Moreover, the TEM micrographs depict the equiaxial grain structures with relatively uniform grain sizes in nanometer scale for both GST and Ce-GST. As illustrated by the electrical analysis presented below, the AC impedance spectroscopy is a feasible tool for analyzing the chalcogenide thin films within nano-scale grain sizes.

B. Electrical analysis

In this work, titanium (Ti) thin film was adopted as the electrodes of samples due to its Ohmic contact feature with the chalcogenides as revealed by the I - V measurement shown in Fig. 4(a). Moreover, the transmission line model (TLM) measurement⁴¹ revealed the specific contact resistance (R_S) of Ti with GST and Ce-GST is 19.8 Ω and 306.06 Ω , respectively, as illustrated by Fig. 4(b). The relatively low R_S 's for Ti/GST and Ti/Ce-GST systems indicate that Ti is a suitable electrode material for chalcogenides. Notably, the presence of contact resistance has been incorporated in subsequent

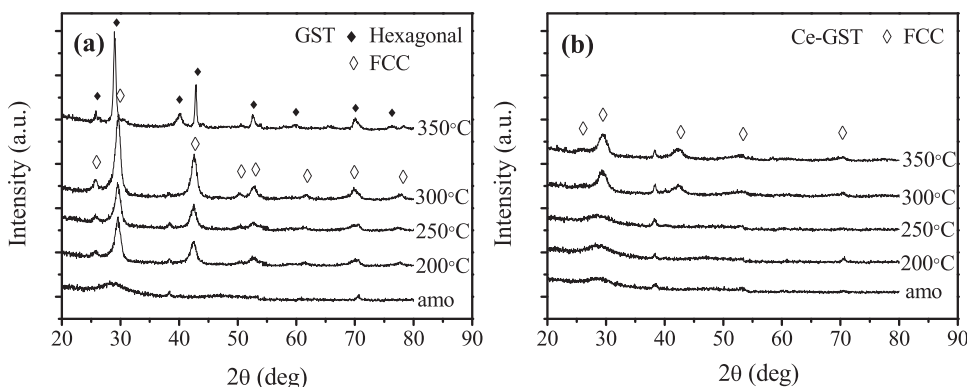


FIG. 2. XRD patterns of (a) GST and (b) Ce-GST layers subjected to 1 h annealing at various temperatures.

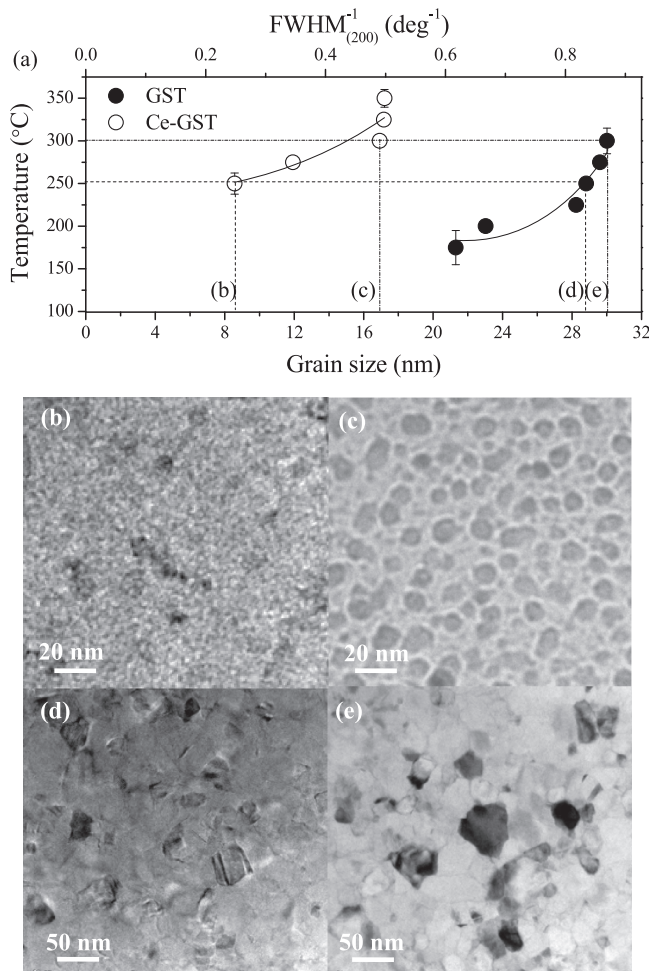


FIG. 3. (a) Correlation of annealing temperature with grain size of chalcogenide samples deduced by the XRD FWHM analysis shown in Fig. 2 and TEM characterizations. Plan-view TEM micrographs of Ce-GST layers annealed at (b) 250 °C and (c) 300 °C for 1 h and GST layers annealed at (d) 250 °C and (e) 300 °C for 1 h.

analysis based on the equivalent circuit models. It was found that the addition of R_S 's causes the shift of impedance plots (i.e., the plots of $-\text{Im}(Z)$ vs. $\text{Re}(Z)$) without altering the geometries of semi-circles corresponding to the grain and grain boundary. Since the analysis is aimed at those semi-circles, the incorporation of R_S hence has no influence on the results of electrical analysis once the electrode material is properly selected.

Figure 5 presents the resistance profiles of GST and Ce-GST as a function of the temperature deduced from the *in situ* electrical measurement. According to the derivatives of resistance profiles, the phase-transition temperatures (T_x 's) of GST and Ce-GST were determined as 153 and 219 °C, respectively. The increment of T_x in doped sample is ascribed to the stress field induced by the uniformly dispersed Ce solutes in GST matrix that inhibit the grain growth and coalescence during the recrystallization.²⁴ In addition to the dramatic improvement of thermal stability revealed by Fig. 5, a unique feature of Ce doping is that it does not suppress the resistance level of amorphous state, i.e., it effectively stabilizes the amorphous GST. Unlike other metallic dopants which often cause the resistance drop in amorphous state,^{10–22} Ce doping is able to preserve the resistance ratio

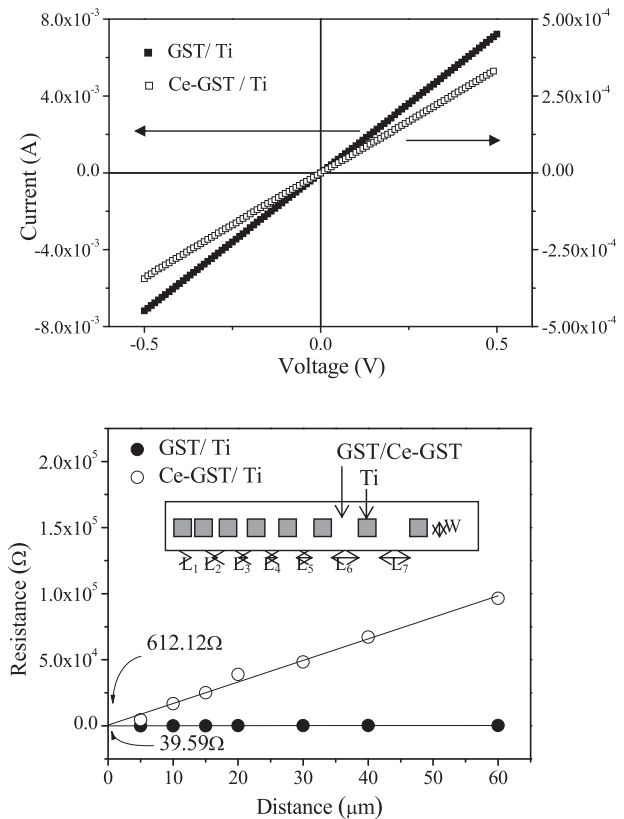


FIG. 4. (a) The I - V characteristics of Ti/GST and Ti/Ce-GST systems. The straight lines imply the Ohmic contact feature of Ti on GST and Ce-GST. (b) TLM measurement for the specific contact resistances of Ti on GST and Ce-GST layers subjected to 1 h annealing at 300 °C.

of amorphous to crystalline GST at about five orders of magnitude. This would benefit the signal contrast when Ce-GST is implanted in PRAM. As to the crystalline Ce-GST, its resistance level is moderately higher than that of pristine GST at the same temperature. This is ascribed to the grain refinement which increases the number of grain boundaries in doped sample. It amplifies the charge scattering effect and thus escalates the resistance level of crystalline Ce-GST.

A typical example of impedance plots deduced from the impedance analysis for 300 °C-annealed GST is shown in Fig. 6(a). The equivalent circuit for data analysis is also depicted in the inset at the bottom of Fig. 6(a). It was

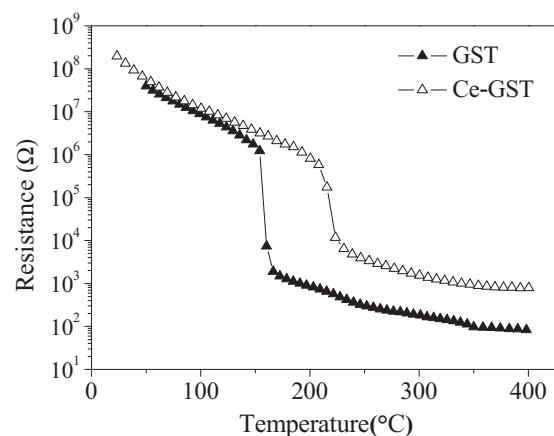


FIG. 5. Resistance profiles of GST and Ce-GST as a function of temperature.

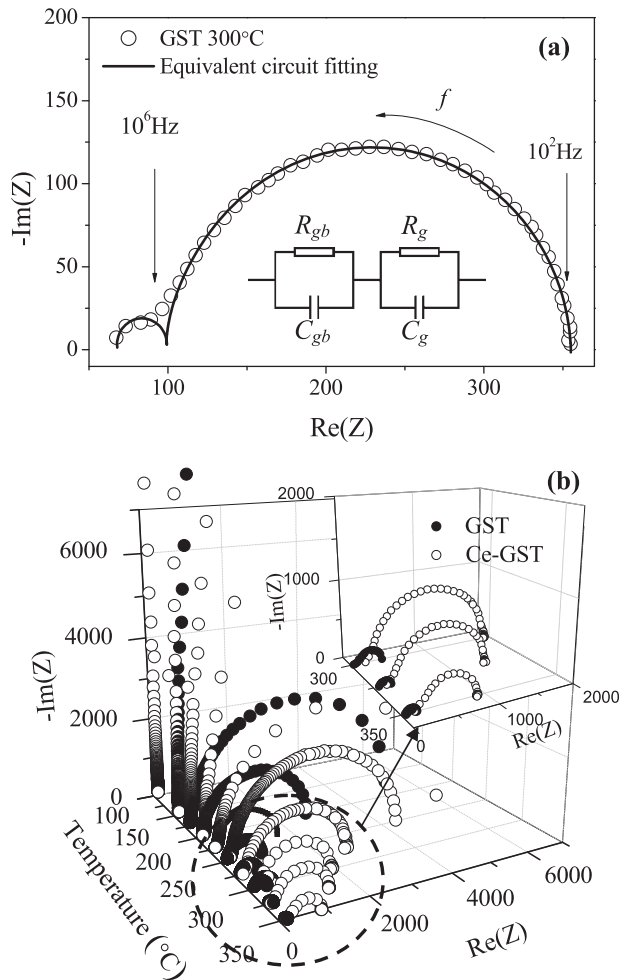


FIG. 6. (a) An example of impedance plots for GST sample subjected to 300 °C annealing for 1 h. The inset shows the equivalent circuit model for data analysis. (b) Evolution of first semicircles or, the grain-boundary response, for GST and Ce-GST as a function of temperature based on BLM analysis.

constructed in terms of the BLM that the electrical response of samples can be termed as a parallel RC circuit with the grain and grain-boundary components acting in series manner. As illustrated in Fig. 6(a), the impedance plot can be deconvoluted into two semicircles, e.g., the low-frequency semicircle corresponds to the grain-boundary response (i.e., the first semicircle), whereas the high-frequency semicircle corresponds to the grain response (i.e., the second semicircle). Notably, the BLM is essentially applied to the polycrystalline samples since its hypotheses include the cubic grains and laterally homogeneous grain boundaries with identical physical properties. On the contrary, the structure irregularity in amorphous sample implies no preferential path for current flow. The weak frequency response hence diminishes the semicircle feature in impedance plot for amorphous sample. As a result, the progress of amorphous-to-crystalline transition in GST can be elucidated by the evolution of impedance plots for the samples annealed at various temperatures.

Figure 6(b) presents the evolution of first semicircles (i.e., the grain-boundary response) for GST and Ce-GST as a

function of temperature. It can be readily seen that, due to the grain refinement in doped sample, the $\text{Re}(Z)$ level of Ce-GST is higher than that of pristine GST at the same temperature. This is in agreement with the resistance profiles presented in Fig. 5 which depicts a higher resistance for crystalline Ce-GST than that for pristine GST at the same temperature. As mentioned above, the emergence of grain-boundary semicircle can be regarded as the onset of phase transition in chalcogenides. Figure 6(b) indicates that such semicircles separately emerge at 160 and 225 °C for GST and Ce-GST, about the same as the values of T_x deduced by the resistance profiles depicted in Fig. 5. Due to the difference in atomic sizes ($r_{\text{Ce}} = 0.185 \text{ nm}$; $r_{\text{Ge}} = 0.125 \text{ nm}$; $r_{\text{Sb}} = 0.145 \text{ nm}$; $r_{\text{Te}} = 0.140 \text{ nm}$), Ce doping causes the distortion of GST lattice and the resulted stress field would retard the recrystallization. This implies a higher T_x for Ce-GST and the hindrance of grain-boundary motions consequently delays the emergence of grain-boundary semicircles for doped sample.

In order to explore the limitations on impedance analysis in terms of the grain size, the n-GCM analysis proposed by Kidner *et al.*³⁸ was also adopted for electrical analysis. Such an analysis considers the effects of grain size on electrical properties by calculating the grain-core volume fractions (ϕ) of sample as its grains evolve from the microcrystalline form ($\phi \rightarrow 1$) to the nanocrystalline form ($\phi \rightarrow 0$). Figure 7(a) plots ϕ against the test temperature for GST and Ce-GST samples in accord with the n-GCM analysis. Compared with Ce-GST, the pristine GST was found to possess a larger ϕ value at the same temperature and hence, a much obvious grain size effect on the electrical properties.

Variations of R_{gb} , R_g , C_{gb} , and C_g as a function of temperature deduced from the impedance analysis based on the BLM are separately plotted in Figs. 7(b)–7(e). The variations of R_{gb} and R_g as a function of temperature calculated in terms of the formulation proposed by Kidner *et al.*³⁸ are also presented in Figs. 7(b) and 7(c). It can be seen that the BLM and n-GCM analyses yield a rather similar R_{gb} behavior against the temperature as illustrated by Fig. 7(b). Though Fig. 7(c) indicates some discrepancies in R_g 's as predicted by these two equivalent circuit models, the levels of R_g 's are in fact far insignificant than that of R_{gb} 's. As a result, the classical BLM analysis remains in an appropriate tool for impedance analysis on the samples with nano-scale grain sizes.

As shown in Figs. 7(b) and 7(c), decrease of R_{gb} and R_g with the increase of temperature for GST and Ce-GST illustrates that annealing treatment improves the crystallinity and eliminates the grain boundaries in both samples. This suppresses the scattering of charge carriers during transport and hence results in the decrease trend of resistance. Notably, both R_{gb} and R_g for Ce-GST are always higher than that of GST at the same temperature. This is ascribed to the grain refinement effect in doped sample, resulting in a higher amount of grain boundaries to impede the carrier transport in Ce-GST.

It is known that the characteristic time (τ) of the parallel RC circuit can be expressed as $\tau = RC$.⁴² The decrease trend of R_{gb} hence implies the increase trend of C_{gb} as shown in Figs. 7(b) and 7(d). Moreover, the decrease trend of R_g with

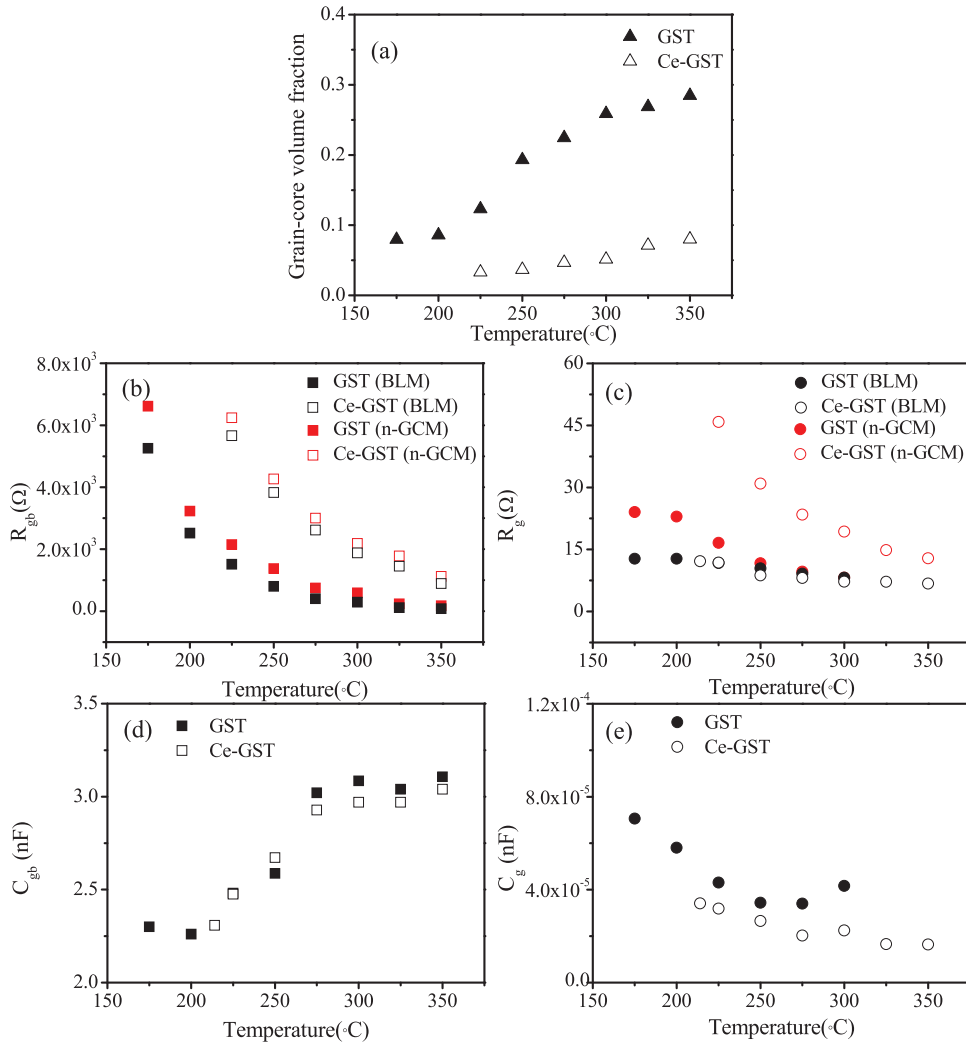


FIG. 7. (a) Grain-core volume fraction (ϕ) (b) R_{gb} , (c) R_g , (d) C_{gb} , and (e) C_g of GST and Ce-GST as a function of temperature deduced by BLM and n-GCM analyses.

the increase of temperature shown in Fig. 7(c) seems to imply the variation of C_g shown in Fig. 7(e) is against the RC circuit principle. A comparison of Figs. 7(c) and 7(e) found that the magnitude of C_g is in fact negligibly smaller than that of C_{gb} and the insignificant C_g should result from the thermal fluctuation effects. C_g is known to correlate to the presence of electric dipoles in the grains. Since this study collected the electrical data in an *in situ* manner, the randomization of dipole alignment became severe with the increase of test temperatures and consequently weakened the performance of C_g .

Figures 7(b)–7(e) clearly indicate that the electrical properties associated with grain-boundary are far more significant than those corresponding to grain and R_{gb} is the physical property most sensitive to the change of test temperature. Grain boundaries are well-known structural discontinuities adverse to the electrical conductivity of polycrystalline samples. Deep electron trap states may form in grain boundaries, causing the charge build-up and pinning effects. The dominance of grain boundaries in the charge transport process of chalcogenides hence implies that the electrical properties relevant to grain boundaries can be adopted to analyze their phase-transition behaviors.

The data of R_{gb} presented in Fig. 7(b) were fitted by a sigmoid-shaped profile as follows:

$$\frac{R_{\max} - R}{R - R_{\min}} = \exp\left(\frac{T - T_x}{\Delta T}\right), \quad (1)$$

where R_{\max} and R_{\min} is the maximum and minimum values of R_{gb} shown in Fig. 7(b) and ΔT is the temperature span of recrystallization process. As indicated by the results summarized in Table I, T_x 's obtained by such a curve fitting analysis are 148 and 216 °C for GST and Ce-GST, respectively, which are in good coincidence with the values of T_x deduced by resistance profiles presented in Fig. 5. Moreover, Table I shows that Ce-GST exhibits a wider ΔT span in comparison with GST. This implies that Ce doping escalates the barrier of phase transition and thus delays the phase transition. This is consistent with the late emergence of grain-boundary semicircles in impedance plot for Ce-GST as depicted in Fig. 6(b). Analytical results presented above illustrate alien-element doping hinders the phase transition although it might improve the thermal stability of GST. This might affect the

TABLE I. Curve fitting results of R_{gb} for GST and Ce-GST.

	R_{\max} (Ω)	R_{\min} (Ω)	T_x (°C)	ΔT (°C)
GST	2.6×106	710.2	148	3.3
Ce-GST	4.3×106	1527.4	216	11.1

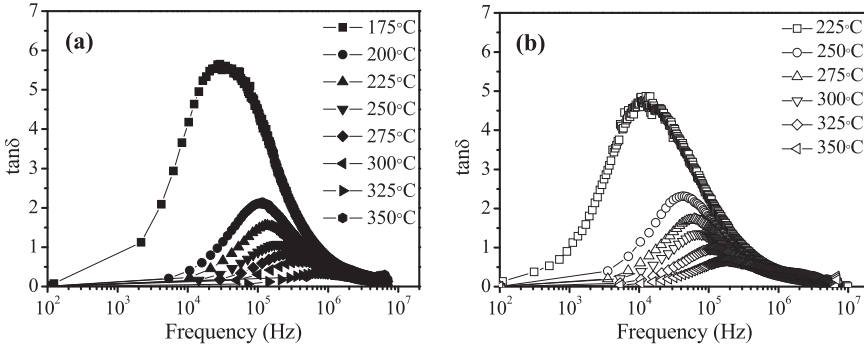


FIG. 8. Frequency dependence of $\tan \delta$ at different temperatures for (a) GST and (b) Ce-GST.

operational characteristics of PRAM containing doped chalcogenides and hence further investigation is required.

Loss tangent ($\tan \delta$) profiles of GST and Ce-GST at different temperatures as a function of measured frequency are separately plotted in Figs. 8(a) and 8(b). Note that there is no characteristic peak in the $\tan \delta$ plot at the temperatures below T_x , implying the absence of space charge response in amorphous chalcogenides. Moreover, the loss phenomena occurred in the frequencies less than 1.5 MHz, indicating the space-charge polarization is the dominant mechanism in GST samples. As mentioned above, grain boundaries can be termed as the transport barrier to induce the charge accumulation at the interfacial regimes. As the space charges at the grain boundaries alter the local electric field, the interfacial polarization hence results in the semicircle feature corresponding to grain boundaries presented in Fig. 6.

Figures 8(a) and 8(b) also indicate that the peaks of $\tan \delta$ shift toward the high-frequency side for both samples when temperature is increased and the loss value of Ce-GST is higher than that of GST at the same temperature. The loss tangent peak emerging at a specific frequency (f_{max}) implies the occurrence of dipole relaxation in the samples. The thermal fluctuation promotes the dipole relaxation and hence the peak shifts towards the higher-frequency side when temperature is increased. The higher loss property of Ce-GST indicates that doping amplifies the interfacial polarization in GST samples. It is known that Ce possesses a relatively small electronegativity (χ) in comparison with the elements of GST ($\chi_{Ce} = 1.2$; $\chi_{Ge} = 1.8$; $\chi_{Sb} = 1.9$; $\chi_{Te} = 2.1$). The difference in χ might alter the chemical bond types in Ce-GST

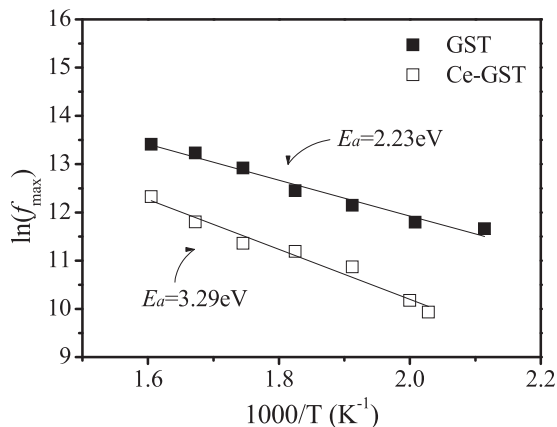


FIG. 9. Logarithm of the f_{max} of $\tan \delta$ profiles versus the reciprocal of the temperature for GST and Ce-GST.

and enhance the rigidity of dipole motions. This dipole motions in alternative bias field were hence restricted, resulting in a higher $\tan \delta$ value for doped sample.

The circuit theory indicates that f_{max} is related to the characteristic time τ by the expression of $\tau = \omega^{-1} = RC$, where $\omega = 2\pi f_{max}$.⁴² Note that τ depicts the time required to charge the capacitor in the RC circuit. Figure 8 shows that the f_{max} for Ce-GST occurs in the frequency range of 22–600 kHz, comparatively lower than that of GST in the range of 75 kHz–1 MHz. As a result, the τ_{Ce-GST} is larger than τ_{GST} , implying the time of charge transit across the grain boundaries in Ce-GST is longer than that in GST. This supports the argument that Ce-doping enhances the interfacial polarization in chalcogenides proposed previously.

According to McCrum *et al.*,⁴³ $\tan \delta$ can be expressed as

$$\tan \delta = \frac{\omega C_{gb} R_g}{1 + (\omega R_g)^2 (C_g + C_{gb}) C_g}. \quad (2)$$

As indicated by Figs. 7(b)–7(e), $R_{gb} > R_g$ and $\omega^2 R_g R_{gb} C_{gb}^2 \gg 1$. The angular frequency corresponding to the maximum of $\tan \delta$, ω_{max} , can thus be expressed as

$$\omega_{max} = \frac{1}{R_g} \sqrt{\frac{1}{C_g (C_g + C_{gb})}}. \quad (3)$$

The variation of ω_{max} as a function of temperature can be plotted by substituting the values of R_g , C_g , and C_{gb} as depicted in Figs. 7(c)–7(e). By assuming the Arrhenius behavior of τ ,⁴⁴ activation energy (E_a) of the phase-transition process can be determined by the slope of the plot of $\ln(f_{max})$ versus reciprocal of temperature as presented in Fig. 9. The values of E_a for GST and Ce-GST were found to be 2.23 and 3.29 eV, respectively. The increase of E_a due to element doping is in agreement with the values deduced from conventional methods such as Kissinger's analysis.⁶ Analytical results presented above hence demonstrated that the *in situ* AC impedance measurement can be an alternative tool for analyzing the phase-transition kinetics of chalcogenides.

IV. CONCLUSIONS

This work demonstrated that *in situ* AC impedance spectroscopy is a feasible tool to characterize the phase-transition behaviors of chalcogenide thin films with the nano-scale grain sizes. The impedance analysis in conjunction with the BLM and n-GCM models illustrated that the physical

properties associated with the grain boundaries dominate the phase-transition behaviors of chalcogenide samples. Moreover, the loss tangent property deduced from the impedance measurements can be applied to determine the E_a value of the phase transition. In this study, the values of E_a for pristine GST and Ce-GST were found to be 2.23 and 3.29 eV, respectively, which are in agreement with those determined by the conventional methods such as Kissinger's analysis. The high E_a observed in the doped sample is ascribed to the difference in the atomic size and electronegativity of the Ce dopant with the elements of GST. The Ce dopant disturbs the space charge distribution and amplifies the interfacial polarization in GST, leading to the higher resistance and loss tangent features in Ce-doped GST.

ACKNOWLEDGMENTS

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