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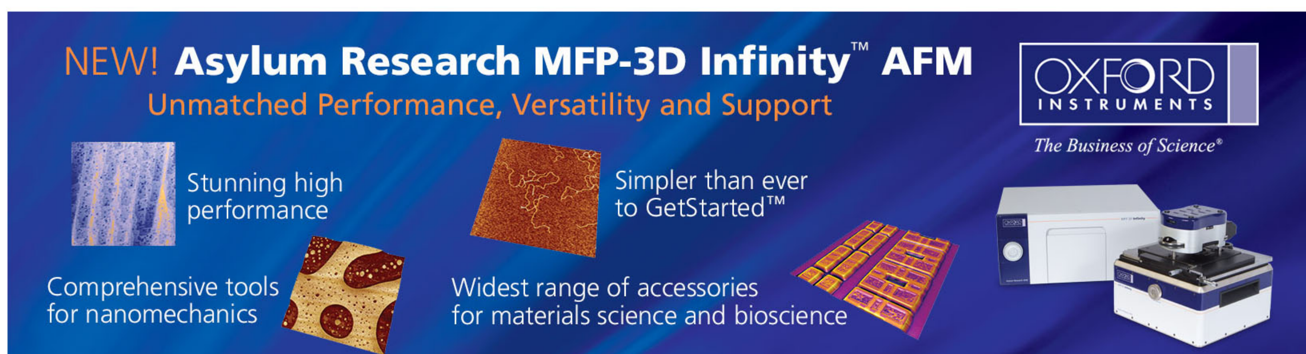

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Memory characteristics of laser-crystallized polycrystalline-silicon silicon-oxide-nitride-oxide-silicon thin-film transistor with location-controlled grain boundary perpendicular to the channel

I-Che Lee, Chun-Chien Tsai, Hsu-Hang Kuo, Po-Yu Yang, Chao-Lung Wang, and Huang-Chung Cheng
Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan

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An excimer-laser-crystallized polycrystalline-silicon silicon-oxide-nitride-oxide-silicon thin-film transistor with recessed-channel structure has been designed to achieve only one grain boundary with a protrusion perpendicular to the channel for investigating the grain boundary location effects on the memory characteristics. After programming, the devices demonstrated better memory characteristics as the grain boundary was allocated near the source junction. In contrast, the memory characteristics were degraded when the grain boundary was located near the drain junction. The phenomenon was explained by the 2-D device simulation and the energy band diagrams. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4724314]

Charge-trapping type memory devices, for example, silicon-oxide-nitride-oxide-silicon (SONOS) type memories, have been extensively studied for a possible replacement of the traditional floating-gate memories because of its many advantages, such as simple process integration, high program/erase (P/E) speed, and better potential for scalability.

Recently, a new device composed of SONOS type memory and polycrystalline-silicon (poly-Si) thin-film transistor (TFT) has been demonstrated to achieve the integration of memory and transistor functions. Poly-Si TFTs have been developed in wide range of applications, such as three-dimensional integrated circuits (3-D ICs),[1] and system-on-panel (SOP) applications.[2] However, poly-Si TFTs without high carrier mobility might encounter difficulties to achieve these advanced applications. Several technologies have been proposed for achieving high mobility, especially excimer-laser crystallization (ELC) technology.[3,4] Moreover, the Si protrusions fabricated by ELC occurred at grain boundaries and some reports utilized the protrusions to enhance memory performance.[5] Consequently, the ELC poly-Si SONOS TFTs have attracted more attention on the embedded system or SOP applications. Although high-performance poly-Si SONOS TFTs could be attained via ELC, the electrical characteristics and uniformity were significantly affected by the random distribution of the grain boundaries along with protrusions in the channel. Therefore, the influence of the grain-boundary location on the memory characteristics of poly-Si SONOS TFTs needed to be realized and controlled.

In order to control the grain boundary location, a SONOS TFT adopted recessed-channel (RC) structure was fabricated via ELC.[6,7] By means of such structure and proper design, the device could be fabricated to possess single-one grain boundary perpendicular to the channel direction near the source or drain junction. Consequently, the better memory characteristics could be obtained as the single perpendicular grain boundary accompanying with a protrusion and corresponding programmed charge located near the source junction. The mechanism was also simulated and proposed.

Figure 1(a) depicts the structure of the proposed poly-Si SONOS TFTs crystallized with ELC. At first, a 100-nm-thick intrinsic amorphous silicon (a-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C on oxidized silicon wafers. Following the etching of the a-Si layer in the channel region, another intrinsic 100-nm-thick a-Si layer was subsequently deposited to form a RC structure. Afterwards, the a-Si films were irradiated by KrF excimer laser ($\lambda = 248$ nm) at room temperature and the energy density of 480 mJ/cm^2 to attain only one perpendicular grain boundary in the RC structure.[6,7] After the definition of the active regions, sequential deposition of an oxide-nitride-oxide (ONO) stacked gate dielectric (5 nm/10 nm/15 nm) and an 100-nm-thick *in-situ* phosphorus-doped polysilicon layer were formed by LPCVD. After the definition of the gate electrodes, a self-aligned phosphorous implantation with a dose of 5×10^{15} cm^{-2} at 36 keV was carried out to form the source and drain regions. Next, a TEOS passivation oxide layer was deposited, and the source/drain-implanted dopants activation was performed by the furnace anneal at 600 °C for 8 h. Finally, standard backend processes were conducted to complete the fabrication of the RC ELC SONOS devices.

The resultant SEM image of poly-Si thin film after Secco etching and the corresponding device design with $L = W = 0.7\ \mu$m in the forward mode, i.e. the perpendicular grain boundary located near the source junction, are also shown in Fig. 1(b). The poly-Si SONOS TFTs were programmed at $V_g = 20$ V, $V_s = 0$ V, and $V_d =$ floating for 10 ms. A typical erase voltage was -20 V for 50 ms. The equivalent device for the forward mode was the near-source-programmed device with one grain boundary (NSP-OG). The NSP-OG device measured with reverse mode could be considered as the near-drain-programmed device with one grain boundary (NDP-OG). It is worthy to notice that a spatially controlled longitudinal silicon grain with a length of 0.9 μm and only one perpendicular grain boundary accompanying with a protrusion were formed in the channel.

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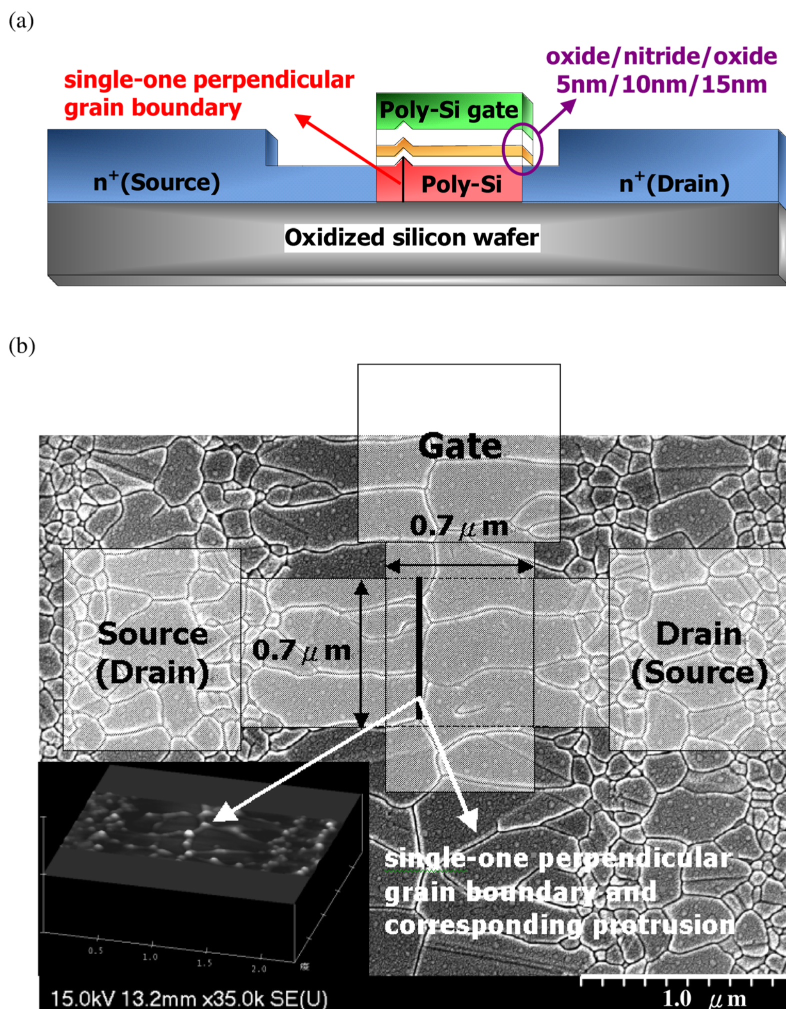

FIG. 1. (a) The structure of the proposed poly-Si SONOS TFTs crystallized with ELC. (b) The SEM image of ELC poly-Si film after Secco etching with proposed structure, the schematically illustrated device design, and the corresponding AFM graph.

After the programming, the memory characteristics of the devices were measured in the forward and reverse modes and shown in Fig. 2. The threshold voltages were shifted positively due to the electrons stored in the nitride layer above the corresponding protrusion at the perpendicular grain boundary. The threshold voltage was defined as the gate voltage with a normalized drain-current of $I_{ds} = (L/W) \times 10^{-8}$ A at $V_{ds} = 1$ V. For the NSP-OG device, the threshold voltage shift, namely the memory window, was

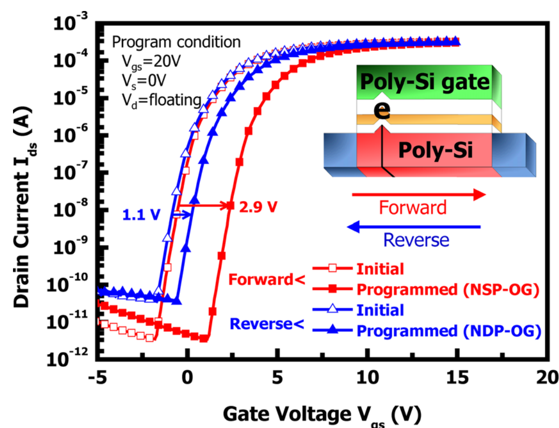

FIG. 2. The memory characteristics of the poly-Si SONOS TFTs in the forward and reverse mode with the program condition $V_{gs} = 20$ V, $V_s = 0$ V, and V_d = floating.

2.9 V, as indicated by the arrows in Fig. 2. In contrast, for the NDP-OG device, the memory window was only 1.1 V. This means that the memory window was degraded when the single perpendicular grain boundary was located near the drain junction. In addition, the retention times of the devices extrapolated up to ten years could sustain the memory window of 2.0 V at room temperature.

To clarify the effects of the location of the perpendicular grain boundary with the corresponding protrusion on the memory characteristics, the Atlas simulation tool was utilized to simulate the conduction band diagrams of three types of devices, the non-programmed device with no grain boundary (NP-NG), the NDP-OG, and the NSP-OG at different V_{ds}. Under $V_{ds} = 0$ V, the NP-NG devices exhibited flat conduction band except a little downturn to the source/drain potential. As for the NSP-OG species, a higher hump of the conduction band could be formed near the source when only the grain boundary effect was considered, as shown in Fig. 3(a). After the programming, the amount of injected charge was set to $5 \times 10^{17}/cm^3$ and a higher hump of the conduction band near the source was also observed when only the programmed charge effect was considered. Therefore, a much higher hump of the conduction band came as a result of the total effects of grain boundary and programmed charge for the NSP-OG devices as well as the NDP-OG ones. The barrier height due to grain boundary was 0.16 eV. In contrast, under $V_{ds} = 1$ V, a smooth monotonically decrease of the

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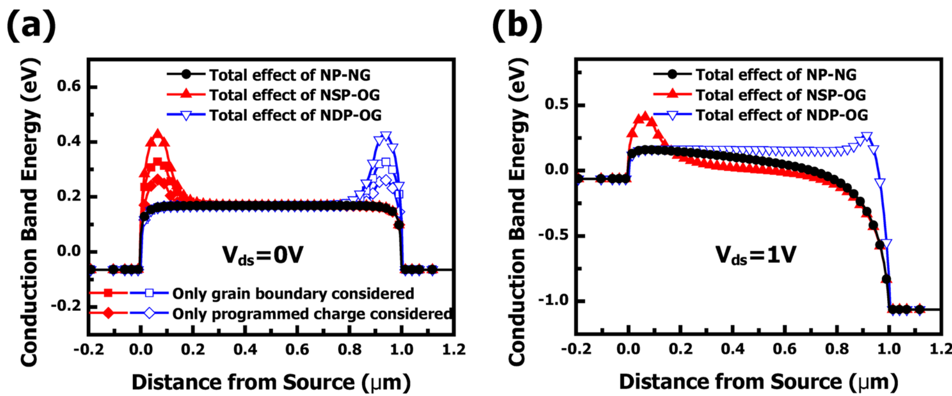

FIG. 3. (a) Simulation results of the conduction band diagrams at $V_{ds} = 0$ V for three types devices, NP-NG, NSP-OG, and NDP-OG. (b) The conduction band diagrams at $V_{ds} = 1$ V.

conduction band was found for the NP-NG devices as shown in Fig. 3(b). However, the raised potential barrier caused by the grain boundary and programmed charge near the source was significant higher than near drain one as the V_{ds} increasing to 1 V, as shown in Fig. 3(b).

According to previous reports, since the grain boundary had higher resistance than in grain, the potential drop was larger as the electric field higher, and, therefore, the potential barrier near drain junction was lowered more than near source junction.[8] The potential barriers in the band diagram after programming came from two sources. One was the negative carriers seized in the trap states at the grain boundaries in the channel. The other was the electrons stored in the nitride layer. Since the programming electric filed could be enhanced by the grain boundary protrusion caused by ELC,[5,7] plenty of electrons were stored above the grain boundary protrusion. As increasing V_{ds}, not only the grain boundary but also the programmed charge induced potential barriers near drain junction were lowered more than near source junction, as shown in Fig. 3(b). Consequently, a large memory window was observed for the forward mode.

To further investigate the grain boundary location effects on the memory characteristics, the device was also programmed at $V_g = 20$ V and $V_s = V_d = 0$ V for 10 ms. After the programming, the memory characteristics of the devices were measured in the forward and reverse modes and shown in Fig. 4(a). The results were similar to those in Fig. 2. For the forward mode, the memory window was 3.06 V while that was 2.9 V in case of the program condition at $V_g = 20$ V, $V_s = 0$ V, and V_d = floating. For the reverse mode, the memory window was 1.38 V while that was 1.1 V in case of the program condition at $V_g = 20$ V, $V_s = 0$ V, and V_d = floating.

Furthermore, when the devices possessed the grain boundary located at the middle of the channel, the memory characteristics were exhibited in Fig. 4(b). After programming at $V_g = 20$ V and $V_s = V_d = 0$ V for 10 ms, the asymmetrical memory characteristics were not observed. Instead, it was observed that the memory windows of the devices were similar for forward and reverse modes. Since the grain boundary located at the middle of the channel, the potential barriers were symmetric for reads in forward and reverse modes.

Via a simple RC structure, the ELC poly-Si SONOS TFT possessing only one perpendicular location-controlled grain boundary has been fabricated to investigate the grain-boundary location effects on the memory characteristics. The NSP-OG devices exhibited a wide memory window of 2.9 V. In contrast, the NDP-OG devices displayed a narrow memory window of 1.1 V. The perpendicular grain boundary along with programmed electrons in the nitride would induce a higher potential barrier height in the channel. As the grain

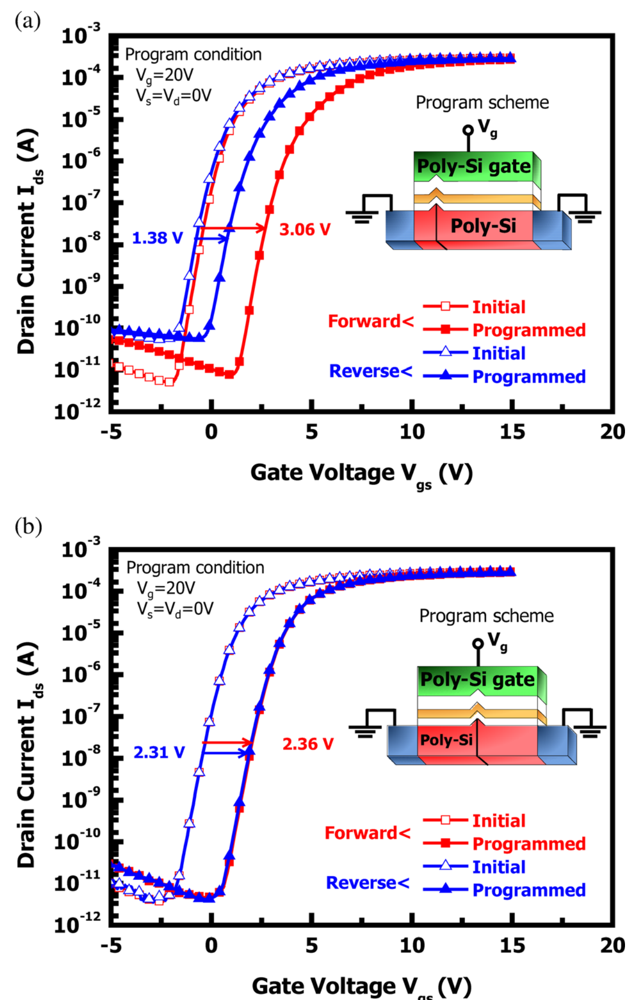

FIG. 4. (a) The memory characteristics of the poly-Si SONOS TFTs in the forward and reverse mode with the program condition $V_g = 20$ V, and $V_s = V_d = 0$ V. (b) The memory characteristics of the poly-Si SONOS TFTs in the forward and reverse mode for the single perpendicular grain boundary located at the middle of channel with the program condition $V_g = 20$ V, and $V_s = V_d = 0$ V.

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boundary and programmed electrons controlled near source, the device exhibited a wider memory window. In contrast, the device displayed a narrow memory window while the grain boundary and programmed electrons located near drain. A simulation result was utilized to prove that the potential barrier, which was caused by the grain boundary trap states and the programmed electrons, was lowered more in the drain junction than in the source junction.

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