A Novel Scheme for Fabricating CMOS Inverters With Poly-Si Nanowire Channels

Chia-Hao Kuo, Horng-Chih Lin, *Senior Member, IEEE*, I.-Che Lee, Huang-Chung Cheng, and Tiao-Yuan Huang, *Fellow, IEEE*

***Abstract*—A novel complementary metal–oxide–semiconductor inverter with poly-Si nanowire channels is proposed and demonstrated in this letter. The scheme employs a clever tilted-angle implant process in the fabrication; therefore, the formation of the source and drain of both p-channel and n-channel devices requires only one lithographic step. The fabricated n-channel and p-channel field-effect transistors in the inverters show a high ON/OFF current ratio, an acceptable subthreshold swing, and a symmetric driving current, thus enabling the realization of excellent characteristics of the inverters.**

***Index Terms*—CMOS inverter, poly-Si, system-on-panel (SoP), thin-film transistor (TFT).**

I. Introduction

RECENTLY, poly-Si thin-film transistors (TFTs) with nanowire (NW) channels have gained increasing attention and been regarded as a promising building block for future 3-D and large-area electronics [1]–[5]. The key attributes of NW structures are low leakage current, subthreshold swing (SS), and improved short-channel effects [6], [7], which are ascribed to the substantially reduced defects and grain boundaries in the poly-Si NW [1]. With the significantly improved device performance, the poly-Si NW devices appear to be promising for future system-on-panel (SoP) applications with the pixel array, driver, memory, and central processing unit all integrated on the same panel.

In this letter, we propose and successfully demonstrate a novel scheme for fabricating CMOS inverters with NW channels. The scheme is modified from the approach described in our previous work [1] by ingeniously incorporating tilted-angle implant processes to form the source/drain (S/D) regions of the p-channel and n-channel devices. With the proposed scheme, a one-mask-count-only S/D formation process can be realized for the CMOS inverters. The device fabrication is simple, without resorting to advanced lithographic tools for forming the NW structures [1], and is compatible with planar TFT processes [8].

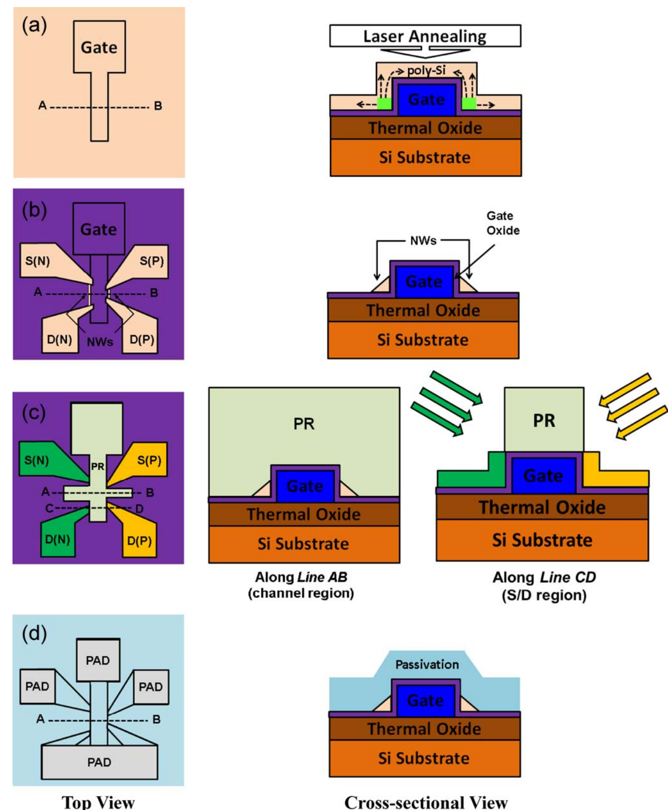

Fig. 1. Major process steps shown in both top and cross-sectional views for fabricating the CMOS inverter. (a) Crystallization of the amorphous Si layer deposited over the common-gate. (b) Definition of the S/D and sidewall NW channels. (c) Respective doping of S/D of p- and n-channel devices with two separate tilted-angle implantations. (d) Surface passivation and metallization.

II. Device Structure and Fabrication

The fabrication process flow of the proposed CMOS inverter in both top and cross-sectional views is depicted in Fig. 1. The starting substrates were 6-in silicon wafers capped with a thick oxide layer. After forming an *in situ* doped n^+ poly-Si gate, a 20-nm-thick tetraethylorthosilicate (TEOS) oxide was deposited to serve as the gate dielectric by low-pressure chemical vapor deposition (LPCVD) system. A 100-nm amorphous Si (α-Si) layer was then deposited by LPCVD at 550 °C. Thereafter, the deposited α-Si layer was recrystallized by an excimer-laser annealing (ELA) treatment [see Fig. 1(a)] with a laser energy density of 560 mJ/cm^2 at room temperature in a vacuum chamber of 10^{-3} torr. Details about the process development

Manuscript received February 21, 2012; accepted March 13, 2012. Date of publication May 1, 2012; date of current version May 18, 2012. This work was supported in part by the Ministry of Education in Taiwan through the Aim for the Top University (ATU) Program and in part by the National Science Council under Contract NSC 99-2221-E-009-172 and Contract NSC 99-2221-E-009-167-MY3. The review of this letter was arranged by Editor W. S. Wong.

C.-H. Kuo, I.-C. Lee, H.-C. Cheng, and T.-Y. Huang are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan.

H.-C. Lin is with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, and also with the National Nano Device Laboratories, Hsinchu 300, Taiwan (e-mail: hclin@faculty.nctu.edu.tw).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2012.2191585

0741-3106/$31.00 © 2012 IEEE

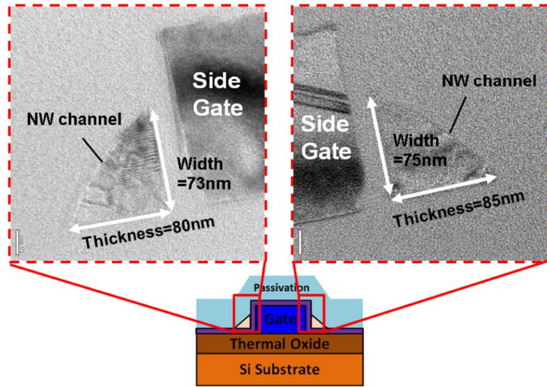

Fig. 2. TEM pictures showing the cross-sectional images of NW channels for devices contained in a fabricated inverter. Channel widths are 73 and 75 nm for n- and p-type devices, respectively

can be found in [9]. Next, a photoresist (PR) pattern was generated to cover both n-type and p-type S/D contact pad regions. Afterward, an anisotropic plasma dry etching was employed to form the S/D regions. In this step, the sidewall-spacer NW channels were simultaneously formed [1], abutting against the gate [see Fig. 1(b)]. After defining the S/D pads and channel regions, n-type S/D doping was then performed with P_{31}^+, at 15 keV, at a tilt angle of 60°, and at 5×10^{15} cm^{-2} dose, whereas p-type S/D doping was performed with BF_2^+, at 33 keV, at a tilt angle of $-60°$, and 5×10^{15} cm^{-2} dose [see Fig. 1(c)]. Note that the tilt angle is relative to the direction normal to the wafer surface, as shown in the figure. To prevent the channel region from being doped during the tilted-angle ion-implantation processes, a PR was generated in advance to cover the NW channels (as shown in Fig. 1(c) with the cross-sectional view along the AB line). Then, a 500-nm-thick TEOS oxide layer was deposited to serve as the passivation layer. Finally, the fabrication was completed after forming the contact holes and Al pads [see Fig. 1(d)]. The transmission electron microscopic (TEM) cross-sectional views of a fabricated device showing the common gate and the NW channels of both n-channel and p-channel devices are given in Fig. 2. The widths of the sidewall NW channel were determined to be 73 nm for the n-channel FET and 75 nm for the p-channel FET.

As compared with conventional planar CMOS inverters that typically demand six masks to fabricate, the proposed NW inverter needs only five masks with the process flow illustrated in Fig. 1. Moreover, when adopting the proposed NW inverter to construct practical circuits such as static random access memory cells or ring oscillators, potential area saving could be achieved considering the compactness of the tiny NW channels.

III. Results and Discussion

The gate voltage (V_G) dependence of gate leakage current and the transfer characteristics I_D–V_G of fabricated n-channel and p-channel FETs, which are formed on a poly-Si NW-channel CMOS inverter, with channel lengths of 3 and 1 μm, respectively, are shown in Fig. 3(a). Note that, as shown in Fig. 2, both n-channel and p-channel devices show almost identical effective channel width, as dictated by the cross-sectional area of the NW. In order to compensate the mobility difference between electrons and holes, we have designed the ratio of channel length between the n-channel FET and the p-channel

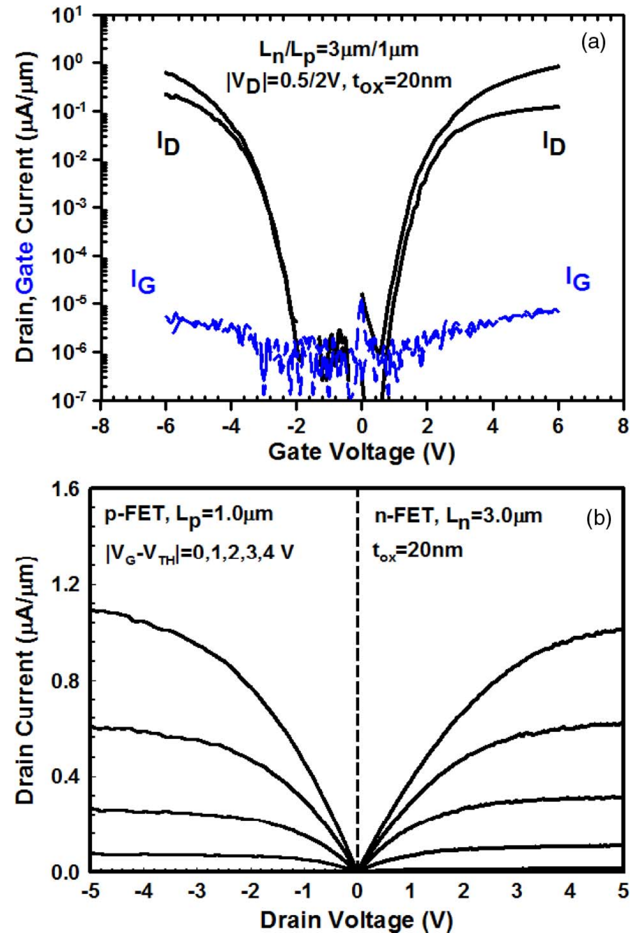

Fig. 3. (a) Transfer and (b) output I–V characteristics of an n-channel device with $L_n = 3$ μm and a p-channel device with $L_p = 1$ μm. The two devices are contained in the same inverter.

FET (L_n/L_p) to be 3 : 1. Excellent device performance for n-channel and p-channel FETs are observed with a small gate leakage current ($< 10^{-11}$ A/μm), a large ON/OFF current ratio ($\sim 10^6$), and small drain-induced barrier lowering with values of 17 mV/V for the n-channel TFT and 10 mV/V for the p-channel TFT, respectively. The field-effect mobility data extracted from transconductance are 23 and 12 cm^2/V $\cdot$ s for n-channel and p-channel devices, respectively. Both devices show an acceptable SS of 227 mV/dec for the n-channel FET and 280 mV/dec for the p-channel FET, respectively. It is believed that the device performance can be further improved by further optimizing the process and structure design such as a reduced gate oxide and dimensions of NWs [10]. The extracted threshold voltage V_T, which is defined as V_G at $I_D = (W/L) \times 10^{-8}$ A, are 1.9 and -2.86 V for n-channel and p-channel FETs, respectively, measured at $|V_D| = 0.5$ V. The asymmetry in V_T is mainly ascribed to the use of the n^+ poly gate. Such a mismatch in V_T between n-channel and p-channel FETs can be reduced if a midgap metal (e.g., TiN) is used instead.

The output characteristics of n-channel and p-channel FETs, as shown in Fig. 3(b), depict roughly symmetric driving current with values of 1.01 and 1.09 μA/μm at $|V_D| = 5$ V and $|V_G - V_T| = 4$ V, respectively. The typical voltage transfer characteristics (VTC) and the voltage gain ($= -dV_{OUT}/dV_{IN}$) of the fabricated poly-Si NW-channel CMOS inverter at a supply voltage of 5 V are illustrated in

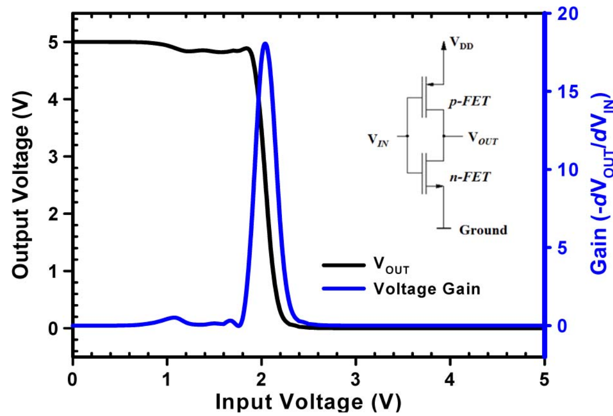

Fig. 4. Voltage transfer characteristics and voltage gain of a fabricated CMOS inverter at a supply voltage of 5 V. The inverter is consisted of the two devices characterized in Fig. 3.

Fig. 4. The inverter shows sharp transfer characteristics and a high voltage gain of around 18 at $V_{IN} = 2$ V. Although the symmetry in V_T is yet to be optimized, the observed VTC curve clearly confirms large noise margins.

IV. Conclusion

In summary, a novel poly-Si CMOS inverter featuring NW channels has been fabricated and characterized. This scheme utilizes sidewall-spacer etching technique to define the NW channels and tilted-angle implant processes to separately dope the S/D of the p-channel and n-channel devices in the inverter. Owing to the superior characteristics of the fabricated p-channel and n-channel devices, excellent VTCs and high voltage gain are obtained. Considering its process simplicity and compatibility with modern manufacturing, this scheme appears to be very promising for future SoP applications.

Acknowledgment

The authors would like to thank the National Nano Device Laboratories and the Nano Facility Center of National Chiao Tung University for assistance in device fabrication.

References

[1] H. C. Lin, M. H. Lee, C. J. Su, T. Y. Huang, C. C. Lee, and Y. S. Yang, "A simple and low-cost method to fabrication TFTs with poly-Si nanowire channel," *IEEE Electron Device Lett.*, vol. 26, no. 9, pp. 643–645, Sep. 2005.

[2] C. J. Su, H. C. Lin, and T. Y. Huang, "High-performance TFTs with Si nanowire channels enhanced by metal-induced lateral crystallization," *IEEE Electron Device Lett.*, vol. 27, no. 7, pp. 582–584, Jul. 2006.

[3] M. Im, J. W. Han, H. Lee, L. E. Yu, S. Kim, S. C. Jeon, K. H. Kim, G. S. Lee, J. S. Oh, Y. C. Park, H. M. Lee, and Y. K. Choi, "Multiple-gate CMOS thin-film transistor with polysilicon nanowire," *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 102–105, Jan. 2008.

[4] C. M. Lee and B. Y. Tsui, "A high-performance 30-nm gate-all-around poly-Si nanowire thin-film transistor with NH_3 plasma treatment," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 683–685, Jul. 2010.

[5] T. K. Kang, T. C. Liao, C. M. Lin, H. W. Liu, F. H. Wang, and H. C. Cheng, "Gate-all-around poly-Si TFTs with single-crystal-like nanowire channels," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1239–1241, Sep. 2011.

[6] X. Duan, C. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles, and J. L. Goldman, "High-performance thin-film transistors using semiconductor nanowires and nanoribbons," *Nature*, vol. 425, no. 6955, pp. 274–278, Sep. 2003.

[7] H. Yin, W. Xianyu, A. Tikhonovsky, and Y. S. Park, "Scalable 3-D fin-like poly-Si TFT and its nonvolatile memory application," *IEEE Trans. Electron Devices*, vol. 55, no. 2, pp. 578–584, Feb. 2008.

[8] H. C. Lin, T. W. Liu, H. H. Hsu, C. D. Lin, and T. Y. Huang, "Tri-gated poly-Si nanowire SONOS devices for flat-panel applications," *IEEE Trans. Nanotechnol.*, vol. 9, no. 3, pp. 386–391, May 2010.

[9] C. C. Tsai, H. H. Chen, B. T. Chen, and H. C. Cheng, "High-performance self-aligned bottom-gate low-temperature poly-silicon thin-film transistors with excimer laser crystallization," *IEEE Electron Device Lett.*, vol. 28, no. 7, pp. 599–602, Jul. 2007.

[10] H. C. Lin, W. C. Chen, C. D. Lin, and T. Y. Huang, "Performance enhancement in double-gated poly-Si nanowire transistors with reduced nanowire channel thickness," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 644–646, Jun. 2009.