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Stress immunity enhancement of the SiN uniaxial strained *n*-channel metal–oxide–semiconductor field-effect-transistor by channel fluorine implantation

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ABSTRACT

Channel fluorine implantation (CFI) has been successfully integrated with silicon nitride contact etch stop layer (SiN CESL) to investigate electrical characteristics and stress reliabilities of the *n*-channel metal–oxide–semiconductor field-effect-transistor (*n*MOSFET) with HfO_2/SiON gate dielectric. Although fluorine incorporation had been used widely to improve device characteristics, however, nearly identical transconductance, subthreshold swing and drain current of the SiN CESL strained *n*MOSFET combining the CFI process clearly indicates that stress-induced electron mobility enhancement does not affect by the fluorine incorporation. On the other hand, the SiN CESL strained *n*MOSFET with fluorine incorporation obviously exhibits superior stress reliabilities due to stronger Si–F/Hf–F bonds formation. The channel hot electron stress and constant voltage stress induced threshold voltage shift can be significantly suppressed larger than 26% and 15%, respectively. The results clearly demonstrate that combining the SiN CESL strained *n*MOSFET with fluorinated gate dielectric using CFI process becomes a suitable technology to further enhance stress immunity.

1. Introduction

As complementary metal–oxide–semiconductor (CMOS) aggressive scaling, high drain current is essential for the high speed circuit operation, which requires high carrier mobility and large oxide capacitance. Therefore, strain technologies and high-permittivity (high-*k*) dielectrics have been successfully integrated with current CMOS technology, in order to increase the carrier mobility and the oxide capacitance, respectively. Hafnium oxide (HfO_2) is the most potential candidate owing to superior characteristics during investigation of the high-*k* dielectrics [1]. Unfortunately, bias temperature instability is another serious reliability issue of the metal–oxide–semiconductor field-effect-transistors (MOSFETs) with HfO_2 dielectric due to high defect densities [2]. High defect densities within the HfO_2 dielectric would increase scattering probability for the channel carriers and result in mobility degradation and drain current reduction [3,4].

Recently, various uniaxial strain technologies have been proposed to improve carrier mobility [5,6]. Silicon nitride contact etch stop layer (SiN CESL) is the simplest process to improve carrier mobility among these uniaxial strain technologies, however, large amount of hydrogen during SiN layer deposition would diffuse to the gate stacks to form Si–H/Hf–H bonds and degrade the channel hot electron reliability [7,8].

Although fluorine passivation technology has been widely used to replace weak Si–H bonds within the high-*k* gate stack to improve stress reliabilities [9–11], however, the impact of combining the fluorine passivation effect with the SiN CESL strained *n*-channel MOSFET (*n*MOSFET) is seldom investigated yet. Moreover, fluorine implantation is also used for work function engineering in metal gate/high-*k* dielectric stacks [12]. Fluorine incorporation using channel fluorine implantation (CFI) process prior to the SiN CESL strained *n*MOSFET fabrication can create Si–F passivated surface to suppress interfacial re-oxidation during the gate stack deposition, which is also beneficial for equivalent oxide thickness scaling [13]. Consequently, electrical characteristics and stress reliabilities of the SiN CESL uniaxial strained *n*MOSFET combining fluorinated HfO_2/SiON (oxynitride) gate stack using CFI process have been studied in this paper, which is expected to reduce threshold voltage (V_{TH}) shift during both constant voltage stress (CVS) and channel hot electron stress (CHES), while maintain high electron mobility simultaneously.

2. Experimental details

*n*MOSFETs were fabricated on 6-in. p-type (100) silicon wafer utilizing a conventional self-align process. Before 15 nm sacrificial oxide stripping, several samples were split to the CFI process at 10 keV with 1×10^{12} cm^{-2} dosage, followed by standard cleaning with a hydrofluoric acid-last process. Relatively low energy and light dosage is mainly to prevent significant channel damage and

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also to avoid eliminating the SiN CESL induced tensile strain in the channel. One nanometer interfacial SiON and 3.8 nm HfO_2 was formed by rapid thermal process at 800 °C in nitrous oxide (N_2O) ambient and metal organic chemical vapor deposition (CVD) at 500 °C in oxygen ambient, respectively, followed by annealing at 600 °C in nitrogen (N_2) ambient for 30 s. A 200 nm poly-Si gate was then deposited by the low-pressure CVD using silane (SiH_4) gas at 620 °C. After gate electrode patterning and subsequently dopant activation, 300 nm highly tensile strain SiN CESL and 100 nm TEOS passivation layer was deposited using the plasma-enhanced CVD at 300 °C with SiH_4 and ammonia (NH_3) or N_2O, respectively. Finally, contact hole etching and Al metallization were performed using standard CMOS process. Schematic cross-section of the SiN CESL strained *n*MOSFETs without and with fluorine incorporation using CFI process is shown in Fig. 1, where hydrogen passivation and fluorine passivation is indicated, respectively. Electrical properties and reliability characteristics of the SiN CESL strained *n*MOSFET with HfO_2/SiON gate stack were measured using the Hewlett-Packard (HP) 4156C semiconductor parameter analyzer. Furthermore, the binding energy of the hafnium and fluorine atom was extracted from the X-ray photoelectron spectrometer (XPS).

3. Results and discussion

Fig. 2 shows XPS spectra of the Hf_{4f} signal for the HfO_2/SiON gate stacks with and without CFI process. The binding energy was calibrated by the C_{1s} signal at 284.5 eV. The device with fluorinated gate stack obviously increases the binding energy larger than 0.5 eV for both $Hf_{4f5/2}$ and $Hf_{4f7/2}$ signal. Binding energy of the $Hf_{4f5/2}$ signal increases from 17.64 eV to 18.16 eV, while binding energy of the $Hf_{4f7/2}$ signal increases from 16.14 eV to 16.66 eV. Fluorine incorporation into HfO_2/SiON gate stack is further confirmed due to the conspicuous signal at ~685 eV, as shown in the inset, which means fluorine has been successfully bonded in HfO_2.

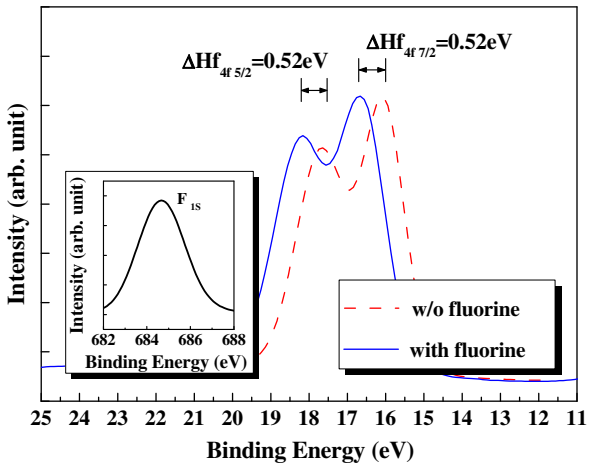

Fig. 2. XPS analysis of the Hf_{4f} electronic spectra for the gate stacks with and without fluorine incorporation. F_{1s} signal of the fluorinated gate stack using CFI process is also shown in the inset.

Fig. 3a presents the transfer curve of the SiN CESL strained *n*MOSFETs. Initial V_{TH} for the devices with and without fluorine incorporation is 1.03 and 1.02 V, respectively, which indicates that

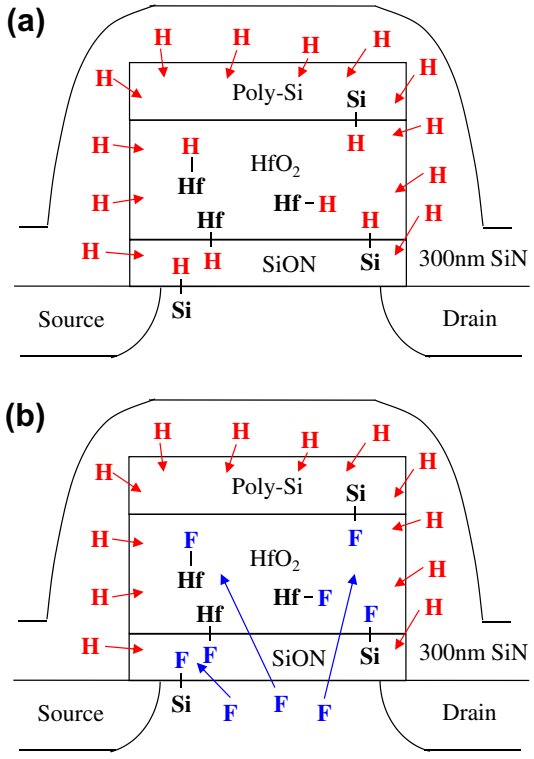

Fig. 1. Schematic cross-section of the SiN CESL strained *n*MOSFETs (a) without and (b) with fluorine incorporation.

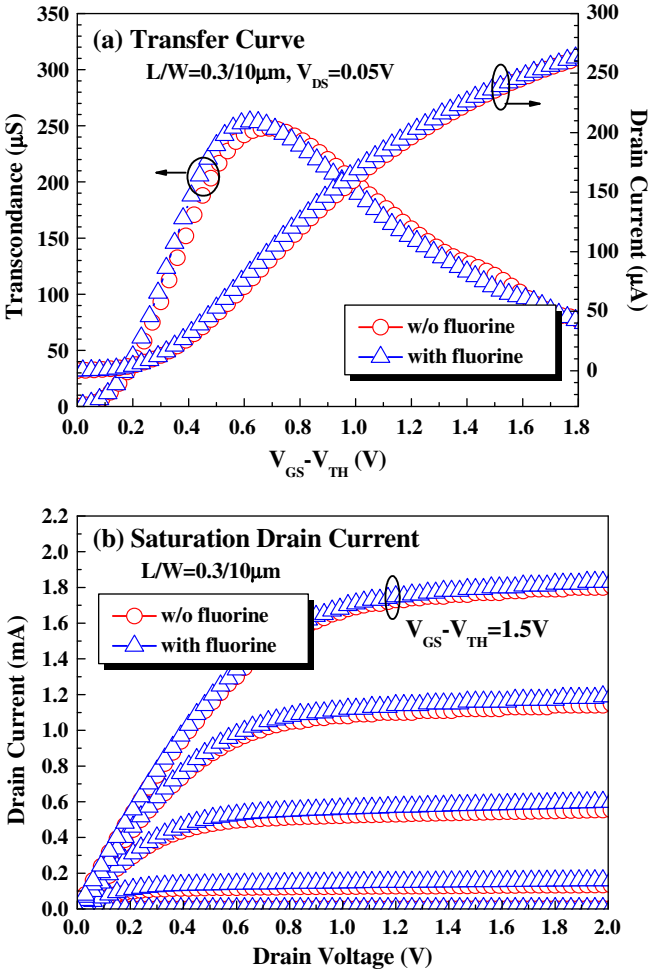

Fig. 3. (a) Transfer curve and (b) saturation drain current of the SiN CESL strained *n*MOSFETs with and without fluorine incorporation.

surface impurity concentration remains the same after fluorine implantation. With fluorine incorporation, maximum transconductance (G_m) and subthreshold swing (SS) has been slightly improved from 247.88 to 253.72 μS and from 97 to 96 mV/dec, respectively. Output characteristics of the SiN CESL strained *n*MOSFETs with and without fluorine incorporation are shown in Fig. 3b. With fluorine incorporation, saturation drain current (I_{DSsat}) has been slightly enhanced from 1.81 to 1.83 mA.

Nearly identical G_m, SS and I_{DSsat} of the SiN CESL strained *n*MOSFET with and without fluorine incorporation clearly indicates that improvement of electron mobility from the SiN CESL process does not affect by the CFI process. Moreover, negligible improvement of basic electrical characteristics by the CFI process also proves equivalent "as-fabricated" dielectric quality for the SiN CESL strained *n*MOSFETs with and without fluorine incorporation. For the device without fluorine incorporation, large amount of hydrogen during SiN layer deposition would diffuse to the gate stacks and the interface between gate stacks and Si substrate to form Hf–H and Si–H bonds, respectively, as shown in Fig. 1a. On the other hand, CFI process is applied prior to the SiN CESL deposition and fluorine exhibits much higher electronegativity than hydrogen (electronegativity of fluorine and hydrogen is 3.98 and 2.2, respectively [14]), it is hypothesized that negligible hydrogen-passivated bonds can be observed for the SiN CESL strained *n*MOSFET with fluorinated gate stack using CFI process. Consequently, most bulk and interfacial defects are passivated by the fluorine atoms, which create Hf–F and Si–F bonds in the fluorinated *n*MOSFET, respectively, as shown in Fig. 1b. As a result, as-fabricated dielectric quality can be improved either by Si–H/Hf–H bonds for the device without fluorine incorporation or by Si–F/Hf–F bonds for the device with fluorine incorporation, and therefore results in nearly identical electrical characteristics.

Fig. 4 compares the V_{TH} shift of the SiN CESL strained *n*MOSFETs with and without fluorine incorporation during channel hot electron stress (CHES) at maximum substrate current (I_{sub}). Substrate current during CHES is also shown in the inset. Incorporating fluorine results in nearly identical substrate current, which indicates both generated hot electron concentration and stressed gate voltage (V_{GS}) are also identical for the *n*MOSFETs with and without fluorine incorporation. On the other hand, the CHES degradation is not identical, the SiN CESL strained *n*MOSFET with fluorine incorporation obviously reduces V_{TH} shift larger than 26% after 1000 s CHES. CFI process prior to gate stacks fabrication is easily to create robust Si–F bonds near the interface, which has much stronger binding energy than Si–H bonds (binding energy of the Si–F bond (5.74 eV) is much higher than the Si–H bond (<3.11 eV) [15]). The SiN CESL strained *n*MOSFET with fluorine incorporation exhibits slightly faster V_{TH} shift saturation, which also demonstrates robust fluorine passivation effect. Moreover, fluorine-incorporated *n*MOSFET has higher critical energy to create interface traps during CHES [16]. Therefore, the SiN CESL strained *n*MOSFET with fluorinated gate stacks using CFI process is valuable to suppress the CHES-induced V_{TH} shift.

Fig. 5 shows the V_{TH} shift of the SiN CESL strained *n*MOSFETs with and without fluorine incorporation during constant voltage stress (CVS) at $V_{GS} - V_{TH} = 3$ V. The device with fluorine incorporation obviously reduces V_{TH} shift larger than 15% after 1000 s CVS. Stress-induced leakage current (SILC) degradation during CVS is also shown in the inset. Measured gate current gradually decreases during CVS for the *n*MOSFETs, which can be ascribed to the electron trapping. Since CVS-induced V_{TH} shift is mostly related with bulk traps rather than interface traps, combining the CFI process into the SiN CESL strained *n*MOSFET obviously enhances passivation of oxygen vacancies to form robust Hf–F bonds (6.75 eV), and suppresses electron trapping and V_{TH} shift [10,15]. As a result, combining the CFI process with the SiN CESL strained *n*MOSFET is demonstrated to reduce V_{TH} shift during both CVS and CHES, while maintain high electron mobility simultaneously. Measured electrical parameters and calculated improvement ratio of the SiN CESL strained *n*MOSFETs with and without fluorine incorporation are summarized in Table 1.

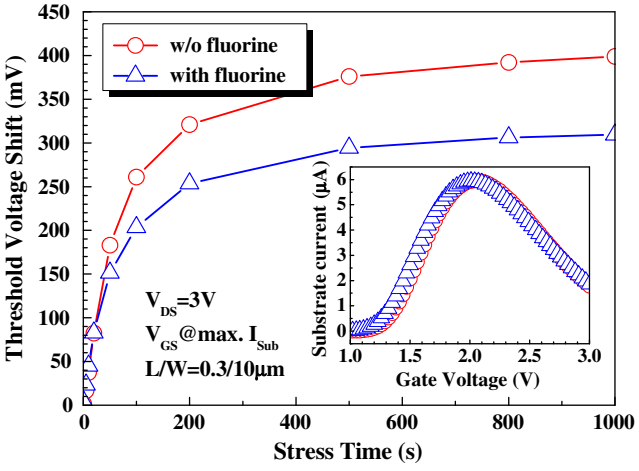

Fig. 4. CHES-induced V_{TH} shift of the SiN CESL strained *n*MOSFETs with and without fluorine incorporation. Substrate current is also shown in the inset.

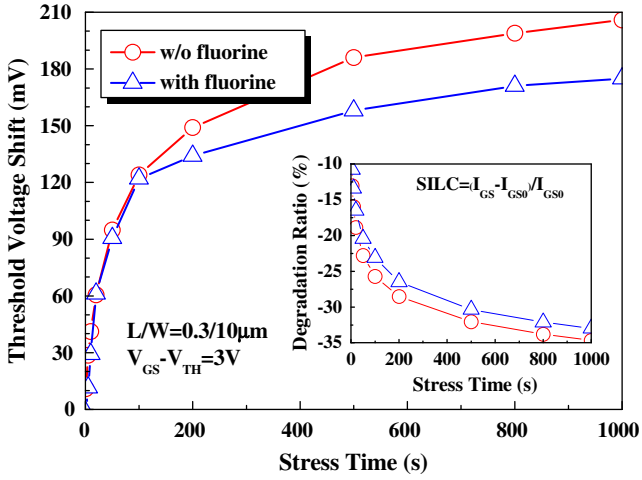

Fig. 5. CVS-induced V_{TH} shift of the SiN CESL strained *n*MOSFETs with and without fluorine incorporation. SILC characteristic is also shown in the inset.

Table 1
Measured electrical parameters and calculated improvement ratio of the SiN CESL strained *n*MOSFETs with and without fluorine incorporation.

	W/o fluorine	With fluorine	Improvement ratio (%)
Maximum G_m	247.88 μS	253.72 μS	2.36
Subthreshold swing	97 mV/dec	96 mV/dec	1.03
Saturation drain current ($V_{GS} - V_{TH} = 1.5$ V, $V_{DS} = 2$ V)	1.81 mA	1.83 mA	1.10
CHES-induced V_{TH} Shift ($V_{DS} = 3$ V, V_{GS} @ max. I_{sub} at 1000 s)	399 mV	294 mV	26.32
CVS-induced V_{TH} Shift ($V_{GS} - V_{TH} = 3$ V at 1000 s)	206 mV	175 mV	15.05

4. Conclusions

Although SiN CESL strained *n*MOSFET has been known to drastically improve the electron mobility and basic electrical characteristics due to high channel tensile strain, the results clearly conclude that further combining CFI process with the SiN CESL strained device exhibits negligible improvement on G_m, SS and $I_{DS\text{-}sat}$. Consequently, equivalent electron mobility and "as-fabricated" dielectric quality for the SiN CESL strained *n*MOSFETs with and without fluorine incorporation can be obtained by fluorine and hydrogen passivation, respectively. On the other hand, fluorine passivation by the CFI process is easily to form stronger Hf–F and Si–F bonds, which has superior stress immunity to against both CVS and CHES. Accordingly, CVS and CHES reliability characteristics for the SiN CESL strained *n*MOSFET can be further improved larger than 15% by the CFI process. Improved device reliabilities clearly indicate that SiN CESL uniaxial strained *n*MOSFET with fluorinated HfO_2/SiON gate stack using CFI process becomes a feasible technology for future CMOS applications.

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