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Study of intrinsic characteristics of ESD protection diodes for high-speed I/O applications

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ABSTRACT

To meet the desired electrostatic discharge (ESD) robustness, ESD diodes was added into the I/O cells of integrated circuits (ICs). However, the parasitic capacitance from the ESD diodes often caused degradation on circuit performance, especially in the high-speed I/O applications. In this work, two modified layout styles to effectively improve the figures of merits (FOMs) of ESD protection diodes have been proposed, which are called as multi-waffle and multi-waffle-hollow layout styles. Experimental results in a 90-nm CMOS process have confirmed that the FOMs ($R_{ON} * C_{ESD}$, I_{CP}/C_{ESD}, V_{HBM}/C_{ESD}, and I_{CP}/A_{Layout}) of ESD protection diodes with new proposed layout styles can be successfully improved.

1. Introduction

In order to effectively protect internal circuits and to minimize the parasitic effects of CMOS input/output (I/O) electrostatic discharge (ESD) protection circuits, the dual-diode ESD protection scheme with active power-rail ESD clamp has been widely adopted for effective on-chip ESD protection [1–3]. Therefore, the dual-diode circuit has been found adequate for protecting high-speed I/O circuits.

High-speed I/O circuits operating at gigahertz frequencies typically adopt "core" transistor with ultra-thin gate oxide. The ultra-thin gate oxide seriously degrades the ESD robustness of integrated circuits (ICs). Furthermore, thinner metal layer and shallower diffusion junction increase the resistance and local heat of the ESD protection devices [4]. These factors raise the difficulty of ESD protection design for ICs implemented in advanced CMOS technology [5,6]. In order to sustain the required ESD robustness, such as 2 kV in human body model (HBM) [7] and 200 V in machine model (MM) [8], the on-chip ESD protection devices must be drawn with large enough device dimension. However, this will increase the parasitic capacitance (C_{ESD}) at the I/O pads to obviously degrade the circuit performance, especially for radio-frequency (RF) front-end and high-speed I/O circuits [9,10]. Therefore, the C_{ESD} of the ESD protection devices must be minimized to reduce the circuit performance degradation but the ESD robustness is demanded to keep at the reasonable level [11]. For ESD protection devices, they must be optimized with consideration of C_{ESD} and ESD protection capability.

In order to minimize the C_{ESD} and to achieve satisfactory ESD robustness of the ESD protection devices at the I/O pads, the STI-bound N+/P_{sub} and P+/N_{well} ESD protection diodes fabricated in a 90-nm CMOS technology were investigated in this work. The evaluations of ESD protection diodes with stripe and waffle layout styles in previous works [12–14] are briefly reviewed. Two new modified layout styles are proposed to effectively improve the figures of merits (FOMs) of ESD protection diodes. The key design variables are the P–N junction dimensions and layout styles. Experimental results of the ESD protection diodes have confirmed that the new modified layout styles can successfully improve $R_{ON} * C_{ESD}$ and I_{CP}/C_{ESD} of the diodes. Compared to the prior arts, the diodes drawn with the new proposed layout styles are adequate for high-speed I/O applications.

2. ESD protection diodes

2.1. Figures of merits (FOMs) for comparison

Under normal circuit operation, the diode is turned off under the reverse-biased condition. Although the diode is turned off, there is still an intrinsic junction capacitance of the diode seen by the signals at the I/O pad. On the other hand, the diode should be turned on to discharge ESD current at forward-biased condition (cooperated with active power-rail ESD clamp) under ESD stresses. Therefore, the intrinsic junction capacitance of the diode at

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reverse-biased condition and the ESD protection capability of the diode at forward-biased condition are the important characteristics to investigate ESD diodes.

The current-handling ability of ESD protection device is usually indicated in terms of its second breakdown current I_{t2}. However, the measured I–V curve of the diode, as shown in Fig. 1, reveals that the ESD protection diode near the failure level I_{t2} may not function as an effective voltage clamp due to the series resistances of the diffusion regions [15]. When the current level approaches to I_{t2}, the increased on-resistance (R_{ON}) would result in local heating in the silicon or metal routing. Therefore, the maximum current-handling capability of the diode is suggested to be defined as the current level at which the measured I–V curve deviates from its linearly extrapolated value by 20% [12–14,16]. In this work, the current compression point is denoted as I_{CP}, which is used to represent the current-handling capability of the ESD protection diode.

Although the I_{CP} and R_{ON} of the ESD diode can be improved by increasing its device size, this would cause larger C_{ESD} and layout area of the ESD diode. Consequently, in order to determine the efficiency of the ESD diodes with different layout styles for high-speed I/O circuits, the FOMs of $R_{ON} * C_{ESD}$ and I_{CP}/C_{ESD} will be utilized. Moreover, the FOM of V_{HBM}/C_{ESD} can also be an alternative evaluation factor for the ESD diodes because the HBM levels (V_{HBM}) of the ESD protection diodes are reasonably relative to I_{CP}.

It should be noted that, for applications other than gigahertz frequency and high-speed I/O circuits, the C_{ESD} of the ESD diode may not be the major concern of the design. Instead, the ESD protection diode might be optimized based on different performance evaluation, such as layout area (A_{Layout}). Therefore, the FOM of I_{CP}/A_{Layout} presented in this work also gives another perspective factor on the tradeoffs between diode dimensions and layout styles.

2.2. Diffusion geometry of stripe and waffle diodes

Under forward-biased condition, the perimeter of the P–N junction in ESD diode primarily provides electrical conduction path [16]. It implies that the bottom plate of the P–N junction in ESD diode mainly contributes the C_{ESD}. Therefore, the FOMs, especially for I_{CP}/C_{ESD}, should be enhanced by maximizing the junction perimeter and minimizing the junction area.

The top view of the STI-bound N+/P_{sub} ESD diode with stripe layout style is shown in Fig. 2, which is the typical layout style often implemented in IC products. This typical stripe diode is realized by P+ stripe with both sides of the N+ stripe to give it with twice the electrical conduction path. Because the dimension D is much smaller than L, these two short sides of N+ stripe do little to improve electrical conduction. For the stripe diode, the ratio of junction perimeter to junction area for N+ strip diffusion region can be expressed as

$$\frac{\text{Junction Perimeter}}{\text{Junction Area}} = \frac{2 \cdot L}{D \cdot L} = \frac{2}{D}. \quad (1)$$

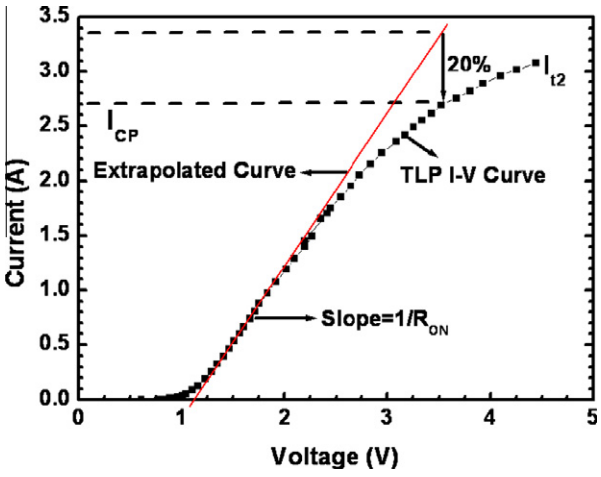

Fig. 1. The measured TLP I–V curve of the ESD protection diode. The current compression point (I_{CP}) is defined as the current level at which the measured I–V curve deviates from its linearly extrapolated value by 20%.

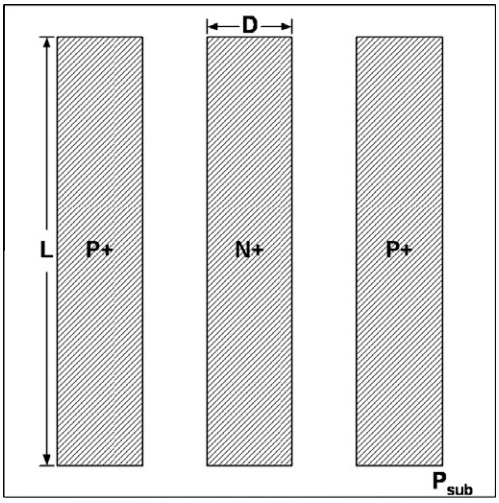

Fig. 2. STI-bound N+/P_{sub} ESD protection diode with typical stripe layout style. The major current conduction path of the stripe diode occurs along the length (L) of the diode.

Another STI-bound N+/P_{sub} ESD protection diode with waffle layout style is shown in Fig. 3a. The waffle diode has been studied in the previous works [17–19]. The N+ diffusion region is surrounded by a P+ diffusion region. In order to obtain different current-handling capability of the diode, multiple waffle diodes can be joined in parallel to form an array structure. A similar waffle structure can be implemented for P+/N_{well} diode, as shown in Fig. 3b. For the waffle diode, the ratio of junction perimeter to junction area can be expressed as

$$\frac{\text{Junction Perimeter}}{\text{Junction Area}} = \frac{4 \cdot D}{D \cdot D} = \frac{4}{D}, \quad (2)$$

which is twice as large as that for the stripe diode in (1). These evaluations imply that a waffle diode may potentially outperform a stripe diode.

In the previous works [12–14], the ESD protection diodes with the waffle layout style have been verified to achieve better FOMs than that of stripe diodes under careful size optimization. In addition, the diodes with waffle-hollow, octagon, and octagon-hollow layout styles have been proposed in the previous work [14] to further improve the FOMs of the waffle diode. Because the junction perimeter and the junction area of the octagon (octagon-hollow) diode are simultaneously smaller than those of the waffle (waffle-hollow) diode by 17%, the measured FOMs of the octagon (octagon-hollow) diode are only slightly better than those of the waffle (waffle-hollow) diode. However, the FOMs of the diodes with hollow layout style are significantly improved because the useless junction area is removed to reduce the parasitic capacitance. In this work, the new multi-waffle layout style based on waffle layout style is proposed. The multi-waffle diode with the increased junction perimeter and the reduced junction area is supposed to have better FOMs than that of waffle diode. Based on the

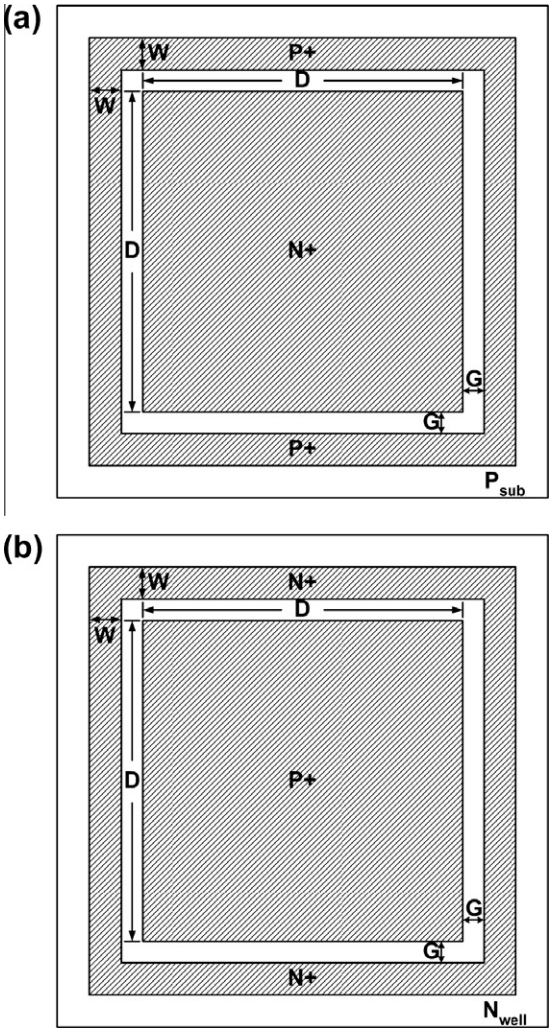

Fig. 3. Layout top view of the STI-bound (a) N+/P_{sub} ESD protection diode and (b) P+/N_{well} ESD protection diode with waffle layout style.

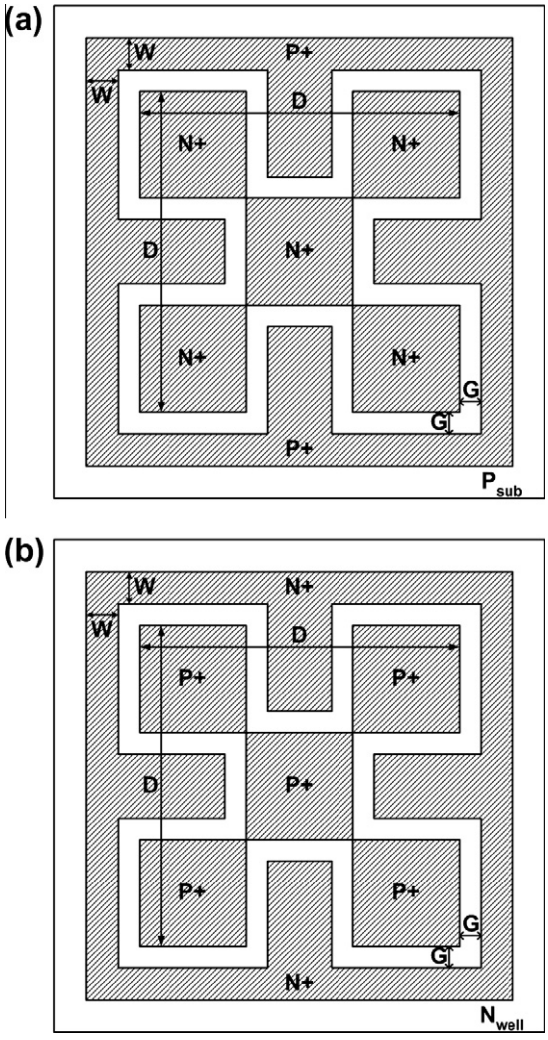

Fig. 4. Layout top view of the STI-bound (a) N+/P_{sub} ESD protection diode and (b) P+/N_{well} ESD protection diode with multi-waffle layout style.

same concept of hollow layout style in [14], the new multi-waffle-hollow layout style based on multi-waffle layout style is also proposed to further enhance the FOMs for high-speed I/O applications.

2.3. Diodes with multi-waffle and multi-waffle-hollow layout styles

The layout top view of the N+/P_{sub} [19] and P+/N_{well} ESD protection diodes with multi-waffle layout style are shown in Fig. 4a and b, respectively. The multi-waffle layout style is modified from waffle layout style. The P+(N+) diffusion region extends into the N+(P+) diffusion region from four sides for N+/P_{sub} (P+/N_{well}) diodes. The junction area can be theoretically reduced by a factor of 44%. Besides, the junction perimeter can also be increased by a factor of 67% at the same time. It implies that the ratio of junction perimeter to junction area for the multi-waffle diode can be given by

$$\frac{\text{Junction Perimeter}}{\text{Junction Area}} = \frac{5 \cdot (4 \cdot D/3)}{5 \cdot (D/3)^2} = \frac{12}{D}, \tag{3}$$

which is triple of that in (2). This suggests that the multi-waffle layout style can be another good method to reduce C_{ESD} of ESD diode for high-speed I/O applications.

It should be noted that the risk of damages located at the corner might be elevated because the corner number of multi-waffle diode is more than that of waffle diode. Moreover, the uniformity issue of discharging current would be emerged in real multi-waffle diode. However, the multi-waffle diode can still be supposed to have better FOMs than those of waffle diode due to great reduction of junction area and great raise of junction perimeter.

The other new modified layout style for ESD diode is illustrated in Fig. 5, which is called as the multi-waffle-hollow layout style. The multi-waffle-hollow layout style is modified from the multi-waffle layout style by removing the N+(P+) central diffusion region of N+/P_{sub} (P+/N_{well}) diodes. The purpose is to further reduce the junction area and to keep the junction perimeter at the same time. Generally, the C_{ESD} of the diode is proportional to the junction area and the ESD robustness is related to the junction perimeter. For instance, the cross-sectional view to explain ESD current flows in the N+/P_{sub} diodes with hollow and non-hollow layout styles are shown in Fig. 6a and b, respectively. For the non-hollow layout style shown in Fig. 6a, the ESD current could not be uniformly discharged through the whole N+ diffusion region because the current always tends to flow through the shortest path between two nodes. The ESD discharging current did not flow through the N+ central diffusion region, where still contributes C_{ESD} at normal circuit operation. To form the hollow layout style as shown in Fig. 6b, the N+ central diffusion region is removed to directly reduce the junction area of the diode. The ESD discharging current can be effectively concentrated in the remaining N+ diffusion region of the diode. Therefore, the ratio of junction perimeter to junction

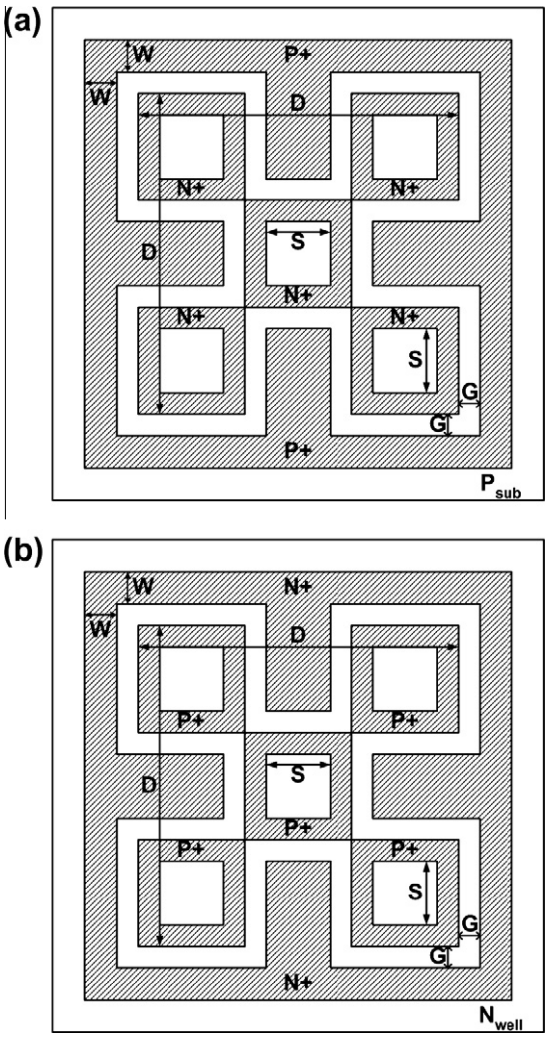

Fig. 5. Layout top view of the STI-bound (a) N+/P_{sub} ESD protection diode and (b) P+/N_{well} ESD protection diode with multi-waffle-hollow layout style. The N+(P+) center diffusion region of N+/P_{sub} (P+/N_{well}) diode with multi-waffle-hollow layout style is removed to reduce the parasitic capacitance.

area for the multi-waffle-hollow diode can be theoretically expressed by

$$\frac{\text{Junction Perimeter}}{\text{Junction Area}} = \frac{5\cdot(4\cdot D/3)}{5\cdot(D/3)^2 - 5\cdot(S)^2} = \frac{12}{D - \frac{(3\cdot S)^2}{D}}, \quad (4)$$

where the junction perimeter is assumed to be the same as that of multi-waffle layout style. The ratio in (4) is always larger than that in (3) for multi-waffle diode. Therefore, the multi-waffle-hollow diode can be expected to further reduce the C_{ESD} and to keep the ESD robustness at the same time.

In this work, the ESD diodes with multi-waffle and multi-waffle-hollow layout styles are drawn and fabricated in a 90-nm CMOS process to investigate their corresponding FOMs. The major layout parameters of those N+/P_{sub} and P+/N_{well} diodes are listed in Table 1, where the different spacings are also marked in Figs. 3–5.

2.4. Interconnect routing of the diodes

To effectively reduce the impact from the parasitic resistance and capacitance of the interconnect routing in the layout of ESD diodes, the arrangement of metal lines to connect the ESD diodes should be considered with the de-embedding calculation. The 3D

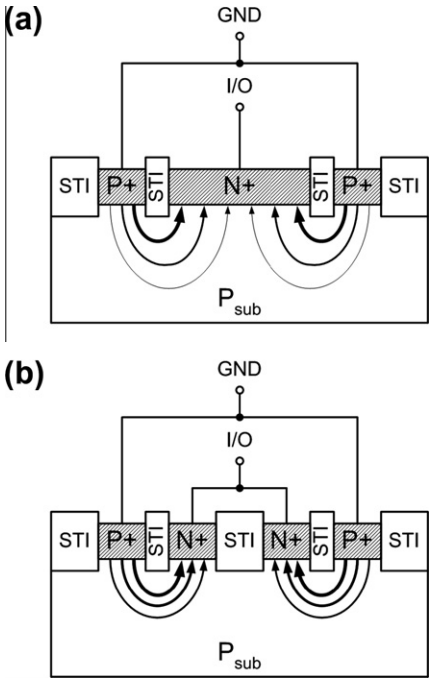

Fig. 6. Device cross-sectional view to explain ESD current flows in the N+/P_{sub} diodes with (a) non-hollow and (b) hollow layout styles.

layout diagram of interconnect routing of the N+/P_{sub} diode is shown in Fig. 7a. The width of metal line from the diode to the bond pad is drawn as large as possible to reduce the parasitic resistance of interconnect routing. With the large width of metal line, the parasitic resistance of interconnect routing (that can be estimated manually with the sheet resistance provided by foundry) can be quite smaller than the on-resistance R_{ON} of the ESD diodes.

About the parasitic capacitance of interconnect routing, the 3D layout diagram of the open pad structure for de-embedding calculation is shown in Fig. 7b. All metal layers are remained except the diodes. With the measured *S*-parameters of the open pad structure, the parasitic capacitance of interconnect routing can be de-embedded to obtain the pure junction capacitance of the ESD diodes.

The different metal routing approaches [12,13] were not discussed in this work because the diodes with waffle, multi-waffle, and multi-waffle-hollow layout styles are totally symmetric. To diminish the parasitic effects of interconnect routing is emphasized in this work to obtain the pure characteristics of the diodes.

2.5. Performance evaluations

Before implementing the diodes, there is a useful evaluation to imply the goodness of ESD diodes. This important evaluation is the ratio of (junction perimeter)/(junction area), which has been calculated in (1)–(4) for different layout styles. Undoubtedly, the high evaluation value suggests that the ESD diodes can sustain high ESD robustness with low C_{ESD} to minimize the degradation of circuit performance for high-speed I/O applications. The evaluation values for the diodes investigated in this work are listed in Table 1 and illustrated in Fig. 8. According to the theoretical calculations, the diode in small size obviously has larger evaluation value at the given layout style. It can also be noted that the diodes in large size with the two new modified layout styles can achieve comparable level to that of small-size diodes with waffle layout style. This result reveals that not to continuously shrink the diode size but to implement the diode with new modified layout styles can be a

Table 1
The device characteristics and previous evaluation items of diodes with different layout styles.

Layout style	Size	Dimensions of device (μm)	Array	Junction perimeter (μm)	Junction area (μm^2)	Layout area, A_{Layout} (μm^2)	Junction perimeter/junction area
Waffle	A	W = 0.22, D = 0.56, G = 0.34	5 × 1	11.2	1.57	14.11	7.13
	B	W = 0.22, D = 1.12, G = 0.34	5 × 1	22.4	6.27	25.09	3.57
	C	W = 0.22, D = 3.36, G = 0.34	5 × 1	67.2	56.45	100.35	1.19
	D	W = 0.22, D = 4.20, G = 0.34	5 × 1	84.0	88.20	141.51	0.95
	E	W = 0.22, D = 5.04, G = 0.34	5 × 1	100.8	127.01	189.73	0.79
Multi-waffle	C	W = 0.22, D = 3.36, G = 0.34	5 × 1	112.0	31.36	100.35	3.57
	D	W = 0.22, D = 4.20, G = 0.34	5 × 1	140.0	49.00	141.51	2.86
	E	W = 0.22, D = 5.04, G = 0.34	5 × 1	168.0	70.56	189.73	2.38
Multi-waffle-hollow	C	W = 0.22, D = 3.36, S = 0.34, G = 0.34	5 × 1	112.0	28.47	100.35	3.93
	D	W = 0.22, D = 4.20, S = 0.62, G = 0.34	5 × 1	140.0	39.39	141.51	3.55
	E	W = 0.22, D = 5.04, S = 0.90, G = 0.34	5 × 1	168.0	50.31	189.73	3.34

good choice for avoiding the penalty, such as parasitic sidewall capacitance from the junction perimeter and local heat distribution [12,13].

3. Experimental results

The testchips of STI-bound N+/P_{sub} and P+/N_{well} diodes with the original waffle and two new modified layout styles have been fabricated in a 90-nm CMOS process. These diodes are prepared with the consideration of two-port *S*-parameter measurement, transmission line pulsing (TLP) system measurement, and HBM ESD robustness measurement. In this work, each diode structure was tested four times from four separated dice.

3.1. Parasitic capacitance

The diodes are arranged with ground–signal–ground (G–S–G) pads to facilitate on-wafer two-port *S*-parameter measurement. During the *S*-parameter measurement, the N+(P+) and P+(N+) diffusion regions of the N+/P_{sub} (P+/N_{well}) diodes are connected to port 1 and port 2, respectively, which are both biased at 0 V.

In order to extract the high-frequency characteristics of the intrinsic device, the parasitic effects of the bond pad and interconnect routing must be de-embedded. The diagrams of test structures, one including the device under test (DUT) and the other excluding the DUT (open pad structure), as shown in Fig. 9a and b, were implemented in the same testchip. The Y_{11}-parameter can be obtained from the measured two-port *S*-parameters by

$$Y_{11} = \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{Z_0((1 + S_{11})(1 + S_{22}) - S_{12}S_{21})}, \quad (5)$$

where Z_0 is the termination resistance of 50 Ω [20]. The measured *Y*-parameter of the including-DUT pattern is labeled as $Y_{11\text{-meas}}$, and the measured *Y*-parameter of the excluding-DUT pattern (open pad structure) is labeled as $Y_{11\text{-open}}$. The intrinsic device characteristics, $Y_{11\text{-DUT}}$, can be obtained by subtracting $Y_{11\text{-open}}$ from $Y_{11\text{-meas}}$. The parasitic capacitance (C_{ESD}) of each diode can be extracted from the *Y*-parameter of the intrinsic device by

$$C_{ESD} = \frac{\mathrm{Im}(Y_{11-DUT})}{2\pi f}, \quad (6)$$

where *f* is the operating frequency. The extracted C_{ESD} of the fabricated N+/P_{sub} (P+/N_{well}) diodes from 4 to 5 GHz under zero DC bias are listed in Tables 2 and 3 and compared in Fig. 10.

From the measured results of the diodes with waffle, multi-waffle, and multi-waffle-hollow layout styles, the extracted parasitic capacitances of the diodes in large dimension are practically proportional to the junction area. It can be observed that the extracted parasitic capacitances of waffle diodes in small size are higher than expected values due to parasitic sidewall capacitances. When the diodes are modified from waffle to multi-waffle and multi-waffle-hollow layout styles, the junction area is purposely decreased and the junction perimeter is increased. The contribution of parasitic sidewall capacitance induced by increased junction perimeter would be gradually emerged. Therefore, the measured C_{ESD} trend lines of the multi-waffle and multi-waffle-hollow diodes in Fig. 10a and b are a little higher than that of waffle diode. Besides, it can be also observed that the measured C_{ESD} of multi-waffle-hollow diode in size C is slightly larger than that of multi-waffle diode in size C due to the effect of parasitic sidewall capacitance. Compared to the N+/P_{sub} (P+/N_{well}) waffle diodes in size C ∼ size E, the C_{ESD} can be reduced 33%, 34%, and 36% (44%, 38%, and 37%) for the N+/P_{sub} (P+/N_{well}) multi-waffle diodes, respectively. Similarly, they can be reduced 32%, 39%, and 46% (43%, 46%, and 47%) for the N+/P_{sub} (P+/N_{well}) multi-waffle-hollow

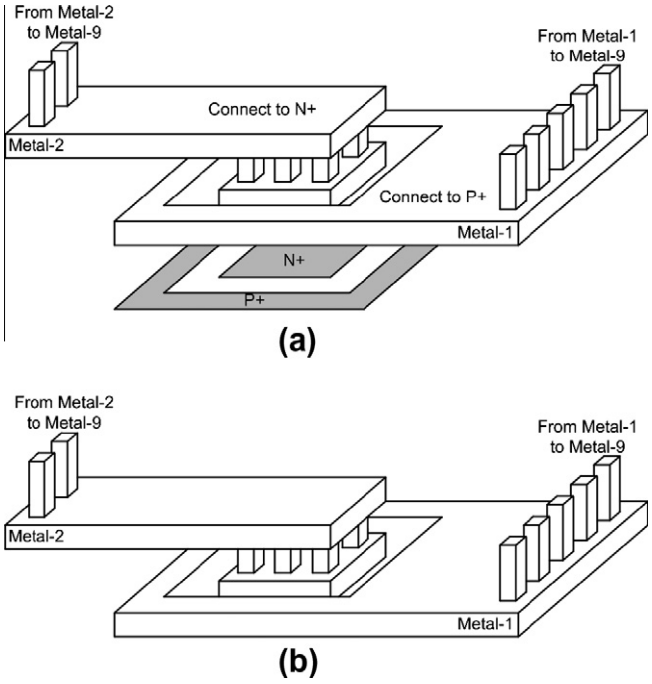

Fig. 7. The 3D views of metal layer arrangement for (a) interconnect routing of N+/P_{sub} diodes and (b) the corresponding open pad structure.

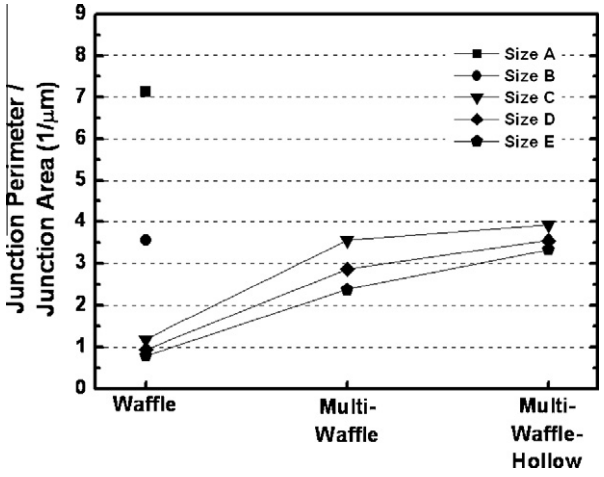

Fig. 8. The performance evaluations with the ratio of (junction perimeter)/(junction area) under different layout styles.

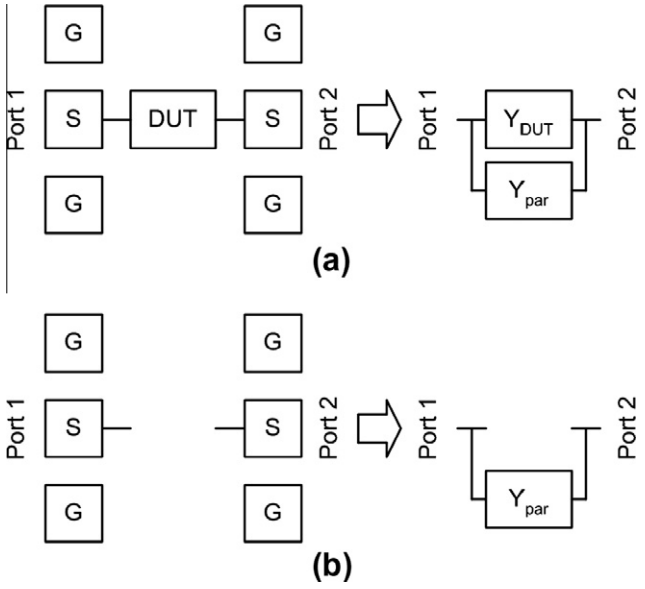

Fig. 9. Layout top views for de-embedded calculation to extract the parasitic capacitance of the fabricated ESD diodes with (a) including-DUT pattern and (b) excluding-DUT pattern.

diodes. These great reductions of C_{ESD} are the major factors to significantly improve the FOMs of the diodes with new modified layout styles.

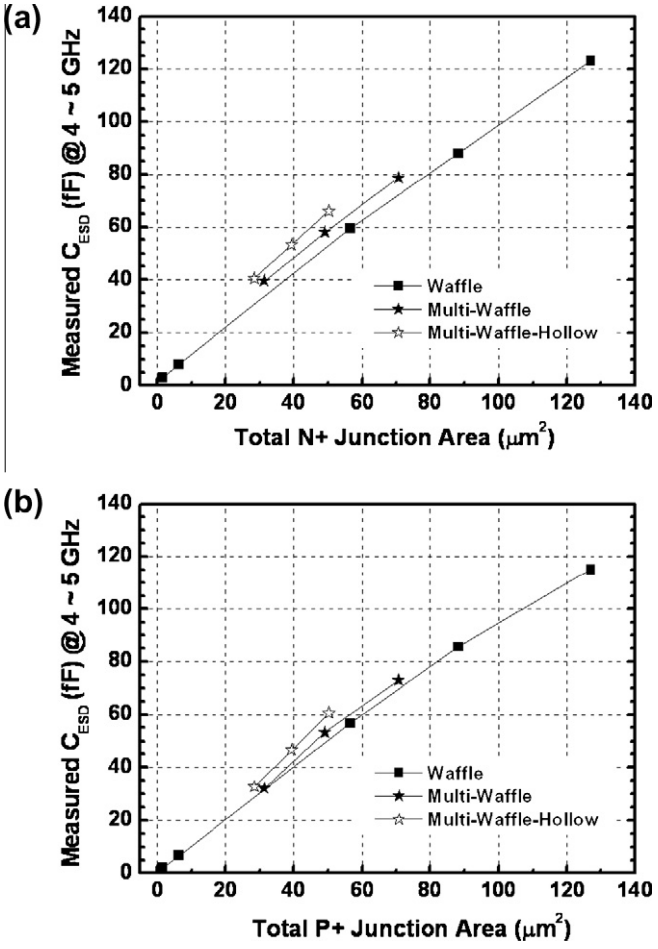

Fig. 10. Dependence of measured C_{ESD} extracted from *S*-parameter from 4 to 5 GHz under zero DC bias on the (a) total N + junction area of N+/P_{sub} diodes and (b) total P + junction area of P+/N_{well} diodes with different layout styles.

3.2. Transmission line pulsing (TLP) measurement

In order to investigate the device behavior during high ESD current stress, transmission line pulsing (TLP) generator with a pulse width of 100 ns and a rise time of ~2 ns is utilized [21]. The on-resistance (R_{ON}) and current compression point (I_{CP}) of the fabricated STI-bound diodes under forward-biased condition were characterized by the TLP system. The current level I_{CP} is utilized for comparison. By using TLP system, the R_{ON} and I_{CP} of the N+/P_{sub} and P+/N_{well} diodes under forward-biased condition are extracted and listed in Tables 2 and 3, respectively. The R_{ON} versus the

Table 2
The measured results averaged from four separated dice and figures-of-merit of N+/Psub diodes with different layout styles.

Layout style	Size	C_{ESD} (fF)	I_{CP} (A)	R_{ON} (Ω)	I_{t2} (A)	V_{HBM} (kV)	$R_{ON} * C_{ESD}$ (Ω-fF)	I_{CP}/C_{ESD} (mA/fF)	V_{HBM}/C_{ESD} (V/fF)	I_{CP}/A_{Layout} (mA/μm²)
Waffle	A	2.84	0.158	10.148	0.178	0.3	28.82	55.63	105.63	11.20
	B	8.01	0.416	3.980	0.476	0.8	31.88	51.94	99.88	16.58
	C	59.44	2.100	0.871	2.361	3.8	51.77	35.33	63.93	20.93
	D	88.00	2.777	0.738	2.890	4.8	64.94	31.56	54.55	19.62
	E	123.09	3.328	0.694	3.536	5.5	85.42	27.04	44.68	17.54
Multi-waffle	C	39.56	1.862	0.819	2.252	3.7	32.40	47.07	93.53	18.56
	D	58.02	2.722	0.699	3.096	5.1	40.56	46.91	87.90	19.24
	E	78.76	3.561	0.601	3.902	6.5	47.33	45.21	82.53	18.77
Multi-waffle-hollow	C	40.51	1.790	0.821	2.229	3.6	33.26	44.19	88.87	17.84
	D	53.31	2.531	0.709	3.017	5.0	37.80	47.48	93.79	17.89
	E	66.03	3.258	0.620	3.752	6.2	40.94	49.34	93.90	17.17

Table 3
The measured results averaged from four separated dice and figures-of-merit of P+/Nwell diodes with different layout styles.

Layout style	Size	C_{ESD} (fF)	I_{CP} (A)	R_{ON} (Ω)	I_{t2} (A)	V_{HBM} (kV)	$R_{ON} * C_{ESD}$ (Ω-fF)	I_{CP}/C_{ESD} (mA/fF)	V_{HBM}/C_{ESD} (V/fF)	I_{CP}/A_{Layout} (mA/μm^2)
Waffle	A	2.01	0.184	9.766	0.195	0.3	19.63	91.54	149.25	13.04
	B	6.75	0.475	3.844	0.514	0.9	25.95	70.37	133.33	18.93
	C	56.71	2.059	0.862	2.285	3.7	48.88	36.31	65.24	20.52
	D	85.73	2.368	0.734	2.724	4.6	62.93	27.62	53.66	16.73
	E	115.11	2.683	0.700	3.134	5.4	80.58	23.31	46.91	14.14
Multi-waffle	C	32.00	2.083	0.790	2.414	4.4	25.28	65.09	137.50	20.76
	D	53.32	2.835	0.669	3.291	5.6	35.67	53.17	105.03	20.03
	E	73.02	3.512	0.592	3.745	6.9	43.23	48.10	94.49	18.51
Multi-waffle-hollow	C	32.59	2.053	0.769	2.259	4.4	25.06	62.99	135.01	20.46
	D	46.68	2.773	0.667	3.288	5.6	31.14	59.40	119.97	19.60
	E	60.56	3.364	0.594	3.688	6.8	35.97	55.55	112.29	17.73

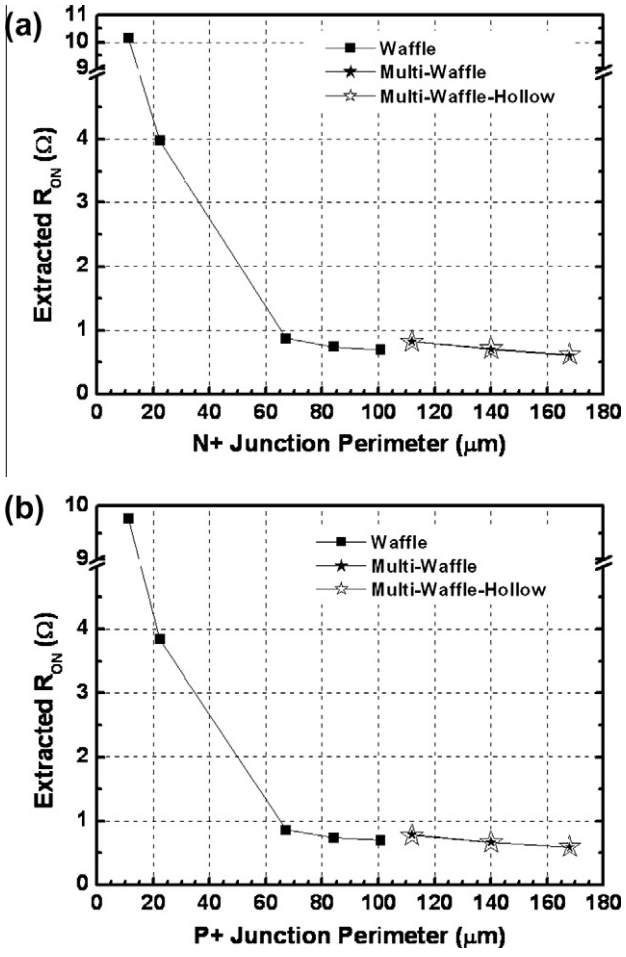

Fig. 11. Dependence of extracted on-resistance R_{ON} on the (a) N+ junction perimeter of N+/P_{sub} diodes and (b) P+ junction perimeter of P+/N_{well} diodes with different layout styles.

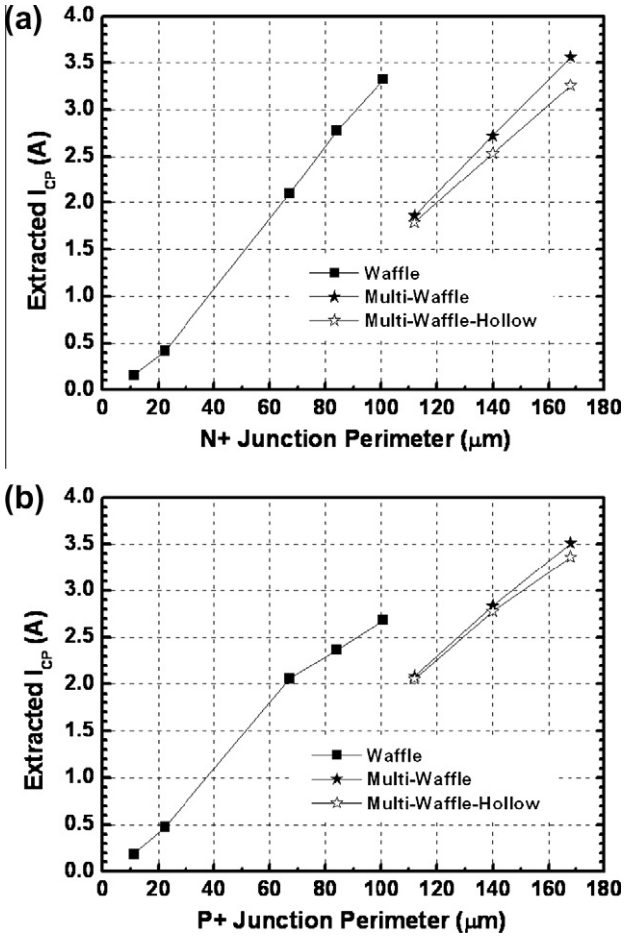

Fig. 12. Dependence of extracted current compression point I_{CP} on the (a) N+ junction perimeter of N+/P_{sub} diodes and (b) P+ junction perimeter of P+/N_{well} diodes with different layout styles.

junction perimeter of the N+/P_{sub} and P+/N_{well} diodes with different layout styles are illustrated in Fig. 11a and b, respectively. Apparently, the R_{ON} is decreased with the increased junction perimeter.

The I_{CP} versus the junction perimeter of the N+/P_{sub} and P+/N_{well} diodes with different layout styles are illustrated in Fig. 12a and b, respectively. The junction perimeter of multi-waffle diode is purposely increased 67% to be larger than that of waffle diode. But the I_{CP} is not increased as much as the theoretical expectation when the diode is modified from waffle to multi-waffle layout style. This is caused by non-uniformity of the ESD discharging current. Besides, the increased corners of multi-waffle diode also increase the risk of damages at the corners. However, the C_{ESD} can be greatly reduced by removing the N+(P+) diffusion region of the N+/P_{sub} (P+/N_{well}) diode. Consequently, the FOMs can still be expected to be further improved by modifying the diode from waffle to multi-waffle and multi-waffle-hollow layout styles.

The line current densities, which are the ratio of I_{CP} to junction perimeter, of multi-waffle and multi-waffle-hollow diodes are calculated in Table 4. The reduction percentages of line current density from multi-waffle to multi-waffle-hollow layout style are

Table 4
The line current density of diode devices.

Layout Style	From multi-waffle to multi-waffle-hollow											
Diode	$N+/P_{sub}$						$P+/N_{well}$					
Size	C	C	D	D	E	E	C	C	D	D	E	E
I_{CP} (A)	1.862	1.790	2.722	2.531	3.561	3.258	2.083	2.053	2.835	2.773	3.512	3.364
Junction perimeter (μm)	112.0	112.0	140.0	140.0	168.0	168.0	112.0	112.0	140.0	140.0	168.0	168.0
Line current density (mA/μm)	16.63	15.98	19.44	18.08	21.20	19.39	18.60	18.33	20.25	19.81	20.90	20.02
Reduction percentage of line current density (%)	3.91		7.00		8.54		1.45		2.17		4.21	

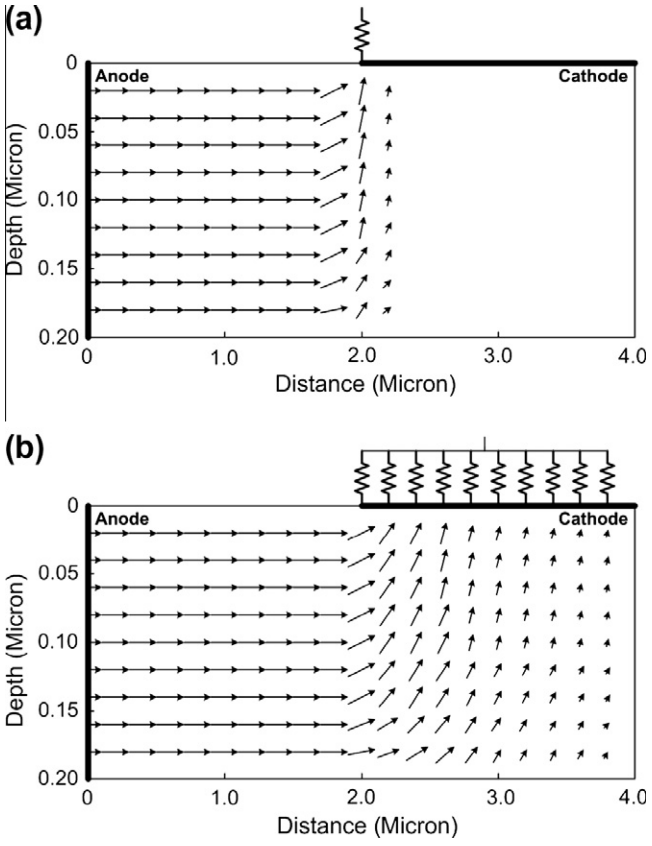

Fig. 13. The simulated vectors of ESD discharging current along the cross section of $N+/P_{sub}$ diodes in (a) small and (b) large device sizes.

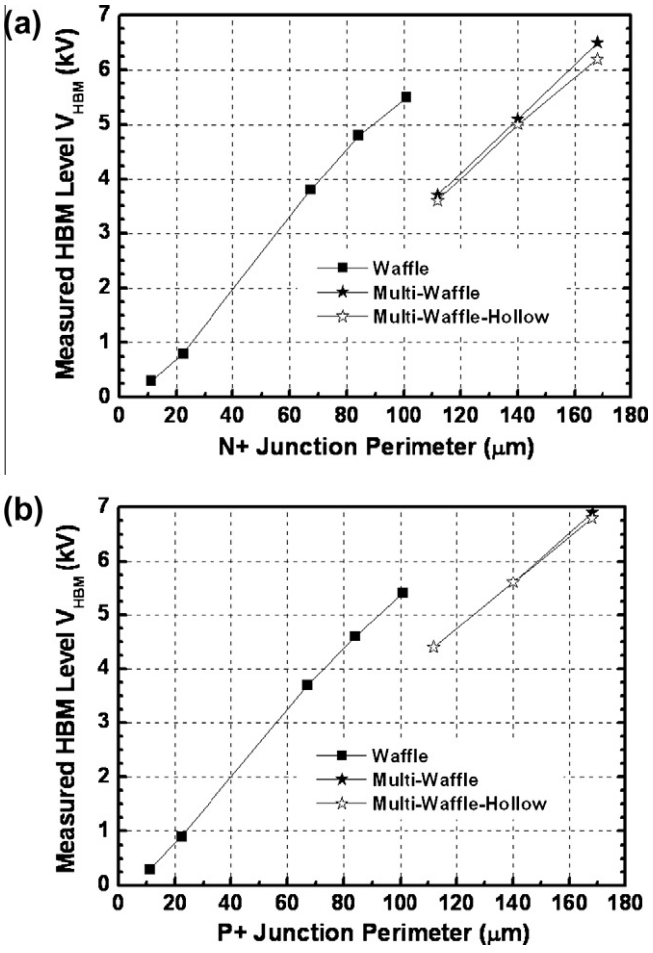

Fig. 14. Dependence of measured HBM level V_{HBM} on the (a) N+ junction perimeter of $N+/P_{sub}$ diodes and (b) P+ junction perimeter of $P+/N_{well}$ diodes with different layout styles.

also calculated in Table 4. When the diode is modified from multi-waffle to multi-waffle-hollow layout style, the reduction on I_{CP} of the diode in large device size is greater than that of the diode in small device size. This implies that the ESD discharging current of multi-waffle diode in large device size would flow more deeply through the central diffusion region because the multi-waffle diode in large device size has more contacts at diffusion region to cause a small equivalent resistance at cathode.

With more detailed illustration, the simulations can give a clear explanation. Fig. 13a and b are the current vector plots of the $N+/P_{sub}$ diode in small size and large size, respectively. For convenience, the anode is set along the entire edge of the diode and the cathode is set along the right half of the top surface of the diode. When the diode is drawn in small size, the fewer contacts at N+ diffusion region make the current crowded into the nearest corner of the electrode. On the contrary, there are more contacts at N+ diffusion region for the diode drawn in large size as shown in Fig. 13b. The current crowding behavior experienced in Fig. 13a can be diminished and the current can be distributed through the entire electrode more widely. Based on the simulation results and the calculations of line current density in Table 4, the ESD discharging current through the diode in large size is expected to flow more deeply through the central diffusion region. Therefore, the diode in large device size has larger reduction of I_{CP} when the diode is modified from multi-waffle to multi-waffle-hollow layout style.

3.3. ESD robustness

The human body model (HBM) ESD robustness of the ESD diode is measured by KeyTek ZapMaster with the test method standard [22]. The ESD diodes are tested from 0.1 kV to 8 kV with the step

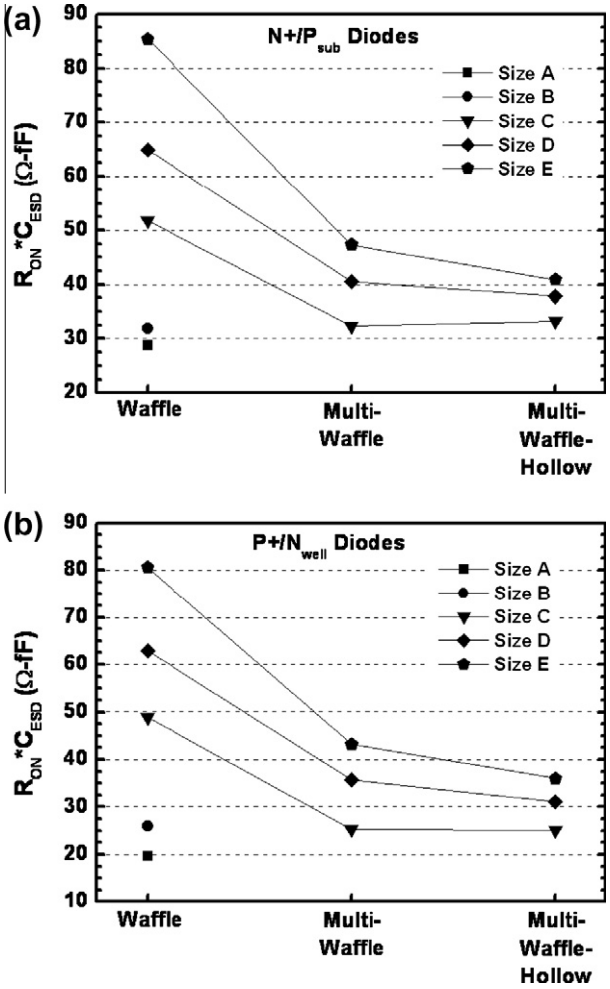

Fig. 15. The exact values of $R_{ON} * C_{ESD}$ of the (a) N+/P_{sub} diodes and (b) P+/N_{well} diodes with different layout styles.

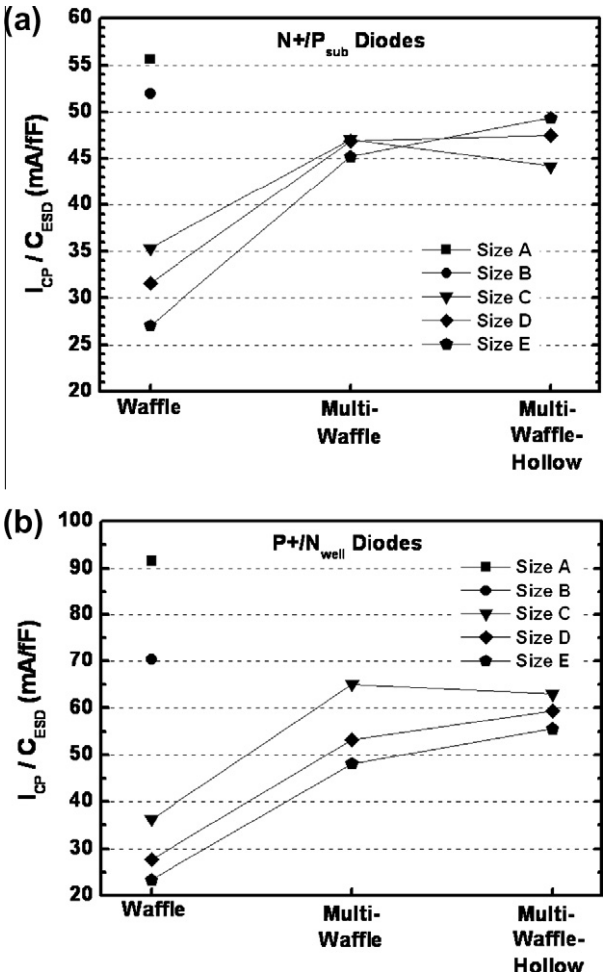

Fig. 16. The exact values of I_{CP}/C_{ESD} of the (a) N+/P_{sub} diodes and (b) P+/N_{well} diodes with different layout styles.

0.1 kV under forward-biased condition and the results are also listed in Tables 2 and 3. The V_{HBM} versus the N+(P+) junction perimeter of the N+/P_{sub} (P+/N_{well}) diodes with different layout styles are shown in Fig. 14. The trend in Fig. 14 is quite similar to Fig. 12.

3.4. FOM comparison and discussion

The FOMs ($R_{ON} * C_{ESD}$, I_{CP}/C_{ESD}, V_{HBM}/C_{ESD}, and I_{CP}/A_{Layout}) of the ESD diodes in a 90-nm CMOS technology are listed in Tables 2 and 3. According to TLP *I–V* measured results in Fig. 11, R_{ON} can be reduced by increasing the junction perimeter, but the junction area of the ESD diodes would be increased simultaneously. The R_{ON} of the ESD diode is expected to be small to effectively clamp the voltage. The C_{ESD} is also highly demanded to be small to minimize the degradation of circuit performance. Therefore, the $R_{ON} * C_{ESD}$ is a useful justification to the ESD diodes. The exact values of $R_{ON} * C_{ESD}$ of the N+/P_{sub} and P+/N_{well} diodes with different layout styles are illustrated in Fig. 15a and b. In Fig. 15, the $R_{ON} * C_{ESD}$ values of the diodes with new modified layout styles in size C can be comparable to that of waffle diodes in small size.

The most important FOM of I_{CP}/C_{ESD} should be expected to be high to sufficiently sustain the ESD stresses. The exact values of I_{CP}/C_{ESD} of the N+/P_{sub} and P+/N_{well} diodes with different layout styles are shown in Fig. 16a and b. For the waffle diodes in size A and size B, the I_{CP}/C_{ESD} values are not improved as high as that of theoretical expectation. The main reason is that the effects of parasitic sidewall capacitance and the local heat dissipation are getting serious when the dimension of the diode is shrunk. However, the I_{CP}/C_{ESD} values of the diodes at given size can be greatly improved from the waffle to the new modified layout styles in order to avoid the penalty when continuously shrinking the diode size. Moreover, the trend of V_{HBM}/C_{ESD} illustrated in Fig. 17 is quite similar to that in Fig. 16 because the HBM ESD level is highly related to I_{t2}. Taking the multi-waffle diode in size C and waffle diode in size A for comparison, the I_{CP}/C_{ESD} and the V_{HBM}/C_{ESD} values of multi-waffle N+/P_{sub} (P+/N_{well}) diode are only smaller than those of waffle diode about 15% and 11% (29% and 8%), respectively. Overall, I_{CP}/C_{ESD} and V_{HBM}/C_{ESD} values of P+/N_{well} diodes are better than those of N+/P_{sub} diodes. It was found that the P+/N_{well} diodes have both a higher I_{CP} and a lower C_{ESD} than their N+/P_{sub} diode counterparts. The higher I_{CP} may be caused by the turn-on parasitic vertical PNP bipolar transistor [12]. The lower parasitic capacitance is most likely due to the different N_{well} and P_{sub} doping concentrations. Besides, $R_{ON} * C_{ESD}$ values of P+/N_{well} diodes are also slightly lower than those of N+/P_{sub} diodes due to the smaller C_{ESD}.

Another design concern for the circuit applications is layout area (A_{Layout}). In advanced CMOS technology, the fabrication cost per die area is getting higher and higher. Therefore, the biggest concern of some ESD designers might be to save the layout area of the protection circuit but to sustain required ESD robustness.

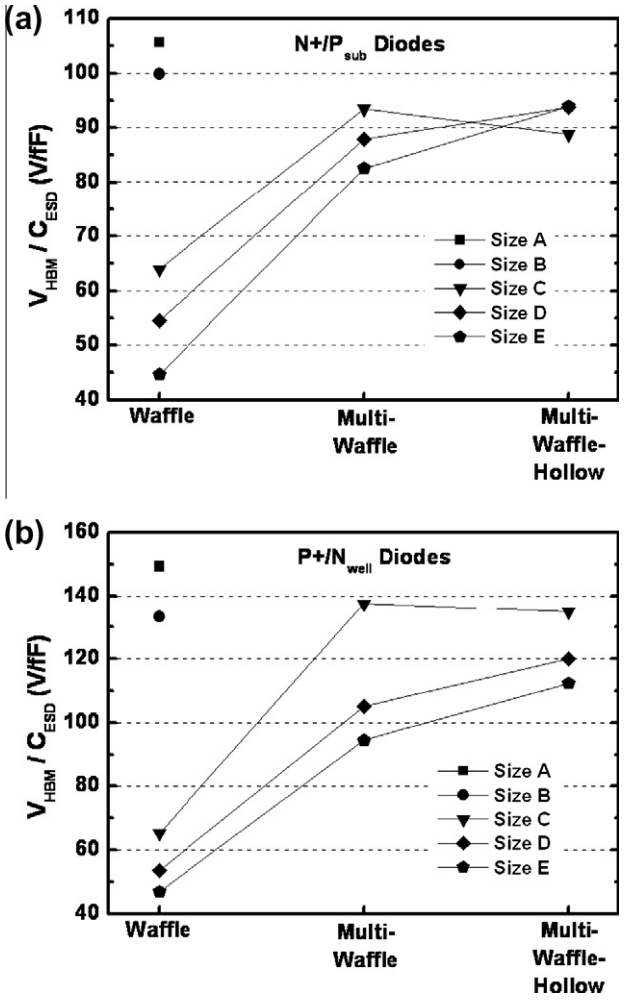

Fig. 17. The FOM V_{HBM}/C_{ESD} of the (a) N+/P_{sub} diodes and (b) P+/N_{well} diodes with different layout styles.

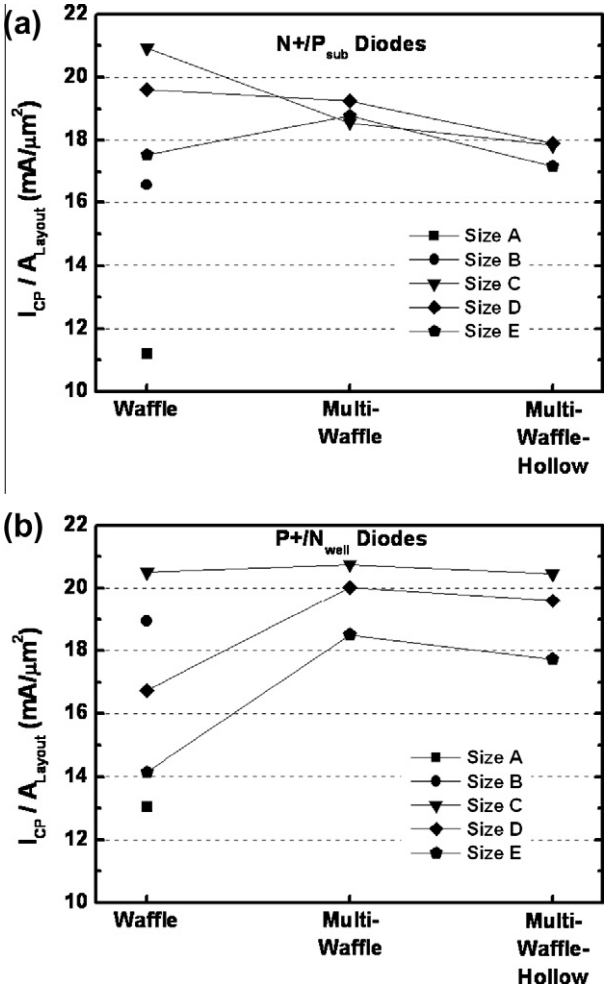

Fig. 18. The FOM I_{CP}/A_{Layout} of the (a) N+/P_{sub} diodes and (b) P+/N_{well} diodes with different layout styles.

The values of I_{CP}/A_{Layout} of the N+/P_{sub} and P+/N_{well} diodes with different layout styles are shown in Fig. 18a and b, respectively. The value of I_{CP}/A_{Layout} is supposed to be large to meet the requirements of layout area efficiency for a given ESD robustness. For the diodes with new modified layout styles, the values of I_{CP}/A_{Layout} are within the range from 17 to 19 mA/μm^2 for N+/P_{sub} diodes and 18–21 mA/μm^2 for P+/N_{well} diodes. The I_{CP}/A_{Layout} value of the waffle diode in size A is obviously the smallest among all ESD diodes. Taking the multi-waffle diode in size C and waffle diode in size A for comparison, the I_{CP}/A_{Layout} value of multi-waffle N+/P_{sub} (P+/N_{well}) diode are higher than that of waffle diode about 66% (59%). It implies that the effect of local heat dissipation is truly getting serious to degrade the current-handling capability when the diode size is getting small.

Although the waffle diodes in size A and size B theoretically have larger ratio of junction perimeter to total junction area as shown in Fig. 8, the size of waffle diode is still required to be carefully optimized. The penalties of parasitic sidewall capacitance and significant reduction on I_{CP} due to local heat dissipation for the waffle diode in small size are emerged. Therefore, it should not to simply shrink the device size of waffle diode for achieving better FOMs. Based on the FOMs illustrated in Figs. 15–18, the characteristics of the diodes in large size can be improved to the level of waffle diodes in small size by adequately modifying the layout style. Overall, the diodes with new modified layout styles are superior to those waffle diodes in small size for implementing to the high-speed I/O circuits with the consideration of layout area.

4. Conclusion

The ESD diodes with new modified layout styles, which are called as multi-waffle and multi-waffle-hollow, have been successfully verified in a 90-nm CMOS technology. They are characterized in terms of some FOMs ($R_{ON} * C_{ESD}$, I_{CP}/C_{ESD}, V_{HBM}/C_{ESD}, and I_{CP}/A_{Layout}) to evaluate the suitability for high-speed I/O applications. It is expected that the FOMs of the ESD diode can be improved by maximizing the ratio of junction perimeter to junction area. However, it is found that the FOMs of waffle diodes with continuously shrinking size would be limited due to emerged parasitic sidewall capacitance and local heat dissipation in small layout area. As a result, the FOMs of waffle diodes will not be further improved by simply shrinking the diode size to maximize the ratio of junction perimeter to total junction area.

The new proposed diodes with multi-waffle and multi-waffle-hollow layout styles have been demonstrated. The new proposed diodes in large size can avoid the penalty of local heat distribution. The reduction of junction area by using new modified layout styles is the key factor to significantly improve the FOMs of the ESD diodes. As compared to the FOMs of waffle diodes, it reveals that the FOMs values of the large size diodes can be enhanced by modifying the layout styles. Therefore, the proposed multi-waffle and multi-waffle-hollow diodes are also adequate to be implemented to high-speed I/O applications with small layout area.

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